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A Novel High Schottky Barrier Based Bilateral Gate and Assistant Gate Controlled Bidirectional Tunnel Field Effect Transistor

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ABSTRACT In this article, we propose a high Schottky barrier source/drain contacts based bilateral gate and assistant Gate controlled bidirectional tunnel field Effect transistor (HSB-BTFET). Different from Schottky barrier (SB) MOSFET which use lower Schottky barrier to produces the thermionic emission current, the proposed HSB –BTFET utilizes higher Schottky barrier to minimize the thermionic emission current and adopts bilateral gate to generate a strong band-to-band tunneling (BTBT) current which works as the conduction mechanism of the forward current. An assistant gate is introduced which efficiently blocks the reverse biased leakage current. Compared to SB MOSFET, HSB-BTFET can realize lower subthreshold swing, much smaller leakage current, higher $I_{on} - I_{off}$ ratio, compared to TFET, it can realize larger forward current. Besides the device symmetry, it's more compatible with MOSFET technology. The function and influence of the Schottky barrier height have been analyzed.

INDEX TERMS Bidirectional TFET, Schottky barrier, BTBT, MOSFET, SB-MOSFET.

I. INTRODUCTION

The research on the basic unit of integrated circuit focuses on two aspects. One is to improve the integration, multi-gate FETs [1]–[2] is impressive in sub-30nm technology nodes. The other is the performance promotion, novel devices are purposefully developed, among which TFET is the most representative [3]–[11]. Unfortunately, it is difficult to make the abrupt junction at a small size. This imposes severe limitations on the processing thermal budget and necessitates the development of costly millisecond annealing techniques. SB-MOSFET forms Schottky barrier instead of the p-n junction barrier of MOSFET [12]–[14]. The metallic source/drain (S/D) architecture holds the advantage to relax severe constraints imposed to conventional implanted S/D [15]. For p-type SB MOSFETs, the height of Schottky barrier for holes in valence band ϕ_{Bp} is set to be much smaller than the one for electrons in conduction band ϕ_{Bn} . For the most ideal case, ϕ_{Bp} is 0V, and the device can work as an ideal pn junction based p-type MOSFET which shows subthreshold swing (SS) ($d(\log(I_{DS}))/dV_{GS}$) equals to 60mV/dec at

room temperature [16], for a finite Schottky barrier height, the thermionic emission current is always smaller than in the ideal 0V barrier height case, thereafter, the SS of SB MOSFETs is often larger than 60mV/dec, the inability of subthermal SS through a Schottky barrier without considering others physical mechanisms such as band-to-band tunneling (BTBT) has been proved by a simple potential mapping method [17]. However, in the reversely biased state, BTBT induced leakage current will be significantly increased, even larger than the forward current [18]. These physical mechanisms lead to that both the on-off current ratio and the forward-reverse current ratio of SB MOSFET are lower than the ones of conventional MOSFET. TFET as the most representative novel device utilizes BTBT as the current conduction mechanism which can realize subthermal SS [19]–[22]. To realize larger forward current and smaller SS, the generation efficiency of BTBT should be increased as much as possible, that means the gate control ability should be strengthened and a sharp abrupt junction between the heavily doped region and intrinsic region should

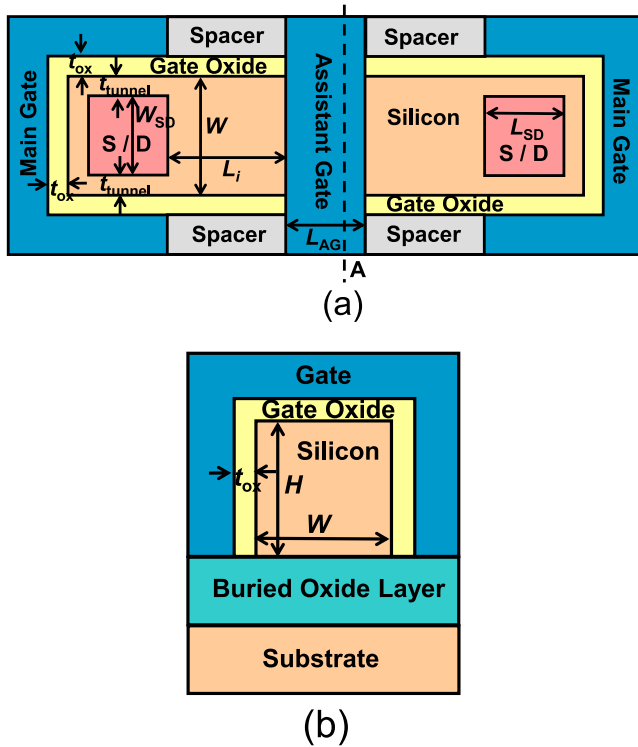


FIGURE 1. (a) A schematic view of the top view of HSB-BTFET, (b) the cross view of HSB-BTFET along the cut line A in (a).

be formed [20]–[22], it is the same problem which should be faced by MOSFET. Therefore, this requirement also increases the manufacturing difficulty of TFET with high performance. The dissymmetry of TFET makes it hard to completely replace the MOSFET which is with symmetrical structural features. Taking the N-type TFET as an example, if the potential difference between n+ drain and the p+ source is reversely biased ($V_{DS} < 0$), the p-n junction formed by source and drain is always forwardly biased, the gate electrode will be failed to switch it, the switching characteristic is invalid. Circuit functional modules (such as transmission gates) which need to make use of the bidirectional switching characteristics of transistors to work are hard to be realized by TFET.

II. DEVICE DESCRIPTION

A. DEVICE STRUCTURE

The Fig. 1 (a) is a schematic view of the top view of HSB-BTFET, Fig. 1(b) is the cross view of HSB-BTFET along cut line A in Fig. 1 (a). The source/drain regions are symmetric and interchangeable. Take n-type as example, the source/drain interfaces form Schottky contacts. The main gate is formed on both lateral sides which near to source and drain regions, the shape of the main control gate is similar to a pair of brackets and controls three sides of the silicon. The assistant gate controls the central part of the silicon body. L_i is the length of the intrinsic silicon region between the source/drain contact and the assistant gate contact, H is the height of the silicon body, t_{ox} is the thickness of gate oxide, L_{SD}

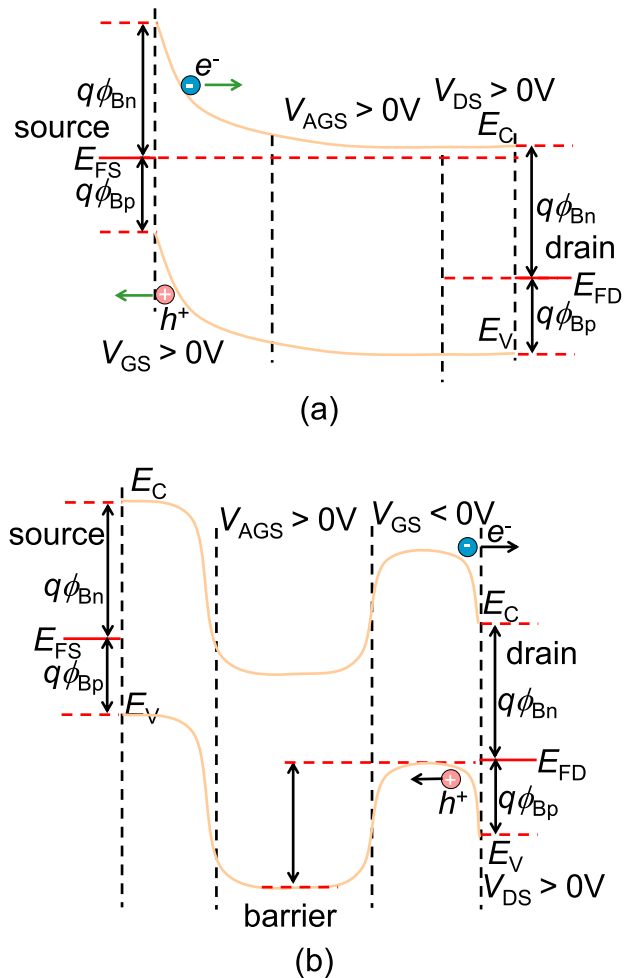


FIGURE 2. Schematic view of the energy band diagram of the proposed HSB-BTFET (a) from source to drain under forward V_{AG} , forward V_{DS} bias and forward V_{GS} biases, (b) from source to drain under forwardly biased V_{AG} , forwardly biased V_{DS} and reversely biased V_{GS} biases.

and W_{SD} are the length and width of source/drain contacts, respectively. t_{tunnel} is the thickness of the intrinsic tunneling region between gate oxide and source/drain contact, L_{AG} is the length of the assistant gate, W is the width of the silicon body.

B. DESIGN CONCEPTION AND OPERATING PRINCIPLE

Considering that the subthermal SS can be obtained by BTBT on an abrupt junction, and the metallic junction is sharper than doping based junction, metallic junctions are adopted to form Schottky barrier. Different from SB MOSFET, the a higher Schottky barrier is utilized to block the Schottky barrier thermionic emission current. In order to reduce the leakage current as much as possible, the carriers produced near the source/drain regions under a reversely biased condition should be effectively blocked. For SB MOSFET, no matter how ϕ_{Bn} is set, a large amount of leakage cannot be avoided, take n type SB MOSFET as example, if ϕ_{Bp} is set to be larger than ϕ_{Bn} , although the hole thermionic emission current could be largely reduced, however, BTBT leakage can be enhanced, too. If ϕ_{Bp} is set to be smaller than ϕ_{Bn} ,

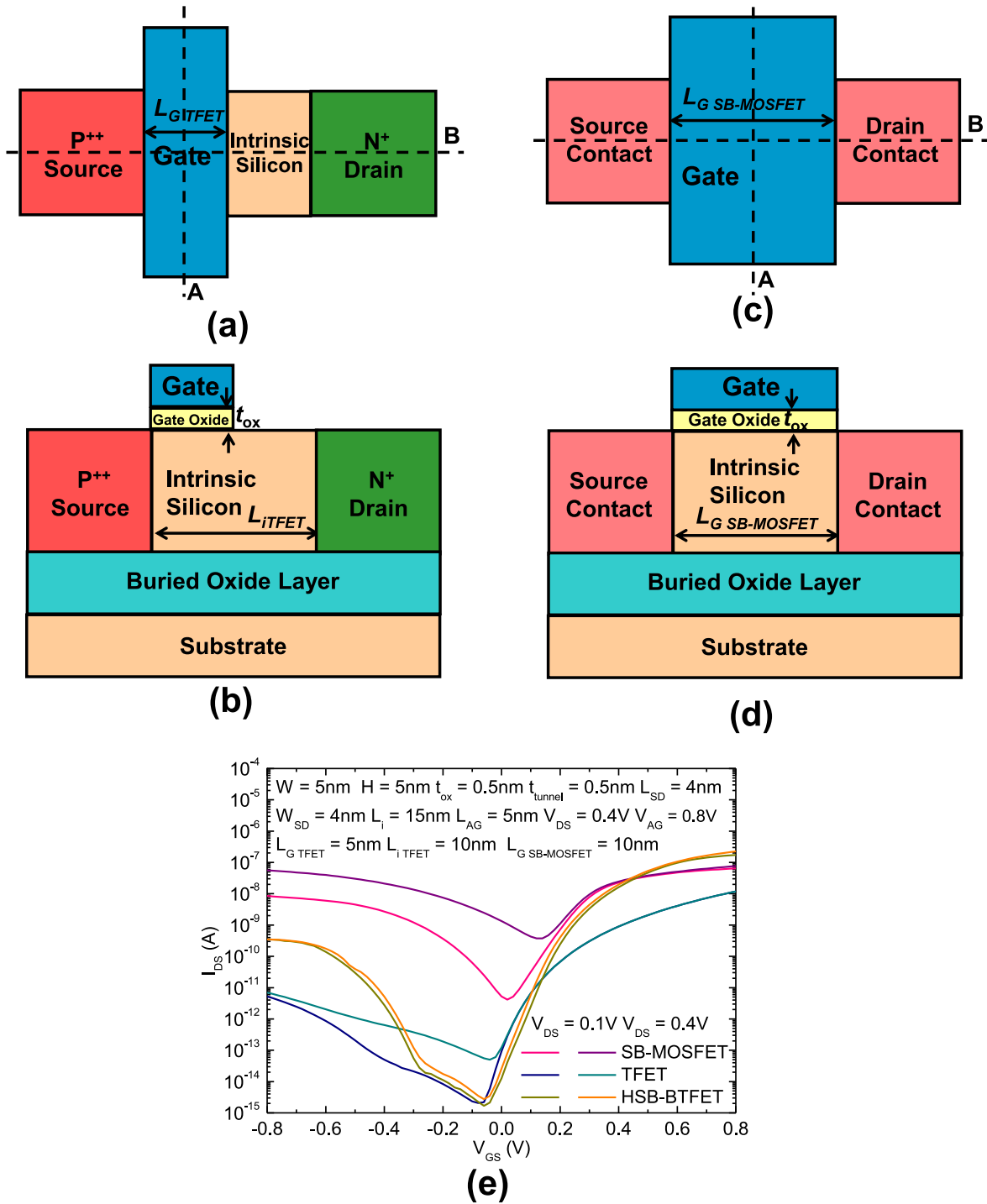


FIGURE 3. (a) A schematic view of the top view of conventional TFET, (b) the cross view of conventional TFET along the cut line B in (a), (c) A schematic view of the top view of SB-MOSFET, (d) the cross view of SB-MOSFET along the cut line B in (c), (e) the transfer characteristics comparison between HSB-BTFET, TFET and SB-MOSFET.

then the forward biased electron thermionic emission current which flows in the conduction band will be largely reduced and the reversely biased hole thermionic emission current which flows in the valence band is strengthened. Then the forward current of SB MOSFET is even smaller than the reversely biased current. An assistant gate is in the central

part and sets it at a constant bias to block the leakage current. Fig. 2 (a) and Fig. 2. (b) show schematic view of the energy band diagram of HSB-BTFET from source to drain under forwardly biased V_{AG} , V_{DS} , V_{GS} and under forwardly biased V_{AG} , V_{DS} , reversely biased V_{GS} , respectively. E_C and E_V are the bottom of the conduction band and the top of

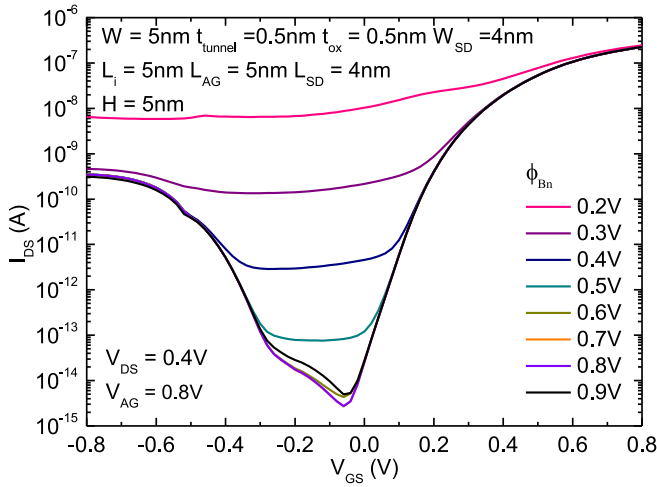


FIGURE 4. The transfer characteristics of HSB-BTFET with different ϕ_{Bn} s.

the valence band, respectively. E_{FS} and E_{FD} are the quasi Fermi level of the source and the drain contact, respectively. Take n type HSB-BTFET as an example, as Fig. 2(a) shows, if both the main gate and the assistant gate are forwardly biased, electron hole pairs generated by BTBT mainly in the source tunnel layer, the holes flow to the source contact, and the electrons in the conduction band flow to the drain contact due to that there is no barrier formed for electrons from source to drain. As Fig. 2. (b) shows, if the main gate is reversely biased and the assistant gate is still maintain the forwardly biased state, the electron hole pairs generated by BTBT mainly in the drain region (V_{DG} is larger than V_{SG}), the electrons flow to the drain contact, however, the forwardly biased assistant gate creates a potential barrier for the holes which can efficiently prevent the holes from flowing to the source contact, thereafter, large amount reversely biased leakage current can be blocked.

III. ANALYSIS AND DISCUSSIONS

The characteristics of the proposed HSB-BTFET have been verified by device simulation using SILVACO Tools [23]. Physical models such as Shockley-Read-Hall recombination model, auger recombination model, Fermi-Dirac statistic model, mobility models, band gap narrowing model, a standard band to band tunneling model, Fowler-Nordheim tunneling model are all turn on. Fig. 3 (a) shows a schematic view of the top view of conventional TFET, Fig. 3 (b) shows the cross view of conventional TFET along the cut line B in Fig. 3 (a), Fig. 3 (c) shows a schematic view of the top view of SB-MOSFET, Fig. 3 (d) shows the cross view of SB-MOSFET along the cut line B in Fig. 3 (c). Both the cross view of conventional TFET along the cut line A in Fig. 3 (a) and the cross view of SB-MOSFET along the cut line A in Fig. 3 (c) are the same with Fig. 1 (b). L_{GTFT} is the gate length of the conventional TFET, L_{iTFET} is the intrinsic silicon body length of the conventional TFET, and $L_{GSB-MOSFET}$ is the gate length of the

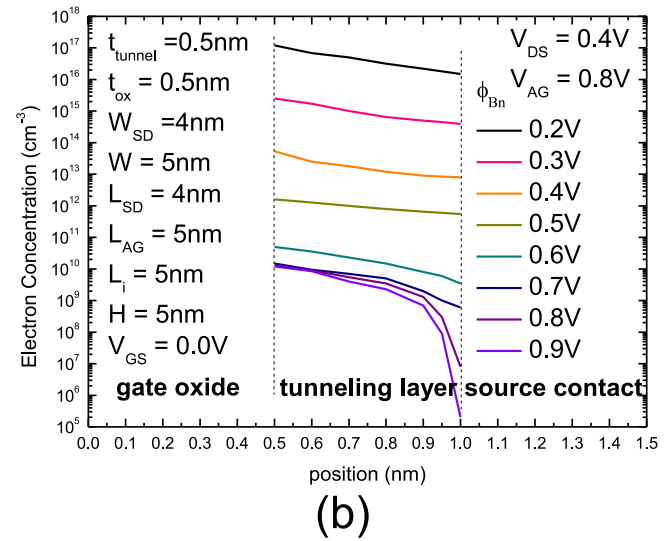
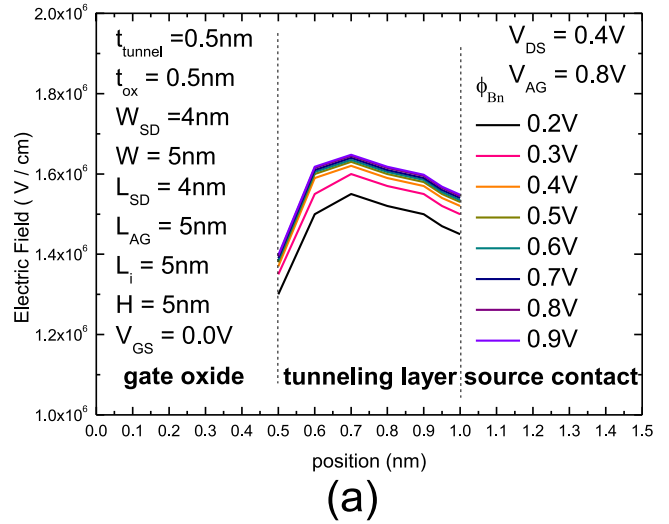


FIGURE 5. (a) The electric field distribution in tunneling layer with different ϕ_{Bn} s, (b) The electron distribution in tunneling layer with different ϕ_{Bn} s.

SB-MOSFET. Fig. 3 (e) shows the transfer characteristics comparison between HSB-BTFET, TFET and SB-MOSFET, ϕ_{Bn} for HSB-BTFET is 0.8V. ϕ_{Bn} of SB-MOSFET is set to be 0.3V. The doping concentration of P^{++} region of TFET is set to be $10^{20}cm^{-3}$. As descriptions, the reversely biased transfer characteristics of SB-MOSFET is poor, the leakage current is enhanced for larger V_{DS} . The forward current of TFET is relatively small. The HSB-BTFET shows higher on-current and sharper SS compared to TFET and SB-MOSFET. The HSB-BTFET shows much lower leakage current compared to SB-MOSFET, especially for larger V_{DS} bias.

Fig. 4. shows the transfer characteristics of HSB-BTFET with different ϕ_{Bn} s. Its value varies from 0.2V to 0.9V. Due to that the assistant gate is always forwardly biased, no barrier for electrons forms in the central part of the device, thereafter, for a smaller ϕ_{Bn} , the thermionic electron current which flows from source to drain is also larger, which

leads to more leakage current flow in both subthreshold region and reversely biased region. As ϕ_{Bn} is increased, the Schottky barrier height for electrons is increased, too. Then thermionic electron current can be also effectively reduced and the BTBT current becomes dominant. The forward and reverse current ratio can be larger than 10^3 , and the $I_{on} - I_{off}$ ratio is larger than 10^7 for ϕ_{Bn} higher than 0.6V. The average SS is 42 mV/dec. It should be noted that the value of L_i should be larger than 4nm, because reducing L_i means that the minimum distance between gate electrode and the assistant gate is reduced, which will enhance the electric field effect between the two gates, resulting in the increase of reverse leakage current and degradation of subthreshold characteristics.

As Fig. 5 (a) shows, the electric field distribution in tunneling layer does not significantly change with different ϕ_{Bn} , it is because that the potential difference between the gate electrode and the source electrode does not change with ϕ_{Bn} , thereafter, the BTBT current will not significantly affected by the changing of ϕ_{Bn} . Fig. 5 (b) shows the electron distribution in tunneling layer with different ϕ_{Bn} . As the ϕ_{Bn} is increased, the thermionic electron current will be greatly restricted by the blocking of the increasing height of the Schottky barrier. For ϕ_{Bn} larger than 0.6V, the electron concentration on the interface between gate oxide and tunneling layer will almost not be affected, and the electron concentration will be dominantly controlled by V_{GS} .

IV. CONCLUSION

In this article, we propose a novel HSB -BTFT. It utilizes a higher Schottky barrier to minimize the thermionic emission current. BTBT current works as the conduction mechanism of the forward current. An assistant gate is introduced which can efficiently block the reverse leakage current. Compared to conventional SB MOSFET or TFET, the proposed device can realize lower subthreshold swing, much smaller reversely biased leakage current, higher $I_{on} - I_{off}$ ratio. Compared to conventional TFET, it can realize larger on current and $I_{on}-I_{off}$ ratio, besides the device symmetry makes it more compatible with MOSFET technology

CONFLICTS OF INTEREST

There are no conflicts to declare.

REFERENCES

- [1] J. P. Colinge, "Multi-gate SOI MOSFETs," *Microelectron. Eng.*, vol. 84, pp. 2071–2076, Sep./Oct. 2007.
- [2] X. Liu, M. Wu, X. Jin R. Chuai, and J. H. Lee, "Simulation study on deep nanoscale short channel junctionless SOI FinFETs with triple-gate or double-gate structures," *J. Comput. Electron.*, vol. 13, pp. 509–514, Feb. 2014.
- [3] D. Sarkar *et al.*, "A subthermionic tunnel field-effect transistor with an atomically thin channel," *Nature*, vol. 526, pp. 91–95, Sep. 2015.
- [4] E. Ko, H. J. Lee, J.-D. Park, and C. H. Shin, "Vertical tunnel FET: Design optimization with triple metal-gate layers," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 5030–5035, Dec. 2016.
- [5] J. C. Lee, T. J. Ahn, and Y. S. Yu, "Work-function engineering of source-overlapped dual-gate tunnel field-effect transistor," *J. Nanosci. Nanotechnol.*, vol. 18, no. 9, pp. 5925–5931, 2018.
- [6] B. Raad, K. Nigam, D. Sharma, and P. Kondekar, "Dielectric and work function engineered TFET for ambipolar suppression and RF performance enhancement," *Electron. Lett.*, vol. 52, no. 9, pp. 770–772, Apr. 2016.
- [7] D. H. Ilatikhameh, T. A. Ameen, G. Klimeck, J. Appenzeller, and R. Rahman, "Dielectric engineered tunnel field-effect transistor," *IEEE Electron Device Lett.*, vol. 36, no. 10, pp. 1097–1100, Oct. 2015.
- [8] S. Sahay and M. J. Kumar, "Controlling the drain side tunneling width to reduce ambipolar current in tunnel FETs using heterodielectric BOX," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3882–3886, Nov. 2015.
- [9] J. Madan and R. Chaujar, "Interfacial charge analysis of heterogeneous gate dielectric-gate all around-tunnel FET for improved device reliability," *IEEE Trans. Device Mater. Rel.*, vol. 16, no. 2, pp. 227–234, Jun. 2016.
- [10] B. R. Raad, K. Nigam, D. Sharma, and P. N. Kondekar, "Performance investigation of bandgap, gate material work function and gate dielectric engineered TFET with device reliability improvement," *Superlattices Microstruct.*, vol. 94, pp. 138–146, Jun. 2016.
- [11] M. Rahimian and M. Fathipour, "Improvement of electrical performance in junctionless nanowire TFET using hetero-gate-dielectric," *Mater. Sci. Semicond. Process.*, vol. 63, pp. 142–152, Jun. 2017.
- [12] F. Bashir, A. G. Alharbi, and S. A. Loan, "Electrostatically doped DSL Schottky barrier MOSFET on SOI for low power applications," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 19–25, 2017.
- [13] F. Bashir, S. A. Loan, M. Rafat, A. Alamoud, and S. A. Abbasi, "A high-performance source engineered charge plasma-based Schottky MOSFET on SOI," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp. 3357–3364, Oct. 2015.
- [14] S. Kale and P. N. Kondekar, "Design and investigation of double gate Schottky barrier MOSFET using gate engineering," *Micro Nano Lett.*, vol. 10, no. 12, pp. 707–711, Dec. 2015.
- [15] S. D. Kim, C.-M. Park, and J. C. S. Woo, "Advanced model and analysis for series resistance in sub-100 nm CMOS including poly depletion and overlap doping gradient effect," in *Int. Electron Devices Meeting Tech. Dig. (IEDM)*, San Francisco, CA, USA, 2000, pp. 723–724.
- [16] Y. J. Zhao *et al.*, "Understanding the impact of schottky barriers on the performance of narrow bandgap nanowire field effect transistors," *Nano Lett.*, vol. 12, pp. 5331–5336, Sep. 2012.
- [17] P. M. Solomon, "Inability of single carrier tunneling barriers to give subthermal subthreshold swings in MOSFETs," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 618–620, Jun. 2010.
- [18] A. V. Penumatcha, R. B. Salazar, and J. Appenzeller, "Analysing black phosphorus transistors using an analytic Schottky barrier MOSFET model," *Nat. Commun.*, vol. 6, p. 8948, Nov. 2015.
- [19] U. E. Avci, D. H. Morris, and I. A. Young, "Tunnel field-effect transistors: Prospects and challenges," *IEEE J. Electron Devices Soc.*, vol. 3, pp. 88–95, 2015.
- [20] Q. T. Zhao *et al.*, "Strained Si and SiGe nanowire tunnel FETs for logic and analog applications," *IEEE J. Electron Devices Soc.*, vol. 3, pp. 103–114, 2015.
- [21] G. V. Luong *et al.*, "Strained silicon complementary TFET SRAM: Experimental demonstration and simulations," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 1033–1040, 2018.
- [22] G. V. Luong *et al.*, "Complementary strained Si GAA nanowire TFET inverter with suppressed ambipolarity," *IEEE Electron Device Lett.*, vol. 37, no. 8, pp. 950–953, Aug. 2016.
- [23] *Device Simulation—New Features in 2019 Baseline Release*. Accessed: Feb. 2020. [Online]. Available: https://www.silvaco.com/products/tcad/device_simulation/device_simulation.html