Received 16 July 2020; accepted 29 August 2020. Date of publication 1 September 2020; date of current version 22 September 2020.
The review of this article was arranged by Editor S. Menzel.

Digital Object Identifier 10.1109/JEDS.2020.3020976

Negative Capacitance Double-Gate Junctionless FETs: A Charge-Based Modeling Investigation of Swing, Overdrive and Short Channel Effect

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This work was supported by the European Research Council (ERC) through the ERC Advanced Grants Milli-Tech under Grant 695459 (ERC Millitech).

ABSTRACT In this article, an analytical predictive model of the negative capacitance (NC) effect in symmetric long channel double-gate junctionless transistor is proposed based on a charge-based model. In particular, we have investigated the effect of the thickness of the ferroelectric on the I-V characteristics. Importantly, our model predicts that the negative capacitance minimizes short channel effects and enhances current overdrive, enabling both low power operation and more efficient transistor size scaling, while the effect on reducing subthreshold slope shows systematic improvement, with subthermionic subthreshold slope values at high current levels. Our predictive results in a long channel junctionless with NC show an improvement in ON current by a factor of 6 in comparison to junctionless FET. The set of equations can be used as a basis to explore how such a technology booster and its scaling will impact the main figures of merit of the device in terms of power performances and gives a clear understanding of the device physics. The validity of the analytical model is confirmed by extensive comparisons with numerical TCAD simulations in all regions of operation, from deep depletion to accumulation and from linear to saturation.

INDEX TERMS Negative capacitance, charge-based model, double-gate junctionless FET, short channel effect.

I. INTRODUCTION

Advanced aggressive scaling of conventional metal-oxide-semiconductor field-effect transistors (MOSFET) requires the use of advanced processing with multiple additive technology boosters, such as strain, high-k dielectrics with metal gate stacks, shallow junctions and the replacement of the silicon channel with materials having higher carrier mobility [1], [2]. Even more sophisticated techniques for locally controlling the strain have been proposed in various research works [3]. Significant efforts are needed for the junction and contact engineering in such advanced MOSFETs. A lot of effort has been recently dedicated to the so-called steep-slope transistors [4] but their maturity is still far from being adopted by the nanoelectronics industry. In an attempt to remove all the limitations related to the junction engineering at nanoscale, the concept of junctionless field-effect transistors (JLFET) has been proposed, where the conduction in a very thin, highly doped semiconductor film is controlled by a gate field effect. Because of the absence of source and drain junctions, junctionless transistors are free from steps to create ultra-steep junctions and high thermal annealing for S/D dopant activation, which is a big advantage for scaling and cost reduction at the nanoscale [5].

However, the scaling of MOS devices must cope with issues such as increased power consumption and degraded off-state current [6] upon reduction of the power supply to mitigate power consumption. The main parameter limiting the power supply voltage scaling in MOS devices is the

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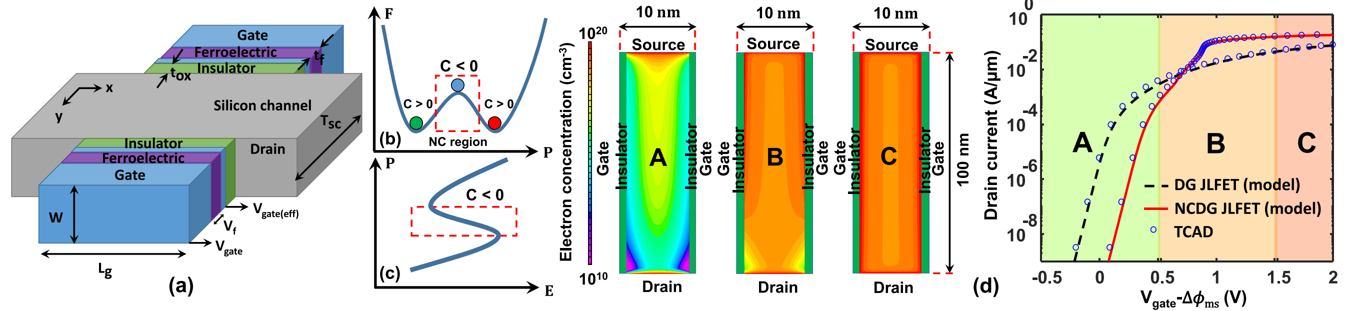

FIGURE 1. (a) 3-D Schematic view of a double-gate JLFET with negative capacitance. (b) The double-well free energy in ferroelectric versus the electric polarization (*P*) from the Landau theory of ferroelectrics. (c) Polarization of ferroelectric as a function of the electric field. The red rectangular in (b) and (c) denotes the region of negative capacitance. (d) Drain current versus the applied gate voltage and electron concentration corresponds to depletion, accumulation and hybrid channel mode of a junctionless transistor at $V_{DS} = 1$ V.

intrinsic limit of 60 mV/dec at 300 K of the subthreshold swing (SS). To overcome this, it was proposed to add to the conventional insulator of the gate oxide a ferroelectric material of a given thickness that will create an effective negative capacitance, resulting in a reduction of the transistor body factor below unity. This would lead to SS values lower than 60 mV/dec [7]–[15]. Having negative capacitance means that a given charge density in the channel can be achieved with a lower gate voltage.

In this work, we investigated by calibrated modeling and simulations, the effect of negative capacitance on the characteristics of junctionless transistors. The phenomena of a ferroelectric material have been modeled by Ginzburg and Devonshire which is based on the Landau theory of phase transitions [16]. Landau theory can predict the behavior of ferroelectric material. To the best of our knowledge, it is the most common approach to the study of negative capacitance effects with ferroelectrics [8]–[14], [16]–[18]. The simulation and modeling study of negative capacitance in the MOSFETs has been investigated in the literature [19]–[23]. Also, some studies have been done to investigate the short channel effect in inversion-mode NC FETs, a majority of them being based on detailed simulations [24]–[26]. However, none of them is an analytical charge-based model and there is no evidence of modeling and investigating the short channel effect in NC JLFETs based on solving 2D Poisson-Boltzmann relationships.

Thus, in order to take account the ferroelectric in junctionless transistors in a simple and compact model approach, in this work, we propose analytical and explicit relationships taking into account the negative capacitance effect in Double-Gate JLFET (NCDG JLFET) and evidences an amplification of the current-voltage dependence with respect to the ferroelectric thickness. This model relies on the charge-based approach developed in [27]–[33]. This approach will be validated with technology computer-aided design (TCAD) simulations in all regions of operation from deep depletion to accumulation and linear to saturation. The effect of the negative capacitance on DIBL (Drain Induced Barrier Lowering) based on the 2D Poisson-Boltzmann relationship is also addressed.

II. MODELING APPROACH

Three-dimensional schematic of the structure of the symmetric double-gate junctionless transistor with the ferroelectric layer is shown in Fig. 1.a. In this structure, an intermediate metallic layer is considered between the insulator and the ferroelectric material. This inner metal film in the gate stack architecture imposes a uniform electric field inside the ferroelectric [7]. Also, in this article, we assume a single-domain ferroelectric film for simplicity. Hence, the single-domain Landau-Khalatnikov theory will be eligible for modeling the ferroelectric dielectric. It has been reported in [34] that in a case in which we have a multi-domain ferroelectric film, using an inner metal cannot stabilize negative capacitance. However, a lot of empirical works have been done with inner metal and they observe the NC effect [7]–[12]. The reason could be that in reality, one of the domains might be dominant and the worst case is that only the biggest domain will stabilize which is similar to a single-domain case. We call the potential of this inner metal layer $V_{gate(eff)}$ and the potential of the real gate, V_{gate}. Hence the potential across the ferroelectric can be expressed as

$$V_f = V_{gate} - V_{gate(eff)}. \tag{1}$$

According to the Landau theory, the Gibbs free energy $F(J/m)$ of the ferroelectric material, respect to the polarization P is

$$F = \alpha P^2 + \beta P^4 + \gamma P^6 - \vec{E}\vec{P}, \tag{2}$$

where α, β, γ are ferroelectric material constants and $\vec{E}$ is the electric field in the ferroelectric. The F-P curve has two minima as shown in Fig. 1.b. These represent the two counter stable states in the ferroelectric material ($\pm P$) which can be switched by applying an external electric field (note that since the electric field and polarization are uniform and aligned with the y-axis, we will consider them as scalars). Then we have $Q = P$ and $V_f = Et_f$ [13], where Q is the charge density of the ferroelectric (per unit area) and t_f is the ferroelectric thickness. The derivation of $U_F = Ft_f$ with respect to Q gives (see Fig. 1.c)

$$\frac{\partial U_F}{\partial Q} = 2\alpha t_f Q + 4\beta t_f Q^3 + 6\gamma t_f Q^5 - V_f - Q\frac{\partial V_f}{\partial Q}, \tag{3}$$

The capacitance is related to the slope of the *P-E* curve as follows (see the Appendix)

$$C = \frac{1}{t_f}\left(\epsilon_0 + \frac{dP}{dE}\right), \tag{4}$$

thus, as illustrated in Fig. 1.b and c, there is a region where the capacitance is negative (red rectangular). The negative capacitance region is naturally unstable but can be stabilized when combined with an ordinary capacitor in series [13]. The free energy of an ordinary capacitor (C_D) which is in series with the ferroelectric is given by [34]

$$U_D = \frac{Q^2}{2C_D} - QV_D, \tag{5}$$

where V_D is the potential across the ordinary capacitor. Therefore, the minimum of the total free energy ($U = U_D + U_F$) happens when $\partial U/\partial Q = 0$

$$V_f + V_D = \frac{Q}{C_D} + 2\alpha t_f Q + 4\beta t_f Q^3 + 6\gamma t_f Q^5 - Q\frac{\partial V_G}{\partial Q}, \tag{6}$$

where $V_G = V_f + V_D$ is a constant voltage across the ferroelectric-insulator stack and we also know $V_D = Q/C_D$. Hence, NC happens for a specific Q-V_f relationship

$$V_f = 2\alpha t_f Q + 4\beta t_f Q^3 + 6\gamma t_f Q^5. \tag{7}$$

From the charge-based model in [27], [28], what we know is the relationship between the $V_{gate(eff)}$ and the charge density in the channel. In addition, from (1) and (7), we also know how V_{gate} and $V_{gate(eff)}$ are interrelated. These sets of relations will be now combined to simulate the device characteristics with respect to the external voltages (gate, source, and drain).

A. RECALLING JLFET CORE EQUATIONS

We consider an n-type long-channel symmetric double-gate JLFET with ferroelectric material (as shown in Fig. 1.a) with a doping density N_D, a channel length, thickness and width L_g, T_{sc} and W respectively. Gate oxide and ferroelectric film thicknesses are t_{ox} and t_f. Device parameters are listed in Table 1. When the JLT is OFF, the channel becomes depleted of majority carriers and results in negligible current conduction (See A in Fig. 1.d). By increasing the gate voltage carriers can pass through the channel and the electron concentration increases (See B in Fig. 1.d). Finally, when the JLT is ON a high electron concentration in the channel appears, facilitating current conduction between source and drain (See C in Fig. 1.d) [35]. According to the derivation of the charge-based model for double-gate symmetric JLFETs developed in [27]–[30], we have the two following relationships which link The total charge in the semiconductor, Q_{sc} and the effective gate voltage ($V_{gate(eff)}$):

$$\left(\frac{Q_{sc}}{2\epsilon_{si}}\right)^2 = \frac{2qn_iU_T}{\epsilon_{si}}\left\{\exp\left(\frac{\psi_0 - V_{ch}}{U_T}\right)\left[\exp\left(\frac{\psi_s - \psi_0}{U_T}\right) - 1\right] - \frac{N_D}{n_i}\left(\frac{\psi_s - \psi_0}{U_T}\right)\right\}, \tag{8}$$

$$Q_{sc} = -2C_{ox}\left(V_{gate(eff)} - \Delta\phi_{ms} - \psi_s\right), \tag{9}$$

where ψ_s and ψ_0 are the surface potential and the center potential respectively, n_i is the intrinsic carrier concentration, ϵ_{si} is the permittivity of silicon, V_{ch} is the quasi-Fermi potential, $U_T = k_BT/q$ is the thermal voltage, C_{ox} is the capacitance of the insulator, $\Delta\phi_{ms}$ denotes the difference between the work function of metal and the work function of the intrinsic semiconductor, other symbols having their usual meaning.

A.1. DEPLETION MODE

In depletion mode, the potential at the center of the semiconductor channel is higher than the surface potential, and the net charge density in the semiconductor is positive ($Q_{sc} \geq 0$). Therefore, the exponential term in (8) is negligible. By manipulating [27]–[30], the effective gate potential in the depletion mode with respect to the total charge density is as follows

$$V_{gate(eff)} = \Delta\phi_{ms} + V_{ch} - \frac{Q_{sc}}{2C_{ox}} + U_T\ln\left(\frac{N_D}{ni}\right) + U_T\ln\left[1 - \left(\frac{Q_{sc}}{Q_f}\right)^2\right] - \frac{Q_{sc}^2}{8C_{sc}Q_f}, \tag{10}$$

where $Q_f = qN_DT_{sc}$ is the fixed charge in the channel and $C_{sc} = \epsilon_{si}/T_{sc}$.

A.2. ACCUMULATION MODE

Under accumulation mode, the last term in (8) is always smaller than the exponential term, which leads to a negative charge density in the semiconductor ($Q_{sc} \leq 0$). In addition, in accumulation, the center potential remains close to the value it takes at the flat-band condition $\psi_0 \approx V_{ch}+U_T\ln(N_D/n_i)$ [27]. Therefore, the effective gate voltage in accumulation mode becomes

$$V_{gate(eff)} = \Delta\phi_{ms} + V_{ch} - \frac{Q_{sc}}{2C_{ox}} + U_T\ln\left(\frac{N_D}{ni}\right) + U_T\ln\left(1 + \frac{Q_{sc}^2}{\theta}\right), \tag{11}$$

where $\theta = 8\epsilon_{si}qN_DU_T$.

A.3. DRAIN CURRENT

The relationships derived previously (10) and (11) for depletion and accumulation modes give rise to explicit relationships for the channel current [27]. The drain current in depletion is given by

$$I_{Dep} = \mu\frac{W}{L_g}\left[\left(\frac{1}{8C_{sc}} - \frac{1}{4C_{ox}}\right)Q_{sc}^2 - \frac{Q_{sc}^3}{12Q_fC_{sc}} + \left(\frac{Q_f}{2C_{ox}} + 2U_T\right)Q_{sc} - U_TQ_f\ln\left(1 + \frac{Q_{sc}}{Q_f}\right)^2\right]_S^D, \tag{12}$$

and in accumulation we have

$$I_{Acc} = \mu\frac{W}{L_g}\left[\left(\frac{Q_f}{2C_{ox}} + 2U_T\right)Q_{sc} - \frac{1}{4C_{ox}}Q_{sc}^2 - U_T Q_f \ln\left(1 + \frac{Q_{sc}^2}{8Q_f C_{sc} U_T}\right) - 2U_T\sqrt{8Q_f C_{sc} U_T}\arctan\left(\frac{Q_{sc}}{\sqrt{8Q_f C_{sc} U_T}}\right)\right]_S^D, \quad (13)$$

where μ is the free carrier mobility assumed constant along the channel in this work. Also, for gate voltages where a hybrid channel takes place [27], i.e., part of the channel (near the source) in accumulation and the rest in depletion, the drain current becomes

$$I_{hyb} = I_{Acc}\Big|_S^{FB} + I_{Dep}\Big|_{FB}^{D}. \quad (14)$$

B. MERGING JLFET WITH FERROELECTRIC

B.1. LANDAU EQUATION

In this section, we will merge the model of the JLFET described above with the core relation governing the ferroelectric layer.

B.2. TOTAL CHARGE DENSITY

To obtain V_f from (7) the total charge density in the ferroelectric material Q must be known. This is obtained by calculating the integral of the semiconductor charge density over the channel length

$$WL_g \times 2Q = -\int_0^{L_g} WQ_{sc}dx. \quad (15)$$

The total charge density is the sum of fixed and mobile charges $Q_{sc} = Q_f + Q_m$. Hence, we can write

$$L_g \times 2Q = -Q_f L_g - \int_0^{L_g} Q_m dx. \quad (16)$$

Although we do not know how Q_m is related to x, we know the relation between Q_m and V_{ch} from (10) and (11) in depletion and accumulation modes respectively. In addition, from the drain current I_{ds} relationship, dx and V_{ch} are linked as follows

$$dx = -\frac{\mu Q_m}{I_{ds}}dV_{ch}. \quad (17)$$

By substituting (17) in (16) the integral in space turns into an integral over the potential of the channel from the source (S) to the drain (D)

$$Q = -\frac{Q_f}{2} + \frac{\mu}{2L_g I_{ds}}\int_S^D Q_m^2 dV_{ch}. \quad (18)$$

In depletion mode, dV_{ch} is obtained from (10) as follows

$$dV_{ch} = \left(\frac{1}{2C_{ox}} + \frac{2U_T Q_{sc}}{Q_f^2 - Q_{sc}^2} + \frac{Q_{sc}}{4C_{sc}Q_f}\right)dQ_{sc}. \quad (19)$$

Since $dQ_{sc} = dQ_m$, we introduce (19) in (18). After solving the integral, an analytical and explicit relation for the total charge in the ferroelectric is obtained (in depletion mode):

$$Q = -\frac{Q_f}{2} + \frac{\mu}{2L_g I_{ds}}\left\{\frac{Q_m^3}{6C_{ox}} + 2U_T\left[Q_m Q_f - \frac{Q_m^2}{2} - 2Q_f^2\ln(2Q_f + Q_m)\right] + \frac{Q_m^4}{16C_{sc}Q_F} + \frac{Q_m^3}{12C_{sc}}\right\}_S^D. \quad (20)$$

In accumulation, we have

$$dV_{ch} = \left(\frac{1}{2C_{ox}} + \frac{2U_T Q_{sc}}{Q_{sc}^2 + \theta}\right)dQ_{sc}. \quad (21)$$

Substituting (21) in (18) and then solving the integral gives an analytical and explicit relationship for the total charge density of the ferroelectric when the whole device is biased in accumulation:

$$Q = -\frac{Q_f}{2} + \frac{\mu}{2L_g I_{ds}}\left\{\frac{Q_m^3}{6C_{ox}} - 2U_T\left[\frac{Q_m^2}{2} + \frac{Q_f^2 - \theta}{2}\ln(Q_{sc}^2 + \theta) - Q_m Q_f + 2Q_f\sqrt{\theta}\arctan\left(\frac{Q_{sc}}{\sqrt{\theta}}\right)\right]\right\}_S^D. \quad (22)$$

The way charges and voltages have been calculated is now explained: for a given effective gate voltage $V_{gate(eff)}$, the total charge density of ferroelectric Q is known either from (20) or (22). Next, introducing Q in (7) and using equation (1), the applied gate voltage V_{gate} is finally obtained.

Proceeding through this sequence greatly simplifies the way plots are obtained, avoiding cumbersome self-consistent calculations, and providing a clear and simple understanding of the imbrication of the different parts of the model.

To confirm the validity of the model, we performed simulations with TCAD software. The simulation result of NCDG JLFET is numerically calculated by combining SILVACO TCAD software with a MATLAB script to include the Landau equation.

For extracting the coefficients in relation (7), we rely on the data published in [17], where authors fabricated and characterized metal–ferroelectric–metal (MFM) capacitors by using an HZO film as a ferroelectric material in 11.6 nm thickness. They extracted a *P-E* hysteresis loop with a remanent polarization P_r of about 17 μC/cm^2 and a coercive field E_c of about 1.2 MV/cm. By using the experimental data of remanent polarization and coercive field and based on the approach presented in [36], we extracted the

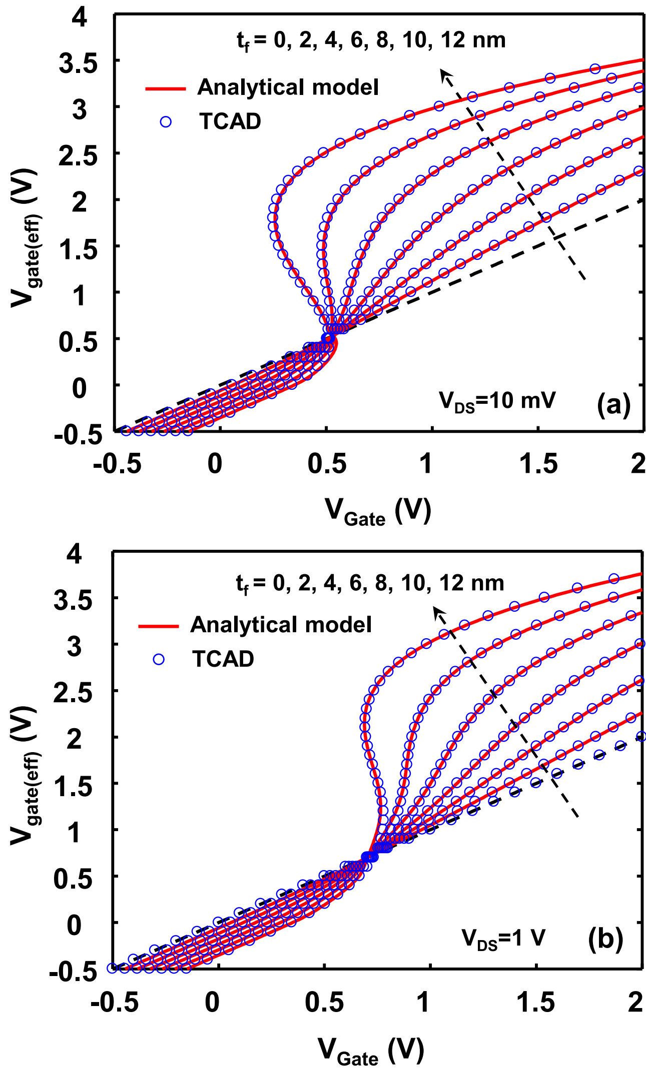

FIGURE 2. The potential of middle metal versus the applied gate voltage from the analytical model (lines) and TCAD simulations (circles) for the various thickness of ferroelectric from 2 nm to 12 nm (a) at V_{DS} = 10 mV and (b) V_{DS} = 1 V. By increasing the thickness of ferroelectric the voltage amplification increases.

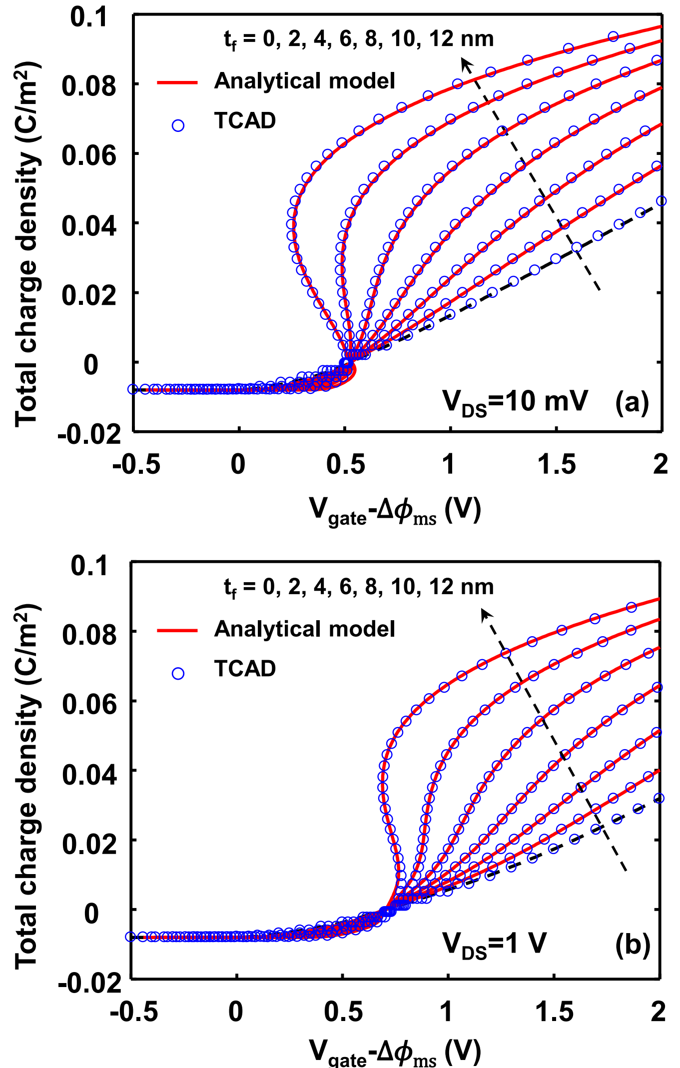

FIGURE 3. The total charge density in the ferroelectric versus the applied gate voltage from the analytical model (lines) and TCAD simulations (circles) for the various thickness of ferroelectric from 2 nm to 12 nm (a) at V_{DS} = 10 mV and (b) V_{DS} = 1 V.

Landau coefficients. The effect of the film thickness on the ferroelectricity of an HZO film has been studied in [37]. The coercive electric field of the HZO film is almost constant in various thicknesses. However, its remnant polarization decreases when the film thickness increases. This effect has been attributed to the change in the grain size of the HZO film during the atomic layer deposition (ALD) process [37]. Unlike HZO and hafnia films with other dopants, Gd:HfO_2 shows no reduction of the polarization in a different range of ferroelectric material [38]. Nevertheless, this effect merely changes the Landau coefficients for the different thicknesses of the ferroelectric film but the model can still predict the NC effect properly with the new coefficients. Also, for such a thin HZO film and high applied gate voltage, charge trapping effects might observe [17]. However, we have proposed a core model and one can include this effect by employing the approach which is developed in our previous work [30].

Next, we consider a double gate JLFET with 100 nm channel length, 1 μm channel width, and with 10 nm of silicon thickness. The doping density and oxide thickness were set respectively to $N_D = 10^{19}$ cm^{-3} and 1 nm (see Table 1).

Fig. 2.a and b show the applied gate voltage versus the effective gate voltage for various thicknesses of the ferroelectric ranging from 2 nm to 12 nm, both at low and high V_{DS} respectively. Lines and blue circles have been used for the analytical model and TCAD simulations, respectively. The analytical model at both low and high V_{DS} demonstrates a full agreement with TCAD simulations. It can be seen that increasing the thickness of the ferroelectric layer increases the voltage amplification, which is the signature of the negative capacitance effect. The total charge density of the ferroelectric versus the applied gate voltage at $V_{DS} = 10$ mV and $V_{DS} = 1$ V obtained from TCAD simulations and from the model is plotted in Fig. 3.a and Fig. 3.b.

TABLE 1. Device parameters used for TCAD and model.

Gate oxide thickness	t_{ox}	1 nm
Channel length	L_g	100 nm
Channel Width	W	1 µm
Channel thickness	T_{sc}	10 nm
Doping concentration	N_D	$10^{19}\,\mathrm{cm}^{-3}$
Ferroelectric thickness	t_f	0 − 12 nm
Remanent polarization	P_r	17 µC/cm^2
Coercive field	E_c	1.2 MV/cm

To summarize, the total charge density of ferroelectric is now known in all regions of operation from depletion (20) to accumulation (22), resulting in a relationship between $V_{gate(eff)}$ and V_{gate}. Furthermore, we know the link between $V_{gate(eff)}$ and the mobile charge density in the channel, and so the relationship between V_{gate} and Q_m, giving finally the expected $I_D - V_{gate}$ dependence.

Fig. 4.a and b illustrate the drain current versus the applied gate voltage at $V_{DS} = 10$ mV and $V_{DS} = 1$ V for ferroelectric thicknesses from 8 nm to 12 nm. Increasing the thickness of ferroelectric causes a shift to the higher voltage in the subthreshold region, because in subthreshold the amount of fixed charge in the channel dominates over the mobile charge ($-Q_f/2$ in equation (20)). This makes a constant background of charge density regarding to the t_f in the Landau equation. Beyond a threshold voltage, the slope increases and above a critical thickness t_{cr} a snaps back due to the hysteresis effect of a ferroelectric layer is observed. These regions are unstable which are depicted with a rectangular in Fig. 4. In order to have a non-hysteretic operation, the total gate capacitance should be positive in the whole range of the gate voltage [18]. Fig. 5.a shows SS versus the drain current in different thicknesses of ferroelectric at low and high V_{DS}. It illustrates that NC systematically reduces SS, even if not sub-60 mV/dec in all regimes. Subthermionic values down to sub 30 mV/dec are achieved at moderate drain currents and low V_{DS} (see Fig. 5.b). It means that NC still causes a significant improvement in the overdrive voltage. On the other hand, by using a negative capacitance, we gain a remarkable increase in ON current as illustrated in Fig. 5.c. Fig. 5.c shows the percentage of increment of drain current versus applied gate voltage in different thicknesses of the ferroelectric layer.

Our results are conceptually in agreement with the experimental and simulation works [9], [18]. But it is worth noting that these are different from previous work on modeling and simulation of a junctionless transistor with ferroelectric [23] where no such behavior was evidenced.

III. SHORT CHANNEL EFFECT

In this section, we investigate how negative capacitance can affect the DIBL short channel effect. To this purpose, we need to solve the two-dimensional Poisson-Boltzmann relationship in the channel in the subthreshold. This was done for a regular JLFET in [29].

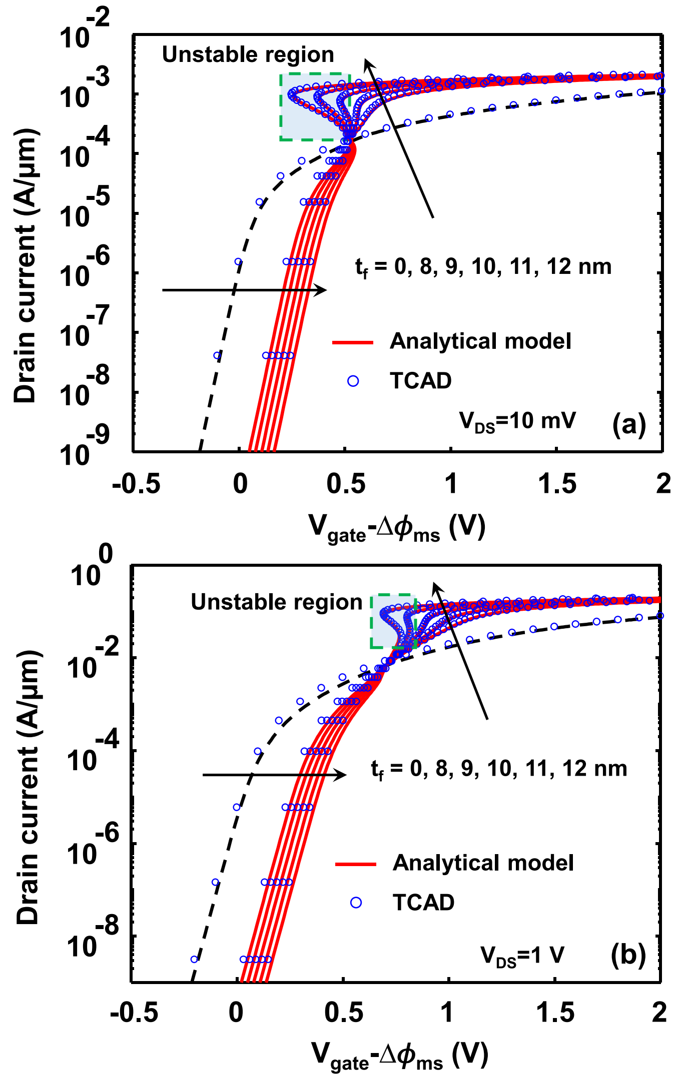

FIGURE 4. Drain current versus the applied gate voltage from the analytical model (lines) and TCAD simulations (circles) for the various thickness of ferroelectric from 8 nm to 12 nm (a) at $V_{DS} = 10$ mV and (b) $V_{DS} = 1$ V.

The potential distribution obtained from the 2D Poisson-Boltzmann relation is expressed as follows [29]:

$$\psi(x,y) = \psi_s(x)\left[1 + y(1 - \frac{y}{T_{sc}})\frac{C_{ox}}{\epsilon_{si}}\right] + (\Delta\phi_{ms} - V_{gate(eff)})y(1 - \frac{y}{T_{sc}})\frac{C_{ox}}{\epsilon_{si}}, \quad (23)$$

where $\psi_s(x)$ is the surface potential at $y = 0$ and $y = T_{sc}$ which is defined as follows

$$\psi_s(x) = \eta\exp(\delta x) + \zeta\exp(-\delta x) + \lambda, \quad (24)$$

$$\delta = \sqrt{\frac{2C_{ox}}{\epsilon_{si}T_{sc}}}, \quad (25)$$

$$\lambda = V_{gate(eff)} - \Delta\phi_{ms} + \frac{qN_D}{\delta^2\epsilon_{si}}, \quad (26)$$

$$\zeta = \frac{-\lambda\left[\exp(\delta L_g) - 1\right] - V_{DS}}{2\sinh(\delta L_g)}, \quad (27)$$

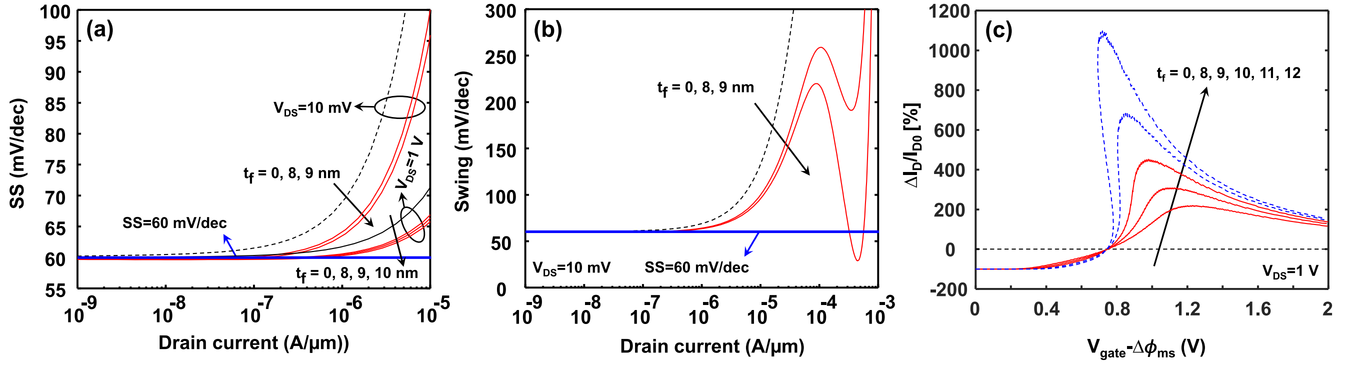

FIGURE 5. (a) SS versus the drain current in different thicknesses of ferroelectric for the various thickness of ferroelectric. (b) Swing versus the drain current for the various thickness of ferroelectric at $V_{DS} = 10$ mV. (c) The percentage of increment of drain current ($\Delta I_D/I_{D0}$) versus applied gate voltage for the various thickness of ferroelectric from 8 nm to 12 nm. Thicknesses of ferroelectric in which NCDG JLFET operates in the hysteretic regime have been shown with dash lines.

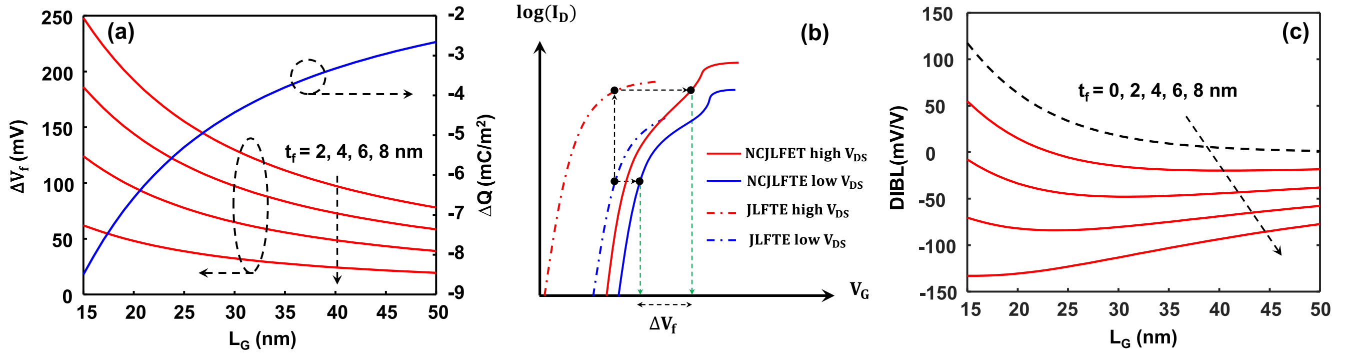

FIGURE 6. (a) The difference of the potential across the ferroelectric (left axis) and the difference of total charge density of ferroelectric (right axis) in high V_{DS} and low V_{DS} versus the channel length. ΔV_f somehow represents ΔV_G. The model confirms that ΔV_f and the absolute value of ΔQ increase by going to the shorter channel length.(b) The schematic of the I-V characteristic of a regular double gate JLFET and a double gate JLFET with negative capacitance at low and high V_{DS}. (c) DIBL of an NCDG JLFET in different thicknesses of ferroelectric versus the channel length.

$$\eta = -\zeta - \lambda, \tag{28}$$

By introducing the surface potential from equation (24) in (9), the total charge density in the channel (which is a function of V_{DS}) becomes

$$Q_{sc} = -2C_{ox}\Big\{V_{gate(eff)} - \Delta\phi_{ms} - \big[\eta\exp(\delta x) + \zeta\exp(-\delta x) + \lambda\big]\Big\}, \tag{29}$$

Finally, the total charge density in the ferroelectric can be obtained by substituting (29) in (15) and calculating the integral along the lateral direction of the channel from 0 to L_g:

$$Q = \frac{C_{ox}}{L_g}\Bigg\{(V_{gate(eff)} - \Delta\phi_{ms} - \lambda)L_g - \left[\frac{\eta}{\delta}\exp(\delta L_g) - \frac{\zeta}{\delta}\exp(-\delta L_g) + \frac{\zeta-\eta}{\delta}\right]\Bigg\}. \tag{30}$$

Since Q is a function of the drain voltage, we can estimate how much V_{DS} affects the charge density of ferroelectric. Therefore, we define $\Delta Q = Q_h - Q_l$ as the difference in the charge density of ferroelectric between high and low V_{DS}:

$$\Delta Q = \frac{-2C_{ox}\Delta V_{DS}}{2L_g\delta\sinh(\delta L_g)}\big[\cosh(\delta L_g) - 1\big], \tag{31}$$

where $\Delta V_{DS} = V_{DS(high)} - V_{DS(low)}$.

To find ΔV_f, the difference of the electrostatic potential across the ferroelectric at high and low V_{DS}, we neglect the coefficient γ. Hence, ΔV_f becomes

$$\Delta V_f = \left(2\alpha t_f Q_h + 4\beta t_f Q_h^3\right) - \left(2\alpha t_f Q_l + 4\beta t_f Q_l^3\right), \tag{32}$$

which can be further simplified

$$\Delta V_f = 2\alpha t_f\Delta Q + 4\beta t_f\Delta Q^3 + 12\beta t_f\Delta Q^3 Q_h Q_l. \tag{33}$$

It happens that Q_h and Q_l are the only contributions to ΔV_f that depend on the effective gate voltage. Still, it happens that the last term in (33) containing these quantities is negligible, meaning that we can approximate ΔV_f as follows

$$\Delta V_f \approx 2\alpha t_f\Delta Q + 4\beta t_f\Delta Q^3. \tag{34}$$

Fig. 6.a depicts ΔV_f and ΔQ versus the channel length on the left and right axis respectively. We see that the absolute value of ΔQ increases by going to the shorter channel lengths, and as a result, ΔV_f increases as well. This is

an advantage because it predicts that negative capacitance mitigates short channel effect at high V_{DS}. Actually ΔV_f represents somehow ΔV_G, i.e., the difference of V_G between high and low V_{DS}.

The schematic drawing in Fig. 6.b illustrates this effect. It compares the *I-V* characteristic of a regular double gate JLFET and a double gate JLFET in presence of negative capacitance at low and high V_{DS}. As we mentioned in the previous section, a negative capacitance causes a potential amplification as much as V_f. Although V_f is almost the same for high and low V_{DS} for the long channel device, it becomes less effective at low V_{DS} in regard to high V_{DS} for a short channel device. In fact, in presence of short channel effect, the *I-V* characteristic that shifts towards high V_{DS} is compensated by ΔV_f in NCDG JLFET, thus DIBL reduction in a specific thickness of the ferroelectric film would be feasible.

Unlike conventional MOSFETs where DIBL is related to the shift in the surface potential since most of the current flow from the Si-SiO_2 interface, in JLFETs when they operate below the threshold, the interface no longer represents the lowes energy across the channel and the DIBL must be calculated from the center potential shift upon the drain voltage as follows [28], [29]

$$DIBL_{\Delta\psi} = \frac{\Delta\psi_{BCP,min}}{\Delta V_{DS}}, \tag{35}$$

where $\Delta\psi_{BCP,min}$ is the difference of minimum body center potential in low and high V_{DS}. We know from [28], [29] that the body center potential is linked to the surface potential:

$$\psi_{BCP} = a\psi_s + b, \tag{36}$$

where a and b coefficients are given by

$$a = 1 + \frac{1}{8}\delta^2 T_{sc}^2, \tag{37}$$

$$b = (a-1)(\Delta\phi_{ms} - V_{gate} + V_f). \tag{38}$$

Therefore, the difference of body center potential of an NCJLFET in low and high V_{DS} will be

$$\Delta\psi_{BCP} = a\Delta\psi_s + (a-1)\Delta V_f. \tag{39}$$

Then $\Delta\psi_s$ obtains from (9) as follows

$$\Delta\psi_s = -\Delta V_f + \frac{\Delta Q_{sc}}{2C_{ox}}. \tag{40}$$

We can replace ΔQ_{sc} with $\Delta Q_{sc_{JL}} + \Delta Q'_{sc}$ where $\Delta Q_{sc_{JL}}$ is the difference of the total charge density in the semiconductor in a normal JLFET without NC. Hence, $\Delta\psi_s$ links to the difference of the surface potential of a normal JLFET in low and high V_{DS} ($\Delta\psi_{s_{JL}} = \Delta Q_{sc_{JL}}/2C_{ox}$) as follows

$$\Delta\psi_s = \Delta\psi_{s_{JL}} - \Delta V_f + \frac{\Delta Q'_{sc}}{2C_{ox}}. \tag{41}$$

If we neglect $\Delta Q'_{sc}/2C_{ox}$ and introduce (41) in (39), we will have (we know that $\Delta\psi_{BCP_{JL}} = a\Delta\psi_{s_{JL}}$)

$$\Delta\psi_{BCP} \approx \Delta\psi_{BCP_{JL}} - \Delta V_f. \tag{42}$$

Therefore, DIBL in NCJLFET shifts as much as $\Delta V_f/\Delta V_{DS}$ respect to the DIBL in a JLFET.

$$DIBL_{\Delta\psi} \approx DIBL_{\Delta\psi_{JL}} - \frac{\Delta V_f}{\Delta V_{DS}}, \tag{43}$$

where $DIBL_{\Delta\psi_{JL}}$ defines as follows [28], [29]

$$DIBL_{\Delta\psi_{JL}} = \frac{2a\sqrt{\eta'\zeta'}}{\Delta V_{DS}}\left(\sqrt{1 + \frac{\Delta}{\eta'} - \frac{\Delta}{\zeta'} - \frac{\Delta^2}{\eta'\zeta'}} - 1\right), \tag{44}$$

$$\zeta' = \frac{(-b - a\lambda)\left[\exp(\delta L_g) - 1\right] - V_{DS}}{2a\sinh(\delta L_g)}, \tag{45}$$

$$\eta = -\frac{b}{a} - \zeta' - \lambda, \tag{46}$$

$$\Delta = \frac{\Delta V_{DS}}{2a\sinh(\delta L_g)}. \tag{47}$$

Fig. 6.c shows DIBL of an NCDG JLFET in different thicknesses of ferroelectric versus the channel length. We see that the value of DIBL decreases by increasing the thickness of the ferroelectric. As expected, in the short channel lengths, the different amount of potential drops across the ferroelectric film at low and high V_{DS} which causes a reduction in the DIBL even to the negative values. Hence, it appears that by choosing a proper thickness for the ferroelectric film, an improvement in the DIBL would be achievable, e.g., in our case $t_f \approx 3$ nm gives the lowest DIBL. Further studies for an optimization DIBL strategy and trade-offs with other performance figures of merit are needed, which was beyond the scope of this article.

IV. CONCLUSION

An analytical charge-based model for symmetric double-gate junctionless FETs with negative capacitance was developed. The model incorporates the impact of the negative capacitance of ferroelectric on DC electrical characteristics of double gate JLFETs by proposing an analytical and explicit equation for the total charge density of ferroelectric in depletion and accumulation modes. The model confirms that using the negative capacitance in junctionless transistors means that the gate overdrive voltage decreases, which can be interpreted as lower energy consumption. The model also shows that the subthreshold slope almost remains constant in NCDG JLFET, but an improvement of swing for above the threshold causes a significant enhancement in ON current. In addition, an analysis of the short channel effect predicts an improvement when negative capacitance is observed. The model has been compared to TCAD simulations with an excellent agreement in all regions of operation from deep depletion to accumulation and linear to saturation.

APPENDIX

The total polarization P can be expressed as the sum of a linear and switching dipole P_D contributions as follows [39]

$$P = \epsilon_0\chi E + P_D. \tag{48}$$

Hence, the surface charge density σ of ferroelectric becomes

$$\sigma = V\frac{\epsilon_f}{t_f} + P_D, \tag{49}$$

where $\epsilon_f = \epsilon_0(1+\chi)$. Thus the capacitance becomes

$$C = \frac{d\sigma}{dV} = \frac{1}{t_f}\left(\epsilon_f + t_f\frac{dP_D}{dV}\right). \tag{50}$$

We can replace dV with $t_f dE$ and then $dP_D/dE = dP/dE - \epsilon_0\chi$. Therefore, the capacitance is related to the slope of the P-E curve as expressed in (4).

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