Received 7 August 2020; revised 21 August 2020; accepted 25 August 2020. Date of publication 28 August 2020; date of current version 4 November 2020.
The review of this article was arranged by Editor S. Menon.

Digital Object Identifier 10.1109/JEDS.2020.3020186

Quasi-Normally-Off AlGaN/GaN HEMTs With SiN_x Stress Liner and Comb Gate for Power Electronics Applications

WEI-CHIH CHENG [1,2] (Graduate Student Member, IEEE), FANMING ZENG [1,3,4,5], MINGHAO HE [1,6], QING WANG [1,3,4,5], MANSUN CHAN [2] (Fellow, IEEE), AND HONGYU YU [1,3,4,5] (Senior Member, IEEE)

1 School of Microelectronics, Southern University of Science and Technology, Shenzhen 518055, China
2 Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong
3 Engineering Research Center of Integrated Circuits for Next-Generation Communications, Ministry of Education, Shenzhen 518055, China
4 Shenzhen Institute of Wide-Bandgap Semiconductors, Shenzhen 518100, China
5 Key Laboratory of the Third Generation Semi-conductor, Southern University of Science and Technology, Shenzhen 518055, China
6 Department of Electrical and Computer Engineering, National University of Singapore, Singapore 117583

CORRESPONDING AUTHORS: Q. WANG AND H. YU (e-mail: wangq7@sustech.edu.cn; yuhy@sustech.edu.cn)

This work was supported in part by the Key-Area Research and Development Program of Guangdong Province under Grant 2019B010128001 and Grant 2019B010142001; in part by the Shenzhen Municipal Council of Science and Innovation under Grant JCYJ20180305180619573 and Grant JCYJ20170412153356899; and in part by the National Natural Science Foundation of China under Grant 61704004.

ABSTRACT Recess processes for the fabrication of normally-off GaN HEMTs generally compromise devices' on-state performance. In this work, recess-free quasi-normally-off GaN HEMTs with a threshold voltage of 0.24 V is realized by local control of two-dimensional electron gas (2DEG) density. The devices feature a 0.1 μm gate length, SiN_x stress liner, and comb gate. SiN_x liner can provide significant stress to AlGaN/GaN heterostructure in the scaled gate region. The additional stress translates to the additional electric field and depletes the 2DEG in the gate region. As a result, the quasi-normally-off operation is achieved. Furthermore, the comb gate structure is introduced to suppress the short channel effects, supported by TCAD simulation. The quasi-normally-off devices' excellent on-state performances are benchmarked against the normally-off devices reported recently and a p-GaN HEMT purchased from a commercial foundry. The results support strain engineering as a promising technique to pursue the normally-off operation of GaN HEMTs.

INDEX TERMS High electron mobility transistor (HEMT), gallium nitride (GaN), strain engineering.

I. INTRODUCTION

GaN high electron mobility transistors (HEMTs) have been proven competitive for power switch applications. The high critical electric field of GaN leads to the high breakdown voltage, and the inherent two-dimensional electron gas (2DEG) at the AlGaN/GaN heterojunction enables the low on-resistance [1]–[4]. The inherent 2DEG conducting channel makes GaN HEMTs normally-on devices. However, devices' normally-off characteristics are preferred for power switch applications to ensure the fail-safe operation [3].

Among several approaches attempting to realize the normally-off GaN HEMTs, recessed metal-insulator-semiconductor (MIS) gate and p-GaN gate are the two most trend-leading gate structures [4], [5]. The two gate structures require recess processes for preparation, which usually compromise the devices' performances. Besides, high etching selectivity is hard to attain between AlGaN and GaN, making the process need additional care to maintain. Recess-free approaches have been proposed to realize high-performance normally-off GaN HEMTs, including ultrathin-barrier (UTB) heterostructures and selective area regrowth techniques [6], [7]. However, passivation quality is demanding for UTB HEMTs because the semiconductor surface is close to the conducting channel, enhancing the remote scattering effects. Also, the control of the epitaxy condition is challenging for regrowth techniques.

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

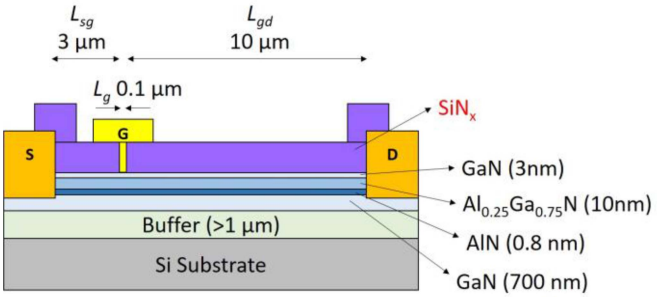

FIGURE 1. Device structure of AlGaN/GaN HEMT with gate length (L_g), source-to-gate length (L_{sg}), and gate-to-drain length (L_{gd}) labeled. The device width is 100 μm. The source/drain lengths are 30μm. The SiN_x layer may be a single low-stress layer (baseline devices) or a dual-layer stress liner (strained devices).

TABLE 1. SiN_x schemes for device groups.

Device group	Non-stress SiN_x [a]	Compressive SiN_x [b]
1. Baseline devices	150 nm	-
2. Strained devices	21 nm	150 nm

[a] 0.3 GPa SiN_x for surface passivation
[b] -1 GPa SiN_x for compression introduction

Due to the piezoelectric nature of GaN, external mechanical stress may create additional polarization charges and modulate threshold voltage (V_{th}) [8]. In order to modulate device characteristics, SiN_x stress liner has been proven to provide significant stress to various kinds of field-effect transistors, especially for the dimension within or below the submicron regime [9], [10]. Therefore, a V_{th} increase can be expected by applying a stress liner with proper stress polarity and gate dimension for GaN HEMTs [8], [11], [12].

In previous work, a dual-layer SiN_x stress liner was developed to provide a satisfactory passivation quality and -1 GPa intrinsic stress [13]. In this work, the quasi-normally-off operation is realized on the AlGaN/GaN HEMTs with 0.1 μm gate length using SiN_x stress engineering. Furthermore, the introduced comb-gate structure can suppress the short channel effects, including drain induced barrier lowering and punch-through. As an extension of the conference presentation [14], the additional TCAD simulation results are implemented to support the increased V_{th} and suppressed short-channel effects, and the switching characteristics of the devices are added. In the absence of the recess processes, the quasi-normally-off devices in this work feature low on-resistance, benchmarked against the normally-off devices reported recently and a p-GaN HEMT purchased from a commercial foundry. The results support the strain engineering as an alternative approach for pursuing high-performance normally-off GaN HEMTs for power electronics applications.

II. DEVICE FABRICATION: ALGAN/GAN HEMTS WITH SIN_X STRESS LINER AND 100 NM GATE

The structure of AlGaN/GaN HEMTs is shown in Fig. 1. The lengths of the source-to-gate, gate, and gate-to-drain are 3, 0.1, and 10 μm. Based on our previous work, the 0.1 μm gate length was selected for better efficiency of introducing the stress from the stress liner [12]. The devices were built on the two-inch Si wafer with MOCVD-grown (Al)GaN epitaxy from Enkris Semiconductor Inc. The epitaxial structure consisted of a 1.05 μm buffer layer, a 700 nm GaN channel layer, a 0.8 nm AlN spacer, a 10 nm $Al_{0.25}Ga_{0.75}N$ barrier, and a 3 nm GaN cap. The barrier thickness and Al composition are customized to attain a channel with the sheet resistance of approximately 400 Ω/□. The GaN cap layer was implemented to prevent the AlGaN layer from oxidation and stress relaxation and flatten the AlGaN surface [15]. The device fabrication started with the device isolation using a BCl_3/Cl_2 based dry etching. Then, Ti/Al/Ti/Au based metal stack was deposited using an e-beam evaporator and annealed at 830°C under nitrogen ambient to form the source/drain Ohmic contacts. The SiN_x layers were deposited by the plasma-enhanced chemical vapor deposition (PECVD) with dual plasma excitation frequencies. The gate region was patterned using e-beam lithography and opened by fluoroform (CHF_3) based dry etching. In this way, the SiN_x film exerts stress in the semiconductor in the gate region near the film edge, according to the edge force model [11]. Subsequently, the Ni/Au metal gate was deposited using an e-beam evaporator, and metal pads were deposited after the via opening.

The stress of SiN_x liners deposited using PECVD with dual plasma excitation frequencies was modulated by adjusting the duration time percentage of low-frequency plasma excitation in each duty cycle [16]. In this work, two groups of devices were fabricated, as listed in Table 1. The first group (baseline devices) has a low-stress (unintentional 0.3 GPa) SiN_x layer. In contrast, the second group (strained devices) possesses a dual-layer scheme that consists of a low-stress interlayer and a compressive layer. The dual-layer stress liner was proved to acquire an adequate passivation quality and intrinsic compressive stress (−1 GPa measured on a Si wafer) [13]. In this article, Group 1 and Group 2 devices are named baseline and strained devices, respectively, even though the SiN_x layer applied onto Group 1 devices is slightly stressed (0.3 GPa). The thicknesses of interlayers were calculated empirically by the deposition rate and time.

III. THRESHOLD VOLTAGE OF ALGAN/GAN HEMTS

The threshold voltage of AlGaN/GaN HEMTs can be expressed as (1) [17].

$$V_{th} = \varphi_m - \triangle E_c - \frac{qN_d d}{2\varepsilon} - \frac{\sigma}{\varepsilon} d \tag{1}$$

where ϕ_m is the Schottky barrier height between the gate metal and AlGaN, and ΔE_c is the conduction band discontinuity between AlGaN and GaN. N_d, d, and ε are the doping concentration, thickness, and dielectric permittivity of the AlGaN barrier. σ is the total sheet charge density at the AlGaN/GAN heterojunction induced by polarization, which

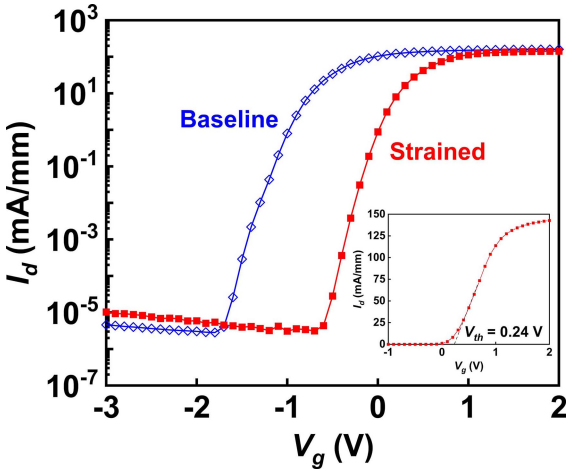

FIGURE 2. Transfer characteristics of the strained device under V_d = 1 V in comparison with the baseline device. The strained device showed V_{th} of 0.24 V, which was defined using the extrapolation in the linear region (ELR) method (inset).

can be defined by (2) [2], [17].

$$\sigma = P_{sp}(AlGaN) - P_{sp}(GaN) + P_{pz}(AlGaN) - P_{pz}(GaN) \tag{2}$$

where P_{sp} and P_{pz} are the spontaneous polarization and piezoelectric polarization charges in the AlGaN and GaN layers, respectively. In the AlGaN/GaN heterostructures, P_{pz}(AlGaN) is caused by the tensile stress due to the lattice mismatch between AlGaN and GaN. P_{pz}(AlGaN) can be calculated with piezoelectric coefficients e_{33} and e_{13} as (3)

$$P_{pz}(AlGaN) = e_{33}\epsilon_z + e_{31}(\epsilon_x + \epsilon_y) \tag{3}$$

where ϵ_x, ϵ_y, and ϵ_z are in-plane strain and the strain along the c-axis [2]. According to equation (1) and (2), introducing in-plane compressive stress can neutralize the in-plane tensile strain in AlGaN. Therefore, P_{pz}(AlGaN) and hence total polarization (σ) reduce, increasing the V_{th} of AlGaN/GaN HEMTs.

IV. ELECTRICAL CHARACTERISTICS OF STRAINED ALGAN/GAN HEMTS

The transfer characteristics of strained devices are shown in Fig. 2. The V_{th} of strained devices is over 1 V higher than that of baseline devices, as predicted by the V_{th} model mentioned in Section III. The V_{th} of the strained devices attain −0.28 V with $I_d = 0.01$ mA/mm as the criterion, and the conducting channel is fully pinched off at approximately −0.6 V. By using the extrapolation in the linear region (ELR) method, the V_{th} of the strained device is found to be 0.24 V (Fig. 2 inset), indicating quasi-normally-off characteristics.

To investigate the stress effects on the device electrical characteristics, Sentaurus TCAD suite from Synopsys Inc. was used to analyze the stress distribution and electrical parameters of devices.

The stress distribution in the gate region of the baseline devices and strained devices were simulated using Sentaurus Process, the results of which are shown in Fig. 3. The device structure for simulation was the same as the devices mentioned in Section II, except that the AlN spacer was neglected for simplification. The intrinsic stress of the compressive SiN_x was set according to the experimental data (−1 GPa). In Fig. 3(a), SiN_x in baseline devices contributes no stress to the system, and the built-in tensile stress in AlGaN is originated from the lattice mismatch between AlGaN and GaN. The lattice mismatch stress is approximately 2.87 GPa for 25% Al content [2]. In Fig. 3(b), the lattice mismatch stress also exists, and the compressive SiN_x introduces an additional compression to the gate region, as expected by the edge force model [11]. As a result, a local compression with up to −3 GPa strength is built in the AlGaN, which can translate to the polarization charges and is expected to increase the device V_{th}.

TABLE 2. Key physical parameters used in simulations.

Physical parameter	Quantity
Fe doping in buffer	$N_{buffer} = 3 \times 10^{16}$ cm^{-3}
Si doping in barrier	$N_{barrier} = 2 \times 10^{16}$ cm^{-3}
Gate metal work function	$\varphi = 5.4$ eV
Mobility	$\mu_{max} = 1350$ cm^{2}V^{-1}s^{-1}
Surface donor-like traps	$N_{TD} = 1.4 \times 10^{13}$ cm^{-2}
	$E_{TD} = E_c - 0.2$ eV
Buffer acceptor-like traps	$N_{TA} = 5 \times 10^{16}$ cm^{-3}
	$E_{TA} = E_c - 0.4$ eV
Piezoelectric coefficients	$e_{33}(Al_{0.25}GaN) = 1.0656 \times 10^{-4}$ C/cm^2
	$e_{33}(GaN) = 8.9841 \times 10^{-5}$ C/cm^2
	$e_{31}(Al_{0.25}GaN) = -5.3183$ C/cm^2
	$e_{31}(GaN) = -5.2964$ C/cm^2

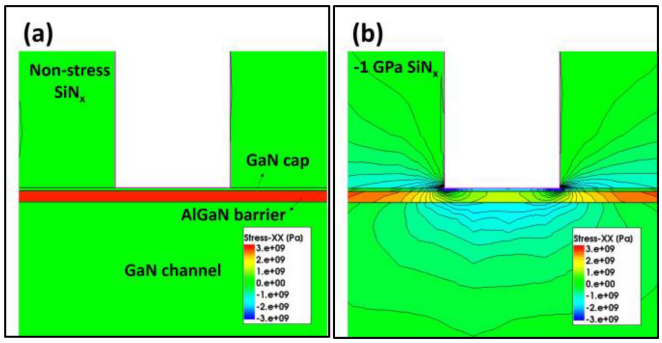

FIGURE 3. Simulated in-plane stress distribution in the gate region of the device with (a) non-stress (baseline device) and (b) −1 GPa SiN_x (strained device). Local compression with up to −3 GPa strength is built in the strained device.

The electrical parameters were simulated using Sentaurus Device. To match the experimental data, the TCAD physical model was calibrated following the procedure detailed in reference [18]. The fitting results of the transfer curve and the output curve of the baseline device are shown in Fig. 4(a) and (b), respectively. The key physical parameters are given in Table 2. A unified Schottky barrier tunneling model is used to account for the gate current [19]. The mobility μ_{max} is the low field mobility in the generic mobility model (4)

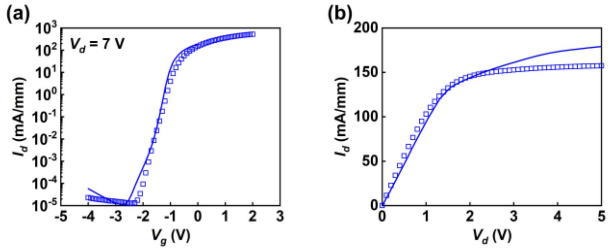

FIGURE 4. Fitting results of (a) transfer curve and (b) output curve of the baseline device. The dots and lines are experimental data and simulation data, respectively.

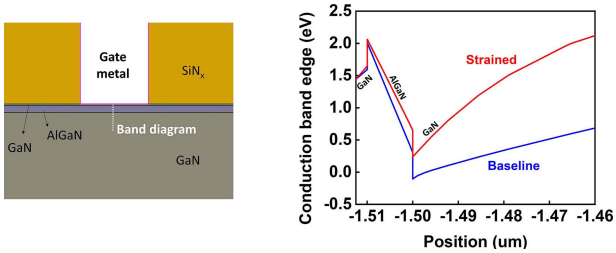

FIGURE 5. Simulated conduction band edge diagram in the middle of the gate region of the baseline and strained device under static condition. The band diagram in AlGaN and GaN layers of the strained device is lifted.

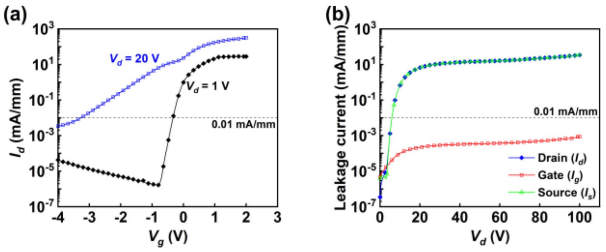

FIGURE 6. (a) The transfer characteristics of the strained device under V_d = 1 V and 20 V. (b) The off-state breakdown characteristics of the strained devices under $V_g = -1$ V. In the off-state breakdown characteristics, the drain current is mainly contributed from the source current.

for electrons:

$$\mu_e(T) = \mu_{max}\left(\frac{T}{T_0}\right) \tag{4}$$

where T_0 is 298 K. To account for the carrier velocity saturation, the Caughey Thomas field-dependent mobility model is used [20]. The epitaxy surface donor-like traps are responsible for the formation of 2DEG. Therefore, surface donors ($N_{TD} = 1.4 \times 10^{13}$ cm^{-2}) at energy level $E_{TD} = E_c - 0.2$ eV are introduced. In addition, acceptor-like traps ($N_{TA} = 5 \times 10^{16}$ cm^{-3} and $E_{TA} = E_c - 0.4$ eV) in the buffer layer are also considered [18]. For the strained device, the external stress was also used as a fitting parameter. The piezoelectric polarization charge introduced by the SiN_x stress liner can be calculated using (3) with default e_{33} and e_{31} defined in Sentaurus Device. The conduction band edge diagram of the baseline and strained device under the static condition (Fig. 5) was simulated using the calibrated physical model. The piezoelectric polarization charge induced by the external stress from the SiN_x stress liner lifts the conduction bands in the AlGaN barrier and GaN channel. Hence, the 2DEG is depleted, increasing the V_{th} of the strained device. The change of the band diagram is similar to the one resulted from inserting a AlGaN back barrier [21]. However, the strain engineering with a SiN_x stress liner is capable of locally changing the band diagram in the gate region, keeping the high-density 2DEG in the access region.

According to the edge force model [11], the gate length of the devices in this work was scaled down to 0.1 μm for the better introduction of the stress from the SiN_x stress liner. However, the scaled gate length may lead to short channel effects, including the drain induced barrier lowering (DIBL) and the punch-through leakage [22], [23]. The transfer characteristics of the strained device measured under $V_d = 1$ V and 20 V are shown in Fig. 6(a). The V_{th} shift is as high as -2.9 V (or $\Delta V_{th}/\Delta V_d = -155$ mV/V), with the criterion of $I_d = 0.01$ mA/mm for defining V_{th}, showing a serious DIBL. The strained device's off-state breakdown characteristics were measured under $V_g = -1$ V with the conducting channel fully pinched off. With the criteria of $I_d = 0.01$ mA/mm, the strained device breaks down before $V_d = 10$ V, as shown in Fig. 6(b). The drain current (I_d) is mainly contributed from the source current (I_s), implying that the punch-through causes the early breakdown.

The gate dimension of the strained devices were scaled in order to better introduce the stress into the semiconductors for realizing the normally-off operation. Unfortunately, the severe short channel effects make the devices hard to be put on the power electronics applications. To address the short channel effects, the comb gate structure was then introduced to the devices.

V. QUASI-NORMALLY-OFF ALGAN/GAN HEMTS WITH STRAINED COMB GATE

The short channel effects are the results of the poor gate control over the conducting channel. To enhance the gate control, the comb gate structure was designed and applied onto the strained devices. The architecture of the device with the comb-gate structure is illustrated in Fig. 7. The fabrication process and device structure were similar to the ones described in Section II for the single-gate strained devices, except that the gate region was extended to 2 μm, and 2, 3, 5, 6, 9, and 11 fingers of 0.1 μm gate were deployed in parallel in the gate region, forming a comb-gate structure. Besides, the gate-to-drain length was extended to 15 μm. The TEM cross-section of the comb-gate structure shows the adequate bottom coverage without sealing-off of the gate opening. More finger numbers were expected to show stronger gate controls. Moreover, the V_{th} shows little dependencies on the number of gate fingers, and the comb-gate devices also show the quasi-normally-off characteristics as the single-gate devices.

In order to evaluate the suppression of short channel effects by the introduction of the comb-gate structure,

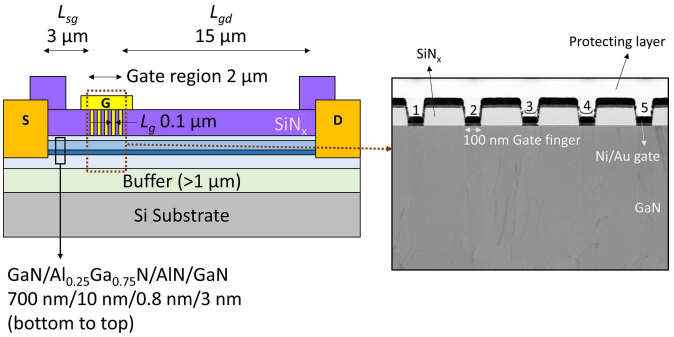

FIGURE 7. **(Left) Device structure of AlGaN/GaN HEMT with the comb-gate structure. The gate region length, gate finger length (L_g), source-to-gate length (L_{sg}), and gate-to-drain length (L_{gd}) were labeled. The SiN_x was a dual-layer stress liner. In the gate region, 2, 3, 5, 6, 9, or 11 0.1 μm fingers were deployed in parallel. (Right) TEM cross-section of the five-finger comb-gate structure.**

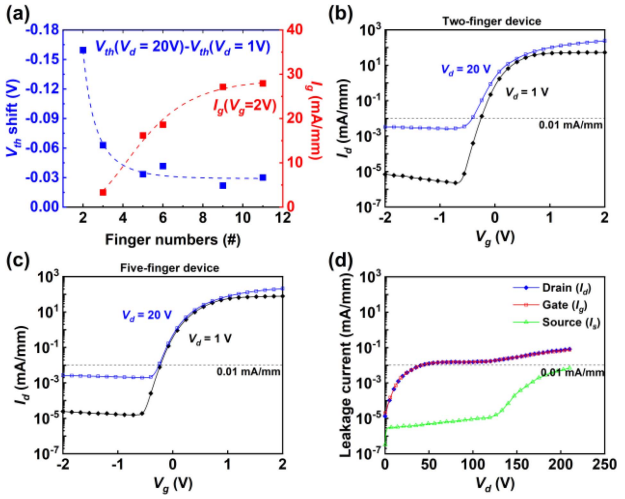

FIGURE 8. **(a) The V_{th} shift of the comb-gate device with various finger numbers under from V_d = 1 V to V_d = 20 V and their gate leakage (I_g) extracted under V_g = 2 V with source and drain grounded. (b) The transfer characteristics of the two-finger comb-gate device under V_d = 1 V and 20 V. (c) The transfer characteristics of the five-finger comb-gate device under V_d = 1 V and 20 V. (d) The off-state breakdown characteristics of the five-finger comb-gate device under V_g = −1. The V_{th} shift decreases as the number of gate fingers increases, and that reaches a plateau after five fingers. The I_g increase with finger numbers. In the off-state breakdown characteristics, the drain current (I_d) is mainly contributed from the gate current (I_g).**

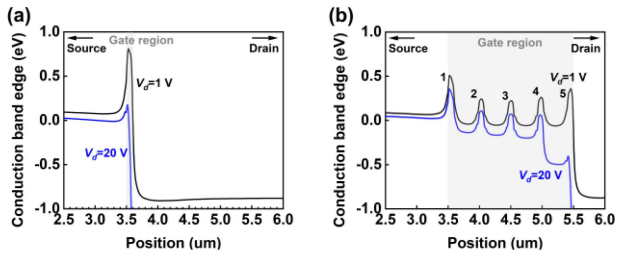

FIGURE 9. **The conduction band diagram of the conducting channel in the gate region of (a) single-gate device and (b) comb-gate device under V_d = 1 V and 20 V.**

the V_{th} shift of the devices with different finger numbers under high V_d were extracted and summarized in Fig. 8(a). Compared with that of the single-gate device (−2.9 V), the V_{th} shift is effectively decreased by introducing the comb-gate structure. The V_{th} shift decreases as the number of gate fingers increases, until reaching a plateau after five fingers, suggesting the well-suppressed short channel effects. The two-finger and five-finger device's transfer characteristics under $V_d = 1$ V and 20 V are plotted in Fig. 8(b) and (c). As shown in Fig. 8(a), the I_g of comb-gate devices under forward bias ($V_g = 2$ V) increases with finger numbers, due to the increased gate region area. Given that I_g under forward bias may limit the overdrive voltage ($V_{ov} = V_g - V_{th}$) and hinder devices' output performances, five finger numbers are chosen for suppressing the V_{th} shift. In the following discussion, the five-finger device represents the comb-gate device to be studied.

Fig. 9 shows the simulated band diagram for the single gate device and the five-finger comb-gate device under off state with $V_d = 1$ V and $V_d = 20$ V. In the gate region of the single gate device, the potential barrier is dramatically lowered by the high drain bias, which is the typical behavior of DIBL. In contrast, the high drain bias mainly affects the region under the two edge fingers on the drain side in the comb-gate device. Quantitatively, the potential barrier height drops 74% when V_d increases from 1 V to 20 V for the single gate device. With the comb-gate structure, the potential barrier lowering is reduced to 13% for finger #2 and #3 labeled in Fig. 9(b), showing the stronger gate coupling to the conducting channel. It is assumed that the punch-through or gate being turned-on happens when all the barriers are lowered. Therefore, the comb-gate structure is believed to suppress short-channel effects, supported by the simulation results.

Regarding the off-state breakdown characteristics, even though the introduction of the comb-gate structure successfully lowers the off-state leakage current by about three orders, the breakdown voltage can attain only tens of volts, as shown in Fig. 8(d). Furthermore, in contrast to the single gate device (Fig. 6(b)), the drain current is mainly contributed by rather the gate current for the comb-gate device than the source current. The short channel effects, including punch-through and DIBL, are suppressed by introducing the comb-gate structure. However, the lack of metal-insulator-semiconductor (MIS) structure leads to the high Schottky gate leakage and constrains the comb-gate devices' off-state performances. The next section shows that the Schottky leakage also limits the comb-gate devices' output performances.

VI. ON-STATE PERFORMANCES OF QUASI-NORMALLY-OFF COMB-GATE ALGAN/GAN HEMTS

Due to the absence of the recess process for preparing the quasi-normally-off comb-gate HEMTs, the devices were prevented from the damages caused by dry etching on either the gate region or the access region. That could translate to the superior on-state performances and switching characteristics,

TABLE 3. Benchmark of normally-off GaN HEMTs.

Normally-off technique	Feature size ($L_{sg}/L_g/L_{gd}$ μm)	V_{th} (V)	R_{on} (Ω-mm)	Reference
Gate-recessed MIS	2/1.5/15	1.15[a]	11.6	[25] HKUST, EDL'17
	3.5/1/17	2.5[b]	20	[26] Xinguang, EDL'20
p-GaN	2/3/7	1.7[c]	14.6	[27] CGU, TED'18
	1.5/5/13.5	1.75[d]	8	[28] HKUST, EDL'19
	3/3.5/10	2.4[b]	14.9	[24] Hiwafer, EDTM'20
UTB	2/4/14	0.41[a]	10.6	[29] NCTU, ISPSD'19
	3/2/10	0.27[a]	9	[6] CAS, TED'18
Regrowth	3/1.5/10	2.19[a]	9.2	[7] HKUST, EDL'18
	4/3/10	2.3[a]	12.9	[30] Univ. Fukui, EDL'20
Stress liner	3/2/15	0.24[b]	11.9	This work

[a] at $I_d = 1$ μA/mm; [b] extracted using the extrapolation in the linear region (ELR) method;
[c] at $I_d = 1$ mA/mm; [d] at $I_d = 0.1$ mA/mm.

such as the saturation current ($I_{d,sat}$), on-resistance (R_{on}), and dynamic R_{on}.

The comb-gate device's output characteristics are compared with a p-GaN gate HEMT purchased from a commercial foundry [24], as shown in Fig. 10(a). The two devices possess similar feature sizes (L_{sg}, L_g, and L_{gd}). The comb-gate HEMT shows R_{on} of 11.9 Ω-mm, which is more superior to that of the p-GaN gate HEMT, 15.9 Ω-mm. The $I_{d,sat}$ of the comb-gate HEMT is 257 mA/mm, lower than 346 mA/mm for the p-GaN gate HEMT. The lower $I_{d,sat}$ is caused by the limited overdrive voltage V_{ov} of the comb-gate HEMT because the Schottky gate would be turned on at a higher V_g. For the same reason, the R_{on} of the comb-gate HEMTs is underestimated in performance. Table 3 presents the V_{th} and R_{on} of comb-gate devices benchmarked against other normally-off GaN HEMTs recently reported. The feature sizes are also listed for comparing R_{on} between devices. The normally-off devices using recess-free fabrication processes, such as UTB and regrowth, generally show lower R_{on}. The comb-gate devices in this work show the competitive R_{on} compared with other recess-free normally-off devices, even though the V_{th} needs further improvement.

To compare the switching characteristics of the comb-gate device and p-GaN HEMT. The dynamic R_{on} is measured using the Keysight B1505A analyzer. Fig. 10(b) shows the normalized R_{on} extracted after high voltage blocking. In the 100 ms blocking period, the devices are stressed at a specific blocking voltage, while the V_g is set to fully pinch off the devices. Subsequently, it was switched to the conducting period, and the devices are turned on with $V_d = 1$ V, $V_g = 2.5$ V for the comb-gate device and 8 V for the p-GaN device. The R_{on} is sampled 200 μs after the switching point to calculate the dynamic R_{on}. Compared with the p-GaN device showing a 37% increase in dynamic R_{on} after 200 V blocking, the comb-gate device's R_{on} increases by 20%. The lower dynamic R_{on} indicates the better switching characteristics of the comb-gate devices as a result of the recess-free fabrication processes.

Besides the off-state breakdown characteristics mentioned in Section V, the output characteristics of the comb-gate

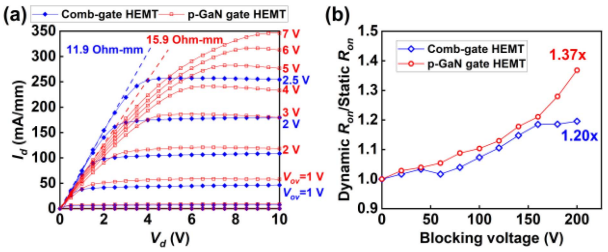

FIGURE 10. (a) Output characteristics of the comb-gate HEMT in comparison with the p-GaN gate HEMT purchased from a commercial foundry. The comb-gate HEMT and p-GaN gate HEMT were swept $V_g = 0$ to 2.5 V with a step of 0.5 V and $V_g = 0$ to 9 V with a step of 1 V, respectively. The overdrive voltage ($V_{ov} = V_g - V_{th}$) of each curve is labeled. (b) Dynamic R_{on} of the comb-gate HEMT and p-GaN gate HEMT extracted after different voltage blocking.

HEMTs, such as the $I_{d,sat}$ and R_{on}, may be improved when the gate leakage is suppressed by the introduction of other gate structures such as a MIS structure, and the devices can operate at a higher overdrive voltage V_{ov}. Furthermore, the intrinsic stress of −2 GPa is attainable for PECVD SiN_x by adjusting the deposition conditions [31], so the strained devices are expected to reach a higher V_{th} for the real-world applications.

VII. CONCLUSION

Dual-layer SiN_x liner provides external mechanical stress to the gate region of GaN HEMTs. The scaled gate dimension (0.1 μm) amplifies the stress effects, and the quasi-normally-off operation is realized. The comb-gate structure effectively suppresses the short-channel effects, including DIBL and punch-through, supported by TCAD simulation. In the absence of the recess processes for preparing devices, the quasi-normally-off comb-gate devices show superior on-state performance and switching characteristics, benchmarked against p-GaN gate HEMTs purchased from a commercial foundry. The off-state characteristics and on-state performance are still limited by the constrained overdrive voltage of the Schottky gate. The other gate structure such as the MIS gate can be implemented to suppress gate leakage, and the comb-gate HEMT with strain engineering

is believed to be a promising candidate for power electronics applications.

ACKNOWLEDGMENT

The work was conducted at CRF, SUSTech. The authors appreciated the technical support from the engineers at the facility.

REFERENCES

[1] R. Gaska *et al.*, "Electron transport in AlGaN–GaN heterostructures grown on 6H–SiC substrates," *Appl. Phys. Lett.*, vol. 72, no. 6, pp. 707–709, 1998.

[2] O. Ambacher *et al.*, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 85, no. 6, pp. 3222–3233, 1999.

[3] M. Su, C. Chen, and S. Rajan, "Prospects for the application of GaN power devices in hybrid electric vehicle drive systems," *Semicond. Sci. Technol.*, vol. 28, no. 7, 2013, Art. no. 074012.

[4] K. J. Chen *et al.*, "GaN-on-Si power technology: Devices and applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017.

[5] G. Greco, F. Iucolano, and F. Roccaforte, "Review of technology for normally-off HEMTs with p-GaN gate," *Mater. Sci. Semicond. Process.*, vol. 78, pp. 96–106, May 2018.

[6] S. Huang *et al.*, "Ultrathin-barrier AlGaN/GaN heterostructure: A recess-free technology for manufacturing high-performance GaN-on-Si power devices," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 207–214, Jan. 2018.

[7] H. Jiang, C.W. Tang, and K.M. Lau, "Enhancement-mode GaN MOS-HEMTs with recess-free barrier engineering and high-k ZrO_2 gate dielectric," *IEEE Electron Device Lett.*, vol. 39, no. 3, pp. 405–408, Mar. 2018.

[8] K. Osipov, I. Ostermay, M. Bodduluri, F. Brunner, G. Tränkle, and J. Würfl, "Local 2DEG density control in heterostructures of piezoelectric materials and its application in GaN HEMT fabrication technology," *IEEE Trans. Electron Devices*, vol. 65, no. 8, pp. 3176–3184, Aug. 2018.

[9] S. Ito *et al.*, "Mechanical stress effect of etch-stop nitride and its impact on deep submicron transistor design," in *Proc. Int. Electron Devices Meeting*, San Francisco, CA, USA, Dec. 2000, pp. 247–250.

[10] L. Xia, V. Tokranov, S. R. Oktyabrsky, and J. A. del Alamo, "Performance enhancement of p-channel InGaAs quantum-well FETs by superposition of process-induced uniaxial strain and epitaxially-grown biaxial strain," in *Proc. Int. Electron Devices Meeting*, Washington, DC, USA, Dec. 2011, pp. 1–4.

[11] N. Shigekawa and S. Sugitani, "Analysis of passivation-film-induced stress effects on electrical properties in AlGaN/GaN HEMTs," *IEICE Trans. Electron.*, vol. 93, no. 8, pp. 1212–1217, 2010.

[12] W. Cheng *et al.*, "Silicon nitride stress liner impacts on the electrical characteristics of AlGaN/GaN HEMTs," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits (EDSSC)*, Xi'an, China, Jun. 2019, pp. 1–3.

[13] W. Cheng *et al.*, "Increasing threshold voltage and reducing leakage of AlGaN/GaN HEMTs using dual-layer SiN_x stressors," *Semicond. Sci. Technol.*, vol. 35, no. 4, Apr. 2020, Art. no. 45010.

[14] W. Cheng, M. He, F. Zeng, Q. Wang, M. Chan, and H. Yu, "Quasi-normally-off AlGaN/GaN HEMTs with strained comb gate for power electronics applications," in *Proc. 4th IEEE Electron Devices Technol. Manuf. Conf. (EDTM)*, Penang, Malaysia, Apr. 2020, pp. 1–4.

[15] D. W. Gotthold, S. P. Guo, R. Birkhahn, B. Albert, D. Florescu, and B. Peres, "Time-dependent degradation of AlGaN/GaN heterostructures grown on silicon carbide," *J. Electron Mater.*, vol. 33, no. 5, pp. 408–411, 2004.

[16] K. D. Mackenzie, D. J. Johnson, M. W. DeVre, R. J. Westerman, and B. H. Reelfs, "Stress control of Si-based PECVD dielectrics," in *Proc. 207th Electrochem. Soc. Meeting*, Quebec City, QC, Canada, May 2005, pp. 148–159.

[17] A. Kranti, S. Haldar, and R.S. Gupta, "An accurate charge control model for spontaneous and piezoelectric polarization dependent two-dimensional electron gas sheet charge density of lattice-mismatched AlGaN/GaN HEMTs," *Solid-State Electron.*, vol. 46, no. 5, pp. 621–630, 2002.

[18] N. K. Subramani, "Physics-based TCAD device simulations and measurements of GaN HEMT technology for RF power amplifier applications," Ph.D. dissertation, Univ. Limoges, Brive, France, 2017.

[19] *Sentaurus Device User Guide*, Synopsys TCAD, Mountain View, CA, USA, 2016

[20] D. M. Caughey and R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proc. IEEE*, vol. 55, no. 12, pp. 2192–2193, Dec. 1967.

[21] "State of the art 2D and 3D process and device simulation of GaN-based devices," in *Simulation Standard*, vol. 23, Silvaco Inc., Santa Clara, CA, USA, Jul.–Sep. 2013, pp. 1–11.

[22] K. Shinohara *et al.*, "Scaling of GaN HEMTs and Schottky diodes for submillimeter-wave MMIC applications," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 2982–2996, Oct. 2013.

[23] M. J. Uren *et al.*, "Punch-through in short-channel AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 395–398, Feb. 2006.

[24] F. Zeng *et al.*, "Study on the optimization of off-state breakdown performance of p-GaN HEMTs," in *Proc. Electron Devices Technol. Manuf. Conf. (EDTM)*, Penang, Malaysia, Apr. 2020, pp. 1–4.

[25] M. Hua *et al.*, "Normally-off LPCVD-SiN_x/GaN MIS-FET with crystalline oxidation interlayer," *IEEE Electron Device Lett.*, vol. 38, no. 7, pp. 929–932, Jul. 2017.

[26] Z. Sun *et al.*, "Improving performances of enhancement-mode AlGaN/GaN MIS-HEMTs on 6-inch si substrate utilizing $SiON/Al_2O_3$ stack dielectrics," *IEEE Electron Device Lett.*, vol. 41, no. 1, pp. 135–138, Jan. 2020.

[27] H. Chiu *et al.*, "High uniformity normally-OFF p-GaN gate HEMT using self-terminated digital etching technique," *IEEE Trans.Electron Devices*, vol. 65, no. 11, pp. 4820–4825, Nov. 2018.

[28] H. Jiang, R. Zhu, Q. Lyu, and K.M. Lau, "High-voltage p-GaN HEMTs with off-state blocking capability after gate breakdown," *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 530–533, Apr. 2019.

[29] P. Han, Z. Yan, C. Wu, E. Y. Chang, and Y. Ho, "Recess-free normally-off GaN MIS-HEMT fabricated on ultra-thin-barrier AlGaN/GaN heterostructure," in *Proc. 31st Int. Symp. Power Semicond. Devices ICs (ISPSD)*, Shanghai, China, May 2019, pp. 427–430.

[30] J. T. Asubar, S. Kawabata, H. Tokuda, A. Yamamoto, and M. Kuzuhara, "Enhancement-mode AlGaN/GaN MIS-HEMTs with high V_{TH} and high I_{dmax} using recessed-structure with regrown AlGaN barrier," *IEEE Electron Device Lett.*, vol. 41, no. 5, pp. 693–696, May 2020.

[31] M. Besland, M. Lapeyrade, F. Delmotte, and G. Hollinger, "Interpretation of stress variation in silicon nitride films deposited by electron cyclotron resonance plasma," *J. Vac. Sci. Technol. A, Vac.*, vol. 22, no. 5, pp. 1962–1970, 2004.