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Printable Low Power Organic Transistor Technology for Customizable Hybrid Integration Towards Internet of Everything

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ABSTRACT A highly customizable hybrid sensor system, composed of a silicon integrated circuit (IC) chip and an organic field effect transistor (OFET) transducer, is proposed for Internet of Everything (IoE). In such a system, the silicon IC chip performs high performance and complex signal processing, and the OFET transducer provides flexible or conformable large area coverage and more friendly interfaces to integrate different sensing materials. A low trap-state density OFET (LTDOFET) technology is developed for such a hybrid system, owning features of low-cost solution printing processes, low operation voltage and excellent operational stability. This technology has been implemented with various materials and processes, indicating its generality. Several sensor applications built based on this device technology are also reviewed, proving the LTDOFET technology would be promising for highly customizable sensor systems towards the IoE era.

INDEX TERMS Internet of Everything, flexible hybrid integration, sensor integration, organic field effect transistor, printed electronics.

I. INTRODUCTION

Internet of Everything (IoE) aims to extend Internet connectivity beyond standard electronic devices, such as computers, smartphones and tablets, to any range of everyday objects [1]. The status or activities of these objects can then be sensed or monitored, to generate valued information for remote control, friendly interactivity, quality inspection, real-time diagnosis, or early risk warning.

To realize that, sensor systems need to be customized to fit diverse types of everyday objects. In addition to the basic functions, there would be more severe requirements in terms of cost, power, design-to-product time, and form factor.

A common approach for short design-to-product time is through packaging the sensors with the readout and control electronics in a printed circuit board (PCB) [2]. However, such systems are difficult to address the requirements of cost, form factor and power, though a certain flexibility can be achieved by assembling components on a flexible PCB [3], [4].

To aggressively minimize the system dimension and power, heterogenous integration of the sensors with application specific integrated circuits (ASICs) can be implemented, benefiting wearable and implantable applications [5]. This type of approaches, however, suffers long design-to-product time and high non-recurring cost.

On the other hand, organic, oxide and nanostructured functional materials have been widely studied to construct various physical and chemical sensors by utilizing their electrical, optoelectronic, or mechanical properties [6], [7]. Sensors using these materials are able to be made on arbitrary

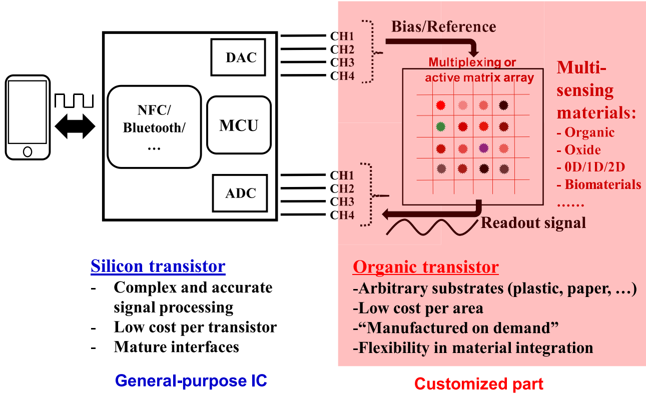

FIGURE 1. **Schematic of the hybrid system architecture composed of the silicon transistor IC, and the organic transistor transducer.**

flexible substrates with low temperature and solution printing processes. Such technology routes would enable ease of customization for diverse sensing functions at low cost and with conformal coverage on non-planar object surfaces. However, most of these reported sensors used custom-designed PCB circuit board for signal readout and processing, which put constraints of the form factor, and cost of the overall systems [8], [9].

To implement signal processing electronics, there have also been tremendous efforts on developing thin-film transistor (TFT) circuits using similar low temperature processes in organic, oxide, 1D/2D nanostructure semiconductors [10], [11], [12], [13]. By integrating all the required electronics based on TFTs and the sensors, simple "stand-alone" flexible sensor systems without silicon IC chips have been demonstrated as a potential solution for lower cost and shorter design-to-product time [14], [15], [16], [17].

Despite of advantages in large area electronics applications, TFTs are of larger feature size, lower device performance, and less maturity in manufacturing and design for high integration density compared to the silicon FET technology. Thus, the circuit complexity, performance and power that can be achieved are far behind than what the silicon ICs do.

To combine the strengths of both flexible sensor technologies and the silicon ICs, an emerging approach, so called flexible hybrid integration (FHI), is to mount IC chips or dies onto the same flexible substrate with the sensors using flexible or stretchable interconnects for electrical connections [18]. The IC performs sensor signal acquisition and conditioning, data processing and transmission through standard interfaces This technology has been used to build various flexible or stretchable sensor systems for smart packaging and wearable health monitoring applications [19], [20]. In the systems, the IC needs to accommodate specific analog interfaces to match the sensor outputs. It would be technically challenging and also costly to design an ASIC for supporting various kinds of sensor outputs. Moreover, output signals from the passive sensors need to pass through relatively long interconnects before going into the readout IC, resulting in poor noise immunity.

This article introduces a more versatile FHI system solution using the organic FET (OFET) technology. The advantages of such an OFET based FHI system will be firstly discussed, followed by a summary of its performance requirements for OFETs. After a complete review of various techniques for low voltage OFETs, the developed low trap density OFET (LTDPFET) technology is described in details. It is shown that the LDTPOFET is a promising technology for developing printed low power transistors to meet the requirements of FHI in terms of steep subthreshold swing, stability and processability. Examples of using this device technology for different sensors are further reviewed, proving its versatility of transducing various kinds of sensed signals.

II. HYBRID SYSTEM AND DEVICE REQUIREMENT

The proposed hybrid sensor system combing a silicon ASIC and an OFET sensor circuitry is illustrated in Fig. 1. With a stack of organic semiconductor (OSC) and polymer dielectric materials, the OFET is able to be manufactured at low temperature on arbitrary substrates over large area via low cost solution printing approaches [21], [22]. It also owns the advantage of excellent intrinsic mechanical flexibility compared to inorganic counterparts. With molecule tailoring or physical mixing of OSCs, there is great room for continuous device performance improvement [23]. Therefore, the OFET part in the system is able to provide flexible or conformable large area coverage and more friendly interfaces to integrate different sensing materials.

In principle, with proper device structure and circuit design, the OFET circuitry can convert any kinds of sensed signals to a standard output signal, which is then read out using a general-purpose ASIC with common analog interfaces. In such systems, the ASIC performs sensor signal acquisition and conditioning, data processing and transmission through standard interfaces, while the sensing functions, form factor, and substrate of the sensors and interconnects being customized according to the specific requirements. It would be able to provide an economic solution for diverse customized sensor applications. Moreover, since the sensed signal is transduced and amplified locally, the influence of external noise during the signal transmission will be suppressed. With the OFET multiplexing circuitry, sensor arrays can also be constructed with a limited number of interfaces at the readout ASIC. The integration of the ASIC and the OFET circuitry with sensors could be realized in two ways: bonding the OFET sensor circuitry onto a flexible PCB composed of the packaged ASICs, or bonding ASIC dies directly onto the OFET circuitry substrate.

Most of such FHI systems are targeted for IoE applications, and are normally powered by a minimized battery or wireless radio frequency power with severe power constraints. This poses a stringent requirement on the operation voltage of the OFET circuitry, which, however, is normally large (i.e., a few tens volts or even more than a hundred volts)

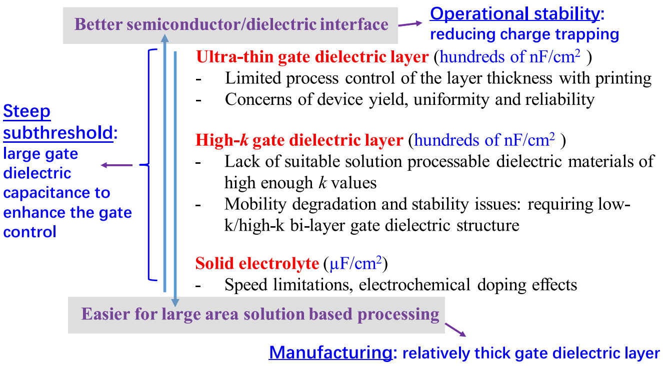

FIGURE 2. Illustration of the trade-off among steep subthreshold swing, operational stability and manufacturing for low voltage OFETs using the conventional approach of enlarging the gate capacitance.

for OFETs. There has been tremendous effort being devoted to different approaches of decreasing the subthreshold swing of OFETs for low operation voltage. These approaches are based on the same principle as that for Si-FETs by using an ultra-thin gate insulator (GI) layer or a high-*k* GI layer to enlarge the gate capacitance [24]–[26].

Since OFETs have much larger area coverage with low temperature solution-based processes, the way of using ultra-thin GI layers is not applicable. The GI layer needs to be certainly thick (at least a few hundred nanometers) for good enough device reliability and yield. High-*k* dielectric or solid electrolytes could be potential solutions for realizing low voltage OFETs based on thick GI layers [27]–[30]. However, the induced localized dipole electric field by polarization in high-*k* dielectric might be unfavorable for carrier transport due to the broadening of the trap-state density at the OSC/GI interface [31]. Most of high-*k* dielectrics used for low voltage OFETs are still inorganic materials, and there is lack of choices for low temperature solution processable high-*k* polymer dielectric materials [24]–[26]. The solid polymer electrolyte, which is made by blending ionic liquids with a gelating triblock copolymer to form a physically cross-linked network, can provide very large specific capacitance up to several μF/cm^2 at low frequency with micrometer level thickness [29]. However, it suffers slow operation speed and the induced electrochemical doping of the channel with ion moving under electrical field might cause reliability issues.

Therefore, as summarized in Fig. 2, with only enlarging the gate dielectric capacitance for steep subthreshold properties, those approaches are not able to meet both requirements of large area solution processability and operational stability. The former needs a thick enough GI layer, while the latter depending low charge trapping interface between the OSC and GI layers.

III. DEVICE TECHNOLOGY

To address the above issue, a new approach to realize low voltage OFETs by reducing the sub-gap trap-state density at the channel interface was proposed [32]. With this approach, low voltage OFETs can be fabricated without strict requirements of the gate dielectric layer, and also exhibit excellent

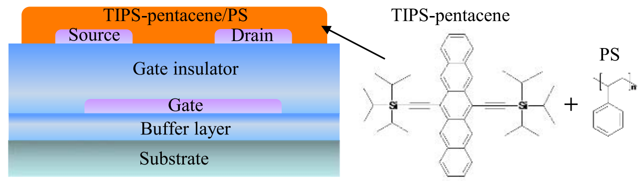

FIGURE 3. Illustration of the bottom-gate bottom-contact structure for realizing the low trap-state density OFET (LTDOFET) with a blended solution of small organic semiconductor (TIPS-pentacene) and insulating polymer binder (PS).

operational stability [33], [34]. So-called low trap-state density OFET (LTDOFET) has been implemented with various OSC and gate dielectric materials using different solution-based processes [32], [34], [35]–[40]. The features of low operation voltage and excellent operational stability with a solution printable structure make this device a promising technology of choice for constructing the proposed FHI system in Fig. 1.

A. BASIC PRINCIPLE

The required operation voltage for a FET is determined by its subthreshold swing (SS). For OFETs, SS can be expressed as [41]:

$$SS = ln10 \cdot \frac{k_B T}{q} \cdot \left(1 + \frac{q^2 N_{ss}}{C_G}\right) \tag{1}$$

where k_B is the Boltzmann's constant, T is the absolute temperature, q is the elementary charge, N_{ss} is sub-gap trap-state density at the channel interface and C_G is the gate dielectric capacitance per unit area.

Based on equation (1), it can be seen that, instead of enlarging C_G, reducing N_{ss} is also possible for realizing lower voltage OFETs. In normal OFETs, the presence of large sub-gap trap-state density at the channel interface causes poor gate modulation efficiency and thus large SS values.

Our earliest work showed that, with a bottom-gate bottom-contact structure (Fig. 3), by depositing a blended solution of small organic semiconductor (TIPS-pentacene) and insulating polymer binder (PS) onto a polymer GI surface, crystallization of TIPS-pentacene was able to be well controlled to obtain a low trap-state density channel. As a result, low voltage OFETs with steep SS of about 100 mV/dec was obtained at an about 400 nm thick polyvinyl alcohol (PVA) GI layer (i.e., gate capacitance of about 12 nF/cm^2) [32]. With the conventional approaches, to achieve the similar level of SS, the gate capacitance needs to be of several hundred nF/cm^2 [27], [42].

B. DIFFERENT MATERIALS AND PROCESSES

The LTDOFET has been verified by several research groups based on different OSC and GI materials using various processing techniques, as summarized in Table 1 [37], [38], [40].

TABLE 1. Summary of the LTDOFET with different OSCs and GI materials using various processing techniques.

Work	OSC/Process	GI/Capacitance (nF/cm²)	Mobility (cm²V⁻¹s⁻¹)	SS (mV/dec)
[32]	TIPS-pentacene/spin-coating	PVA/12.2	1	100
[33]	TIPS-pentacene/drop-casting	SU8/2.9	0.4	250
[34]	TIPS-pentacene/ink-jet printing	PVCN/10.2	0.6	97
[35]	TIPS-pentacene/drop-casting	PLC/6.3	1.2	170
[36]	TIPS-pentacene/drop-casting	PVCN/P(VDF-TrFE-CFE) /46.3	0.25	73
[37]	DTBDT-C_6/ dispensing	Parylene 24	0.8	100
[38]	Ph-BTBT-10/spin-coating	PS/SiO_2 25	3.8	102
[39]	TIPS-pentacene/ink-jet printing	PVP 37	0.26	155
[40]	C_8-BTBT/ink jet printing	PVCN 13.3	/	60.2
[43]	TIPS-pentacene/flexible-blade coating	PVCN 8.6	0.37	140
[44]	TIPS-pentacene/soft-contact coating	PVCN/ES2110 5	0.89	87

It can be seen that, with TIPS-pentacene/PS being deposited by different processing techniques including spin-coating [32], drop-casting [33], [35], [36], blade-coating [43], [44] and inkjet printing [34], [39], similar low trap-state density channels were able to be obtained for steep subthreshold OFETs at small gate capacitance.

This method also enables using various popular low-*k* polymer dielectric materials with a relatively thick layer to realize printable low voltage OFETs [32]–[36], [39], [43], [44]. The measured transfer characteristics ($I_D - V_{GS}$) of OFETs using a poly (vinly cinnamate) (PVCN) GI layer (~300 nm) and a SU-8 GI layer (~1.1 µm) are shown in Fig. 4(a). Even at such a micrometer thick SU8 GI (i.e., gate capacitance of about 3 nF/cm^2), the device can still be switched between ON and OFF states with a small voltage swing [33].

To further reduce the SS of the OFET for lower voltage operation, a low-*k*/high-*k* bilayer structure GI was used [36]. In the structure, the high-*k* P(VDF-TrFE-CFE) layer helps to enlarge the gate capacitance without needs of decreasing the layer thickness, while the low-*k* PVCN layer on top providing a smooth and low polar surface for forming a high-quality OSC channel. The measured $I_D - V_{GS}$ curve of the device is also given in Fig. 4(a) for comparison. With a total thickness of about 360 nm, steep *SS* as small as 64 mV/decade was able to be achieved [36]. The *SS* value versus the gate capacitance for the fabricated OFETs using different polymer dielectric materials is compared in Fig. 4(c) [46]. It can be seen that low voltage OFETs via the LDTOFET technology, using different GI materials, exhibit a similar level of N_{ss}, which is one to two order less than that of previous work [24], [27], [47], [48]. Combining the low-*k*/high-*k* bilayer GI, the LTDOFET technology offers greater room for optimal design of low power OFETs.

Instead of TIPS-pentacene, other OSC materials were also used to implement LTDOFETs [37], [38], [40]. It was found that, with C_8BTBT having better crystallization, low power OFETs of steeper SS were fabricated [40]. By using highly ordered smectic-E liquid crystalline phase of Ph-BTBT-10, LTDOFETs were obtained for both steep SS and also higher mobility (>3 cm^2·V^{-1}·s^{-1}) [38]. The results prove generality

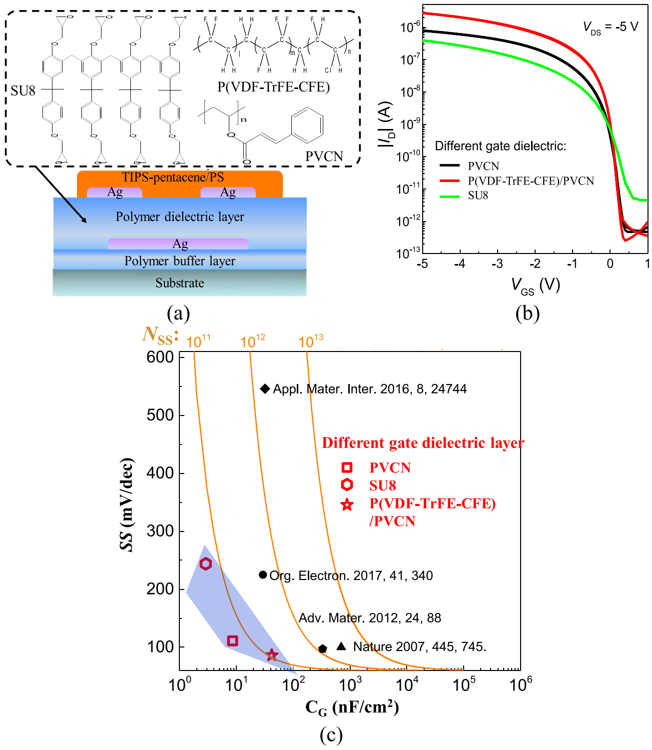

FIGURE 4. (a) The bottom-gate bottom-contact OFET structure using inkjet printed Ag electrodes and various GI materials (PVCN, SU8 and P(VDF-TrFE-CFE)/PVCN bilayer). (b) The measured transfer characteristics ($I_D - V_{GS}$) of OFETs using a PVCN gate dielectric layer (~300 nm), a SU8 gate dielectric layer (~1.1 µm), and a P(VDF-TrFE-CFE)/PVCN bilayer (~360 nm). (c) Comparison of the *SS* value versus the gate dielectric capacitance (C_G) for the LTFOFETs using different polymer dielectric materials with previous work.

of the technology for various OSCs, and also indicate the potential of continuous performance improvement.

C. OPERATIONAL STABILITY

For sensor circuitry application, long term bias stress stability is important. To achieve good stability under electrical bias stress, reducing the charge trapping probability is needed. The charge trapping probability may depend on the trap-state density at the interface, and the electric field perpendicular to the channel. Within a LTDOFET, the trap-state density at the channel interface is minimized. Low voltage operation with a relatively thick GI layer results in weak gate induced electrical field perpendicular to the channel. Choosing air stable and water repellent organic semiconductor and dielectric materials can help to suppress influence from the ambient for long term storage stability [34]. As a result, the LTDOFET can well address the tradeoff issue between steep SS and stability for printable OFETs. As an example, in Fig. 5(b), the measured $I_D - V_{GS}$ characteristics of the LTDOFET using P(VDF-TrFE-CFE)/PVCN bilayer GI shows negligible change under continuous negative gate bias stress for 5000 s [45]. The drain current for the device being continuously operated near threshold also remains nearly constant over time after initial stabilization (Fig. 5(c)). Moreover, the

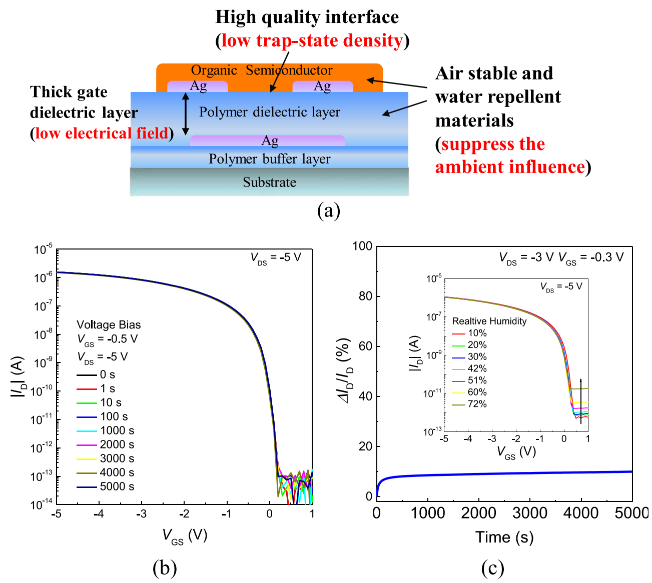

FIGURE 5. (a) Illustration of the mechanisms for the LTDOFET to achieve stable electrical characteristics. (b) The measured transfer characteristics of the LTDOFET with P(VDF-TrFE-CFE)/PVCN gate dielectric layer under continuous negative gate bias stress ($V_{DS} = -0.5$ V, $V_{GS} = -5$ V) for 5000 s. (c) The drain current evolution over time for the OFET being operated near the threshold under continuous voltage bias ($V_{DS} = -3$ V, $V_{GS} = -0.3$ V). Inset shows the influence of humidity on the electrical characteristics [45].

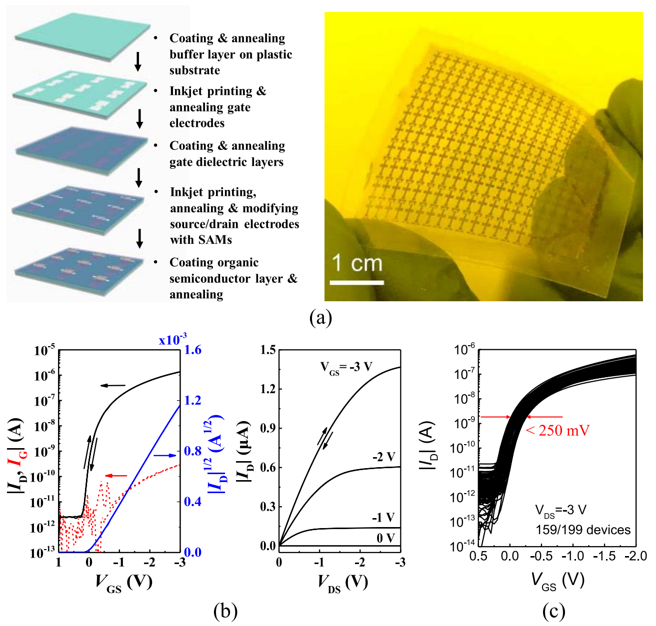

FIGURE 6. (a) Fabrication processes of the LTDOFETs and photo image of the fabricated devices on a 5 cm × 5 cm plastic substrate. (b) The measured typical transfer ($I_D - V_{GS}$) and output ($I_D - V_{DS}$) characteristics. (c) The measured $I_D - V_{GS}$ curves of 159 devices [44].

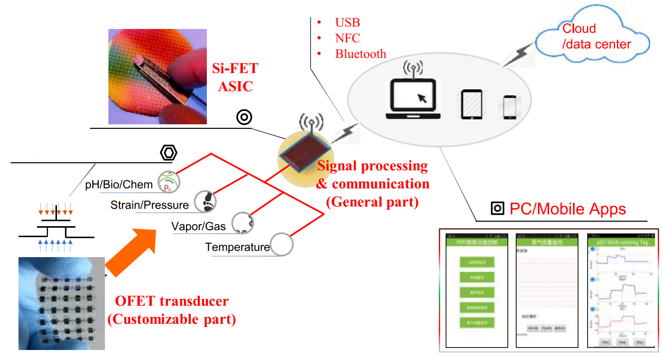

FIGURE 7. Illustration of the highly customizable hybrid sensor system is able to be built with integration of the OFET transducer and the Si-FET chip.

device presents reasonably stable electrical characteristics under a wide range of humidity change [45].

D. PROCESSING SCALABILITY

High throughput manufacturing in terms of short processing time over large area is important for cost reduction. In the LTDOFET, the GI and the electrode layers can be deposited with high throughput using industry available processes. Deposition of the OSC layer over large area in short processing time with well controlled crystallization for low trap-state density is thus vital. Spin-coating, drop-casting, inkjet printing and simple blade-coating have been used in the past to verify the device concept [32], [34]–[36], [39], [43]. However, they are difficult for achieving high throughput and large area manufacturing with uniform crystallization. For spin-coating, although it is the most popular solution based process, large material waste is a serious issue.

A soft-contact coating approach has recently been developed for OSC deposition, using a rotatable steel sheet as the meniscus guide [44]. During the coating process, the meniscus guide maintains very weak contact force to the substrate surface, avoiding damages to the pre-fabricated electrodes. A "manufacturing-on-demand" mask-free process combing inkjet printing Ag electrodes was developed to fabricate OFETs on plastic substrate (Fig. 6(a)). Even at a fast coating speed of 20 mm/s, well controlled crystallization can be achieved to form low trap-state density channels for low voltage operation. As shown in Fig. 6(b) and (c), the fabricated devices exhibit mobility reaching 1.5 $cm^2 \cdot V^{-1} \cdot s^{-1}$, and good uniformity with a small threshold voltage dispersion less than 250 mV for measured 159 devices [44].

IV. SENSOR APPLICATIONS

In principle, the OFET can work for transducing various kinds of sensor signals to a standard electrical output with proper design of the integration structure and circuitry. Therefore, a highly customizable hybrid sensor system is able to be built with integration of the OFET transducer and the Si-FET chip, as depicted in Fig. 7. This printable low voltage and stable LTDOFET technology fits well with the requirements for such an integration architecture. In recent years, this device technology has been used for making various sensors to detect bio-chemical, gas, pressure and electrophysiological signals, respectively, as shown in Fig. 8 [34], [40], [49], [50].

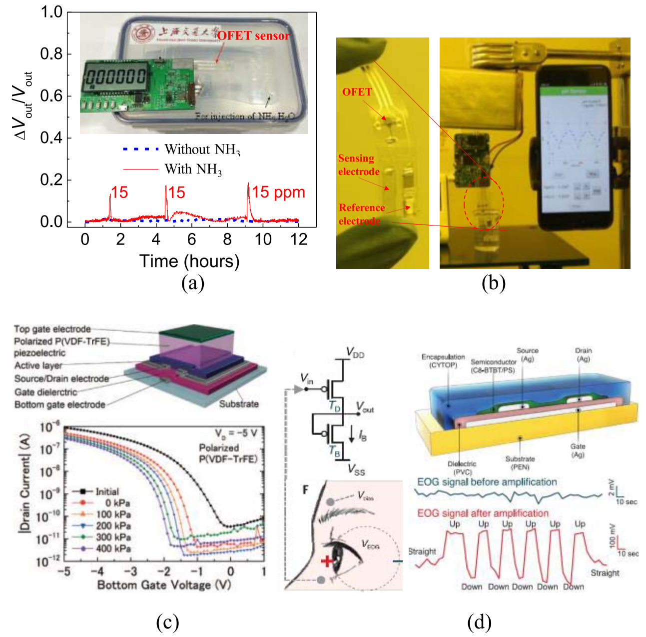

FIGURE 8. **Various sensors being built based on the LTDOFET technology: (a) ammonia (NH_3) sensor [34], (b) H^+ sensor [49], (c) pressure sensor [50] and (d) electro-oculogram (EOG) sensor [40].**

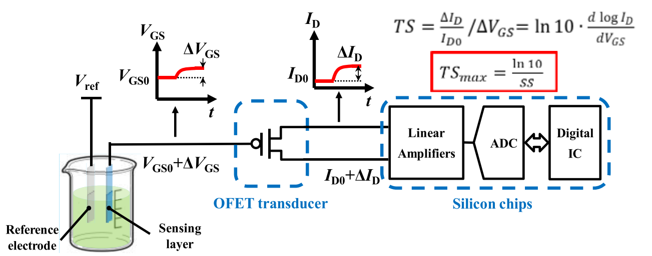

FIGURE 9. **Illustration of the transduction sensitivity (TS_{max}) of the hybrid sensor system, taking the ion sensing as example.**

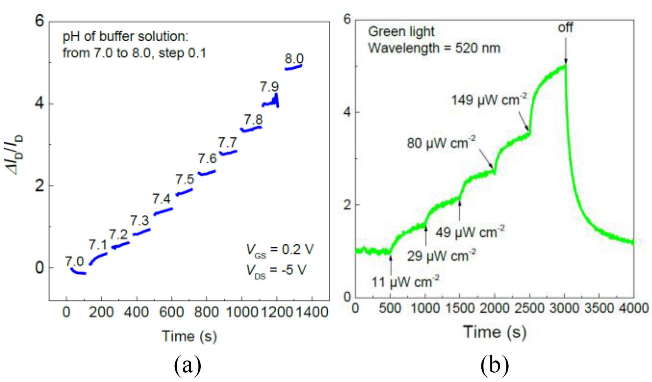

FIGURE 10. **(a) The measured relatively drain current change of LTDOFET based ion sensor with the pH value of the buffer solutions ranging from 7.0 to 8.0. (b) The transient response upon illumination of gradually increased intensity for the LTDOFET photo sensor [45].**

In the sensor system, low voltage OFETs with steep SS can bring benefits of not only ultra-low power operation but also high sensitivity to weak signal changes. As shown in Fig. 9, the maximum transduction sensitivity (TS_{max}) occurs in the subthreshold regime and is proportional to the inverse of SS [51]. Being biased in the subthreshold regime, the OFET was shown to be able to detect not only small ion concentration change and but also weak green fluorescent light signal (Fig. 10) [45]. These ion and fluorescence sensing properties will be important for rapid diagnostic analysis in bio- and chemical applications.

V. CONCLUSION

The developed LTDOFET technology and its sensor applications are reviewed. With this technology, low voltage OFETs are realized by reducing the sub-gap trap-state density at the channel interface. A low-cost solution printing process is able to be developed for high throughput manufacturing of the devices. This LTDOFET technology has been implemented with various materials and solution processes, and used for constructing bio-chemical, gas, pressure, electrophysiological and photo sensors. The core competitiveness of the technology would include: 1) being highly customizable for reducing the short design-to-product time; 2) low cost manufacturing and ease of being scaled up; 3) convenience for sensor material integration; 4) steep subthreshold characteristics for low operation voltage and high sensitivity. These features make this device a promising technology of choice for highly customizable hybrid sensor systems towards the IoE era. For further development, the driving current of this device needs to be improved, by adopting high mobility small molecule OSC materials and decreasing the contact resistance.

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