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Indium Silicon Oxide TFT Fully Photolithographically Processed for Circuit Integration

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ABSTRACT A new class of amorphous oxide semiconductors based on InO_x doped with Ti, W or Si seems to show great promise for large area, flexible, electronics. Of particular interest is the In_2O_3:SiO_2 system as it has a relatively large bond dissociation energy, hence highly suited for long-term environmental stability. In this paper, we present a sub-200°C fully photolithographically-processed indium oxide thin film transistor that is fully compatible to circuit integration on plastic substrates. The TFTs typically showed a mobility of 5 cm^2/Vs, a threshold voltage of -0.16 V and a subthreshold swing of 312 mV/dec. We report on its stability behavior when subject to electrical bias stress and negative bias illumination stress, along with a pulse-based compensation solution for persistent photoconductivity arising from the latter. Following static characterization and subsequent parameter extraction of the indium silicon oxide TFT, design considerations are presented along with measurement results of a fully integrated TFT voltage amplifier with high impedance subthreshold loading.

INDEX TERMS In-Si-O, thin film transistor, threshold voltage shift, NBIS.

I. INTRODUCTION

A morphous oxide semiconductors (AOS) are attractive in view of their large bandgap energy which gives rise to optical transparency, and more importantly, this family of materials can be layered on a wide range of substrates, including plastic or paper, in view of their low temperature attributes. In particular, thin film transistors (TFTs) based on AOS allow for sub-200°C process flows and show excellent large area uniformity and mobilities much higher than the amorphous silicon counterparts [1]–[4], along with a leakage (or OFF-state) current that is in the range of sub-fA. In the family of amorphous oxide semiconductors, the amorphous indium oxide group shows great promise as high performance materials. These include InO_x, IGZO, InSnO, InAlO, and InWO [5]–[9], and very importantly, IGZO is already deployed in large screen display products. Recently, Aikawa *et al.* [9] and Kizu *et al.* [10] reported a new class of materials based InO_x doped with Ti, W or Si. Of particular interest is In_2O_3:SiO_2 (ISO) [11] in view of the relatively large bond dissociation energy of Si-O, which constitutes an important requirement for environmentally stable TFTs. The silicon cations in the ISO film suppress the instability originating from the oxygen vacancy-related defects in conventional metal oxides. The high dissociation energy of the silicon-oxygen bond improves retention of oxygen atoms in the film, thus making the semiconductor more stable. In terms of comparison with current state-of-the-art 2D materials based TFT [12], [13], the technology presented here is highly scalable to very large sizes, and for purposes of process compatibility, we have realized a fully photolithographic fabrication process making the technology amenable for circuit integration as well as large-scale on-panel system integrations.

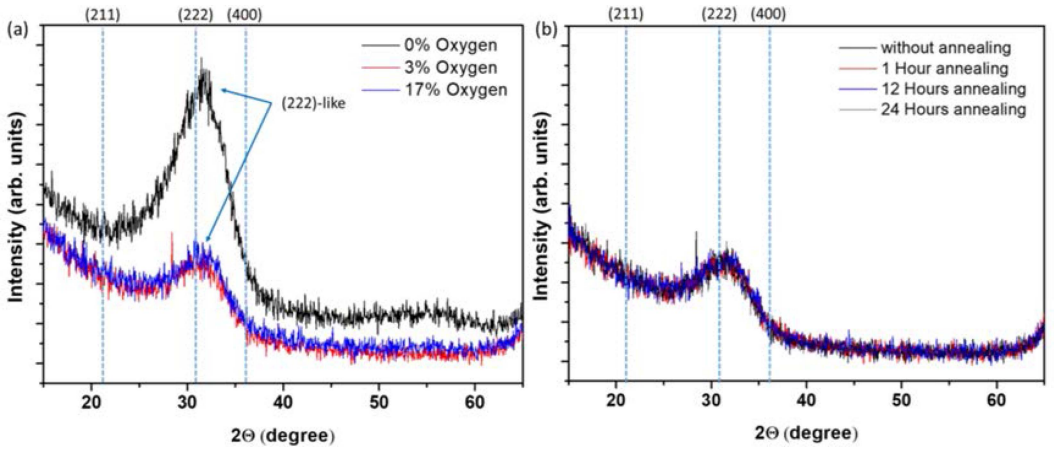

FIGURE 1. XRD data of the (a) as-deposited ISO films with different oxygen flow rate ratios and (b) 3% oxygen films under different annealing conditions.

In this work, we extend our previous work reported in [14], providing a systematic account of the material attributes and process integration considerations pertinent to ISO TFTs. We present ISO TFTs fabricated using an all-photolithographic process at a maximum temperature of 200°C, in which the ISO is deposited by DC sputtering and the dielectric layers by atomic layer deposition. By varying the silicon oxide content, field-effect mobility could be regulated from 5 cm^2/Vs to 30 cm^2/Vs. It is shown that changing the argon/oxygen ratio during sputtering could be used to tune mobility, threshold voltage, and subthreshold swing for a reasonably broad range. The TFTs were subject to both electrical bias stress and negative bias illumination stress (NBIS) stability and a compensation solution based on a positive gate pulse technique is presented to deal with persistent photoconductivity. Following parameter extraction of the fabricated TFTs, design considerations for circuit integration are presented along with results for a fully integrated ISO TFT voltage amplifier.

II. INDIUM SILICON OXIDE

The ISO thin films were grown on a Si substrate using radio frequency (RF) sputtering employing a 90% In_2O_3 and 10% SiO_2 ceramic target. The RF power of the electron guns was 150 W, and the ISO films were sputtered in a 4 mTorr atmosphere. The O_2:(O_2 + Ar) flow rate ratio varied from 0% to 17%. During the sputtering, the ISO target was constantly moving/rotating to obtain uniformly coated films. By varying the deposition time, the film thickness obtained was 100nm. Prior to the deposition, the Si substrates were cleaned in an ultrasonic cleaner with de-ionized water, acetone, and isopropyl alcohol. Three different deposition conditions, namely three oxygen flow rate ratios were used to fabricate samples for the XRD measurements: 0%, 3%, and 17%. The samples were diced into 12 smaller pieces so that the effect of annealing conditions could be investigated as well. Four different annealing durations at 150°C was considered: zero-time, one-hour, 12 hours, and 24 hours. The annealing used an IKA hot plate (metal plate) under atmospheric conditions. The temperature uniformity and stability of the hot plate were verified with a thermometer.

XRD measurements were conducted at the Faculty of Sciences and Technology, UNINOVA, Lisbon, Portugal. The equipment used was a PANalytical X'Pert PRO with Cu Kα radiation (λ = 1.540598 Å). Fig. 1 (a) compares the XRD data of the as-deposited ISO films for the different oxygen flow rate ratios. Peaks at 31.3° were found in all films. According to the Joint Committee on Powder Diffraction Standards (JCPDS), 21.5° (211), 30.6° (222), and 35.5° (400) were assigned to the XRD 2θ peaks of the cubic phase, c-In_2O_3. Here, 31.3° is classified as a (222)-like peak. The (222) peak is asymmetric and broad, due to an overlap of two adjacent peaks or inhomogeneous strain. Compared with the 0% oxygen as-deposited sample, the 3% and 17% oxygen as-deposited samples had much weaker (222)-like peaks. Fig. 1(b) shows the XRD data of the 3% oxygen ISO films under different annealing conditions. Similar trends were also found in the 0% and 17% annealing experiments. Thus, results show that the 150°C annealing did not cause any crystallization changes in the ISO film.

Based on the XRD data, when there was no oxygen in the chamber during deposition, a very small amount of the polycrystalline ISO was found in the deposited film. Feeding oxygen into the chamber seems to effectively reduce the degree polycrystallinity in the film. The 3% and 17% oxygen ratio deposited ISO was amorphous with and without 150°C annealing.

With the band structure unknown, both allowed indirect and allowed direct transitions of the electrons were considered. Fig. 2 (a) shows the allowed indirect transition Tauc plot. The optical bandgap of the 0%, 3%, and 17% oxygen samples were 1.23eV, 1.97eV, and 1.97eV, respectively. In terms of the allowed direct transition scenario, the Tauc plot is shown in Fig. 2 (b). The optical bandgap of the 0%, 3%, and 17% oxygen samples were 2.83eV, 3.55eV, and 3.55eV, respectively.

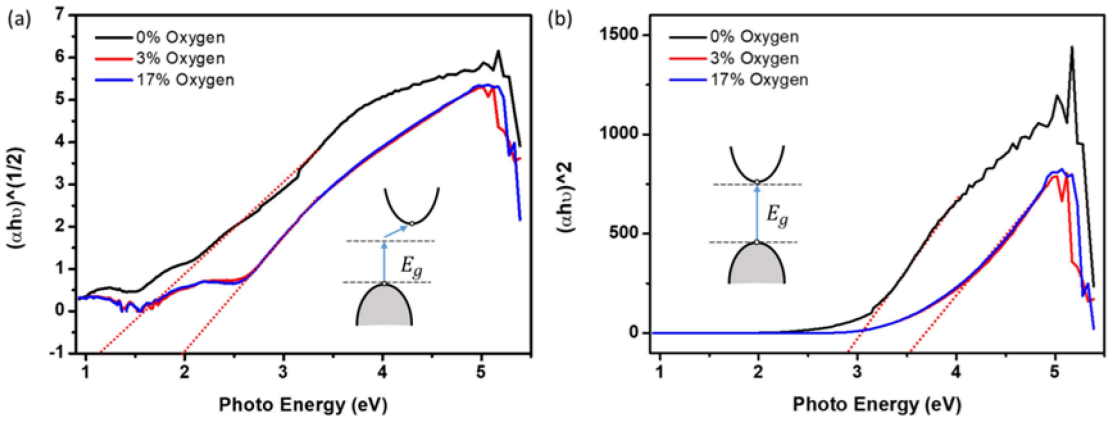

FIGURE 2. Tauc plot of the ISO film indicating transition types that are (a) allowed indirect and (b) allowed direct.

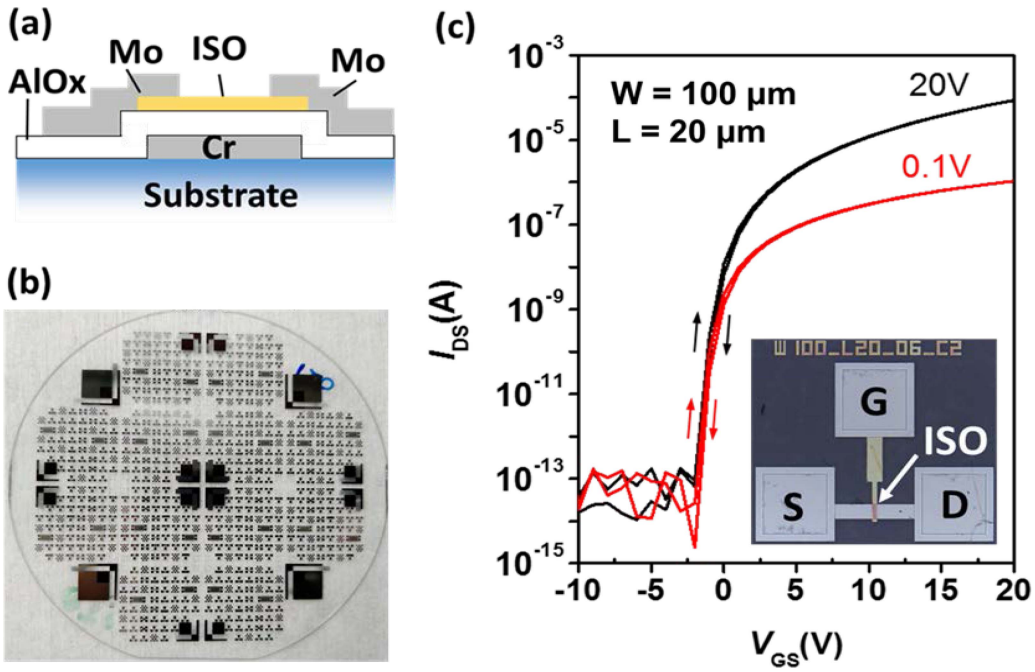

FIGURE 3. (a) Cross-sectional view of the ISO TFT structure, (b) ISO TFT array on a 3-inch glass substrate using fully photolithographic processes, (c) typical transfer characteristics of ISO TFTs, insert depicts the top-view of the measured TFT.

Taking the 3% oxygen sample as an example, its electronic bandgap would likely fall between the allowed direct and indirect transition scenarios, which is [1.97eV, 3.55eV]. Previous reports have suggested that the conventional energy band dispersion model for metal oxides was applicable to the ISO, and that the allowed transitions can be assumed to be direct, although density functional theory (DFT) simulations are needed to give a more accurate band structure.

III. INDIUM SILICON OXIDE TFTS

A. THIN FILM TRANSISTOR FABRICATION

As shown in Fig. 3(a), the bottom-gate top-contact structure was used in the ISO TFT using a fully photolithographic processes. The ISO TFT array was fabricated on a 3-inch Borofloat33 glass substrate, which is shown in Fig. 3 (b). First, a 100 nm Cr film was sputtered onto the glass substrate, and the Cr layer was subsequently etched to form the gate electrode. A 120 nm AlO_x layer was then deposited on top of the Cr at 200°C using atomic layer deposition (ALD). Without breaking the vacuum, a 10 nm ISO layer was deposited by RF-sputtering at room temperature in a different chamber as integral part of a cluster tool. The sample was then etched with buffered hydrogen fluoride and hydrogen chloride to form via holes and semiconductor regions, respectively. Finally, a 100 nm Mo layer was deposited and patterned by reactive-ion etching to form the source and drain electrodes. The sample was annealed at 150°C for 12 hours in ambient air prior to the measurements. Typical transfer characteristics are shown in Fig. 3(c). The TFT exhibited a mobility of 5 cm^2/V-s, a threshold voltage of -0.16 V, and

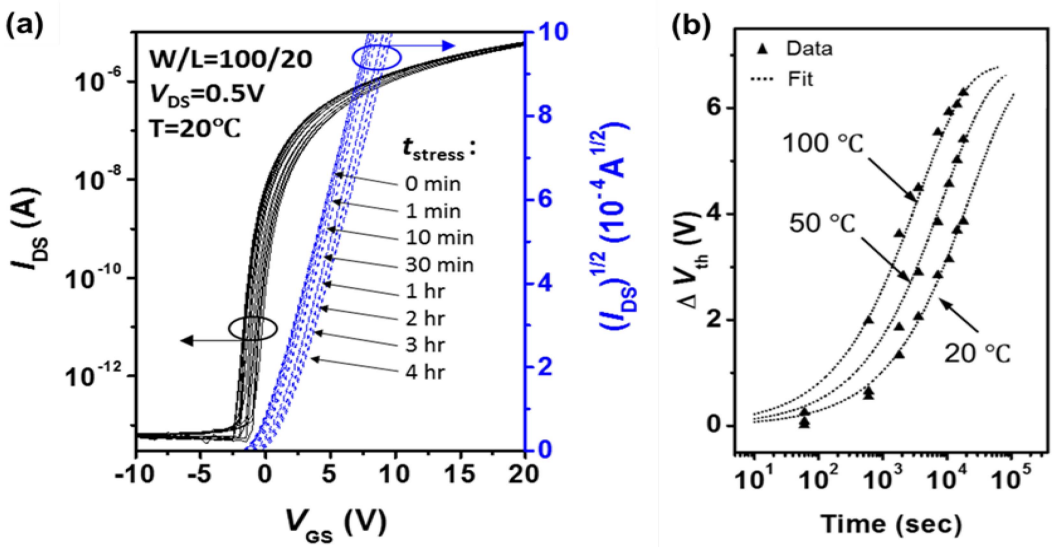

FIGURE 4. (a) Evolution of transfer characteristics of the ISO TFT under bias stress (V_{GS} = 20 V; V_{DS} = 0.5 V) at 20°C, and (b) threshold voltage shift versus stress time.

a subthreshold swing of 312 mV/dec. The insert in the figure depicts the top-view of the measured TFT. We have tested 12 devices within a 15 mm × 15 mm area, and the devices statistics show a good uniformity. The standard deviation for extracted field-effective mobility is 0.05 cm^2/Vs, standard deviation for threshold voltage is 0.42 V, and standard deviation for subthreshold swing is 12.20 mV/dec.

B. BIAS STRESS MEASUREMENT

Bias stress measurements were conducted using a Lake Shore Model PS-100 tabletop cryogenic probe station and a Keithley 4200 semiconductor characterization system. All measurements were conducted in dark and the sample temperature was controlled by a Model 336 controller. To study the evolution of TFT parameters in the presence of bias stress, the bias stress was periodically interrupted to measure the transfer characteristics. The transfer characteristic measurement involved a cyclic sweep of V_{GS} to identify variations in subthreshold slope, threshold voltage and the presence of any hysteresis.

Fig. 4 (a) shows the transfer characteristics variation with time under constant bias stress (V_{GS} = 20 V and V_{DS} = 0.5 V) at 20°C. There was little threshold voltage shift, ΔV_{th} observed with the rate of increase of threshold voltage being 0.3 V/hour to 1 V/hour. Moreover, there was neither a significant variation in subthreshold slope nor any observable hysteresis. However, despite there being a shift in threshold voltage, it is well within the compensation limits for applications in displays [15]–[17]. Following previous reports (see [18] and references therein) and further justified by the insignificant change observed in field-effect mobility and off-current, the bias-induced shift is not caused by defects or vacancy sites in the amorphous oxide channel layer, but likely due to charge trapping in the insulator or at the channel-insulator interface. The latter is not expected to be significant [19], since there was no notable change was observed in the sub-threshold slope.

To further characterize and model the threshold voltage shift, measurements were conducted at 20°C, 50°C and 100°C as shown in Fig. 3b. Since trapping in the insulator is temperature dependent and expected to be predominant at higher temperatures, it becomes important to identify the contribution of the insulator trapping to the dynamics. Thus threshold voltage shift has been expressed as a conventional stretched exponential function of time given as

$$|\Delta V_{th}| = |\Delta V_0|\left\{1 - exp\left[-\left(\frac{t_{stress}}{\alpha + \tau_0 exp(E_\tau/kT)}\right)^{\beta}\right]\right\} \quad (1)$$

where ΔV_0 is the ΔV_{th} at $t = \infty$, E_τ the average effective energy barrier that electrons in the ISO TFT channel must overcome before entering the insulator, β the stretched-exponential exponent and α a coefficient. The trend of threshold voltage shift under bias stress at three temperatures was well fitted by the following parameters: $\Delta V_0 = 8.2$ V, $\alpha = 2.836 \times 10^3$ s, $\tau_0 = 8.209 \times 10^{-4}$ s, $E_\tau = 0.44$ eV, and $\beta = 0.58$.

Charge trapping in the insulator could be reduced by annealing and/or by improving the quality of the dielectric layer, for example, by using non water-based precursors in the ALD.

C. ILLUMINATION-STRESS MEASUREMENTS

In the illumination-stress measurements, the mounted LEDs and a T-Cube LED driver from Thorlabs were used to generate light at different wavelengths. The LEDs were controlled by an Agilent 33500B signal generator. The experiments were conducted in a dark environment, where the impact of ambient light was reduced to the bare minimum. Fig. 5 shows transfer characteristics of ISO TFTs

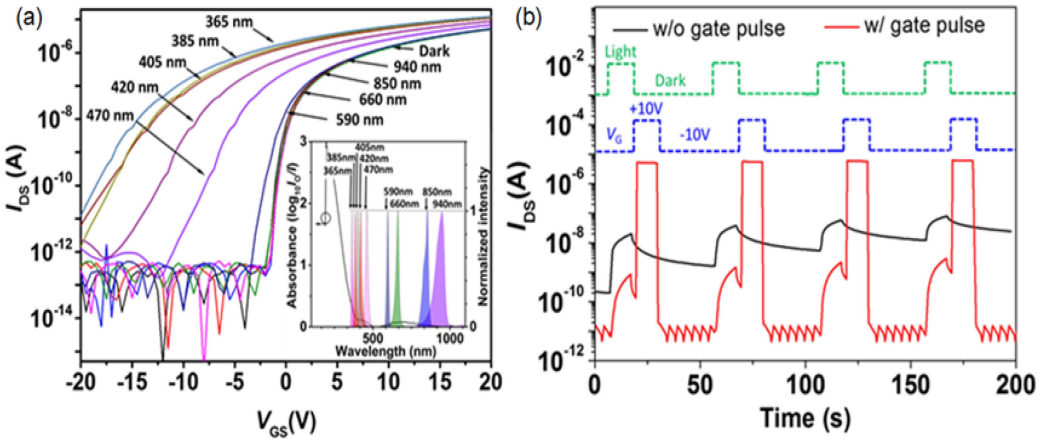

FIGURE 5. **(a) Transfer characteristics of the ISO TFT when subject to illumination stress for different wavelength (VDS = 0.5 V), insert is the UV-Vis absorbance of the ISO film and normalised spectra of the LED intensities. The spectral data of LEDs were adapted from Thorlabs datasheets. (b) Generation, recovery, and elimination of persistent photoconductivity exposed to pulse illumination (470 nm).**

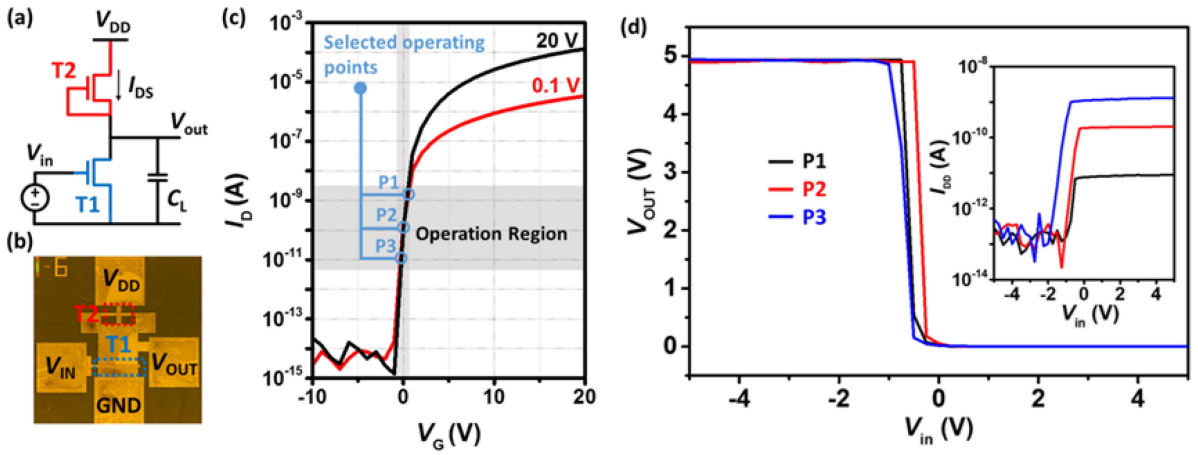

FIGURE 6. **(a) Circuit schematic and (b) photomicrograph, (c) sub-threshold operating points, and (d) corresponding input/output characteristics of the output stage.**

under exposure to light at different wavelengths. We see that the transfer characteristics were affected by the illumination as wavelengths approached the green-blue regions of the spectrum. The subthreshold swing, off-current, and on-current increases were inversely proportional to λ. The figure insert shows the UV-Vis absorbance and the LED spectrum. The ISO film strongly absorbs at wavelengths shorter than 400 nm, with the absorbance decreasing at increasing wavelengths, and eventually vanishing at around 500 nm. At higher wavelengths there is insufficient energy to generate photoconductivity, hence no obvious change in the transfer characteristics was observed.

The illumination ionized vacancy-related sites, typical in uncompensated AOS generate shallow doubly-ionized donor states and an un-depleted channel. These subgap defects have been related to hydrogen bonding within the vacancy sites [20], [21]. The confined photo-generated electrons lead to persistence in photoconductivity [22]–[24]. The persistent photoconductivity in an amorphous oxide semiconductor can be eliminated by a positive gate bias [24], [25].

As shown in Fig. 5, the generation, recovery, and elimination of photoconductivity were investigated with pulses of illumination. A 470 nm LED was selected as the light source. The transistor was biased at a V_{DS} of 20 V and a V_{GS} of −10 V. A 10-second illumination pulse generated a photocurrent of the order of 10 nA. This was followed by a 40-sec rest period in the dark. However, the TFT did not fully recover from exposure to the illumination. To eliminate the persistent photoconductivity, synchronized signals from a signal generator that controlled light illumination and gate voltage were produced. The interval between the falling edge of the light illumination signal and the rising edge of the gate bias signal was three seconds. With a gate pulse, the drain current was reset to its dark current value, which indicates that a positive gate bias could accelerate recovery, thus, effectively suppressing the persistent photoconductivity in the ISO film, thus enabling ISO-TFTs to be deployed in relatively high frame rate active matrix architectures.

IV. INDIUM SILICON OXIDE TFT CIRCUITS

As seen, the fully photolithographic fabricated ISO TFTs showed reasonable stability to electrical bias thereby making circuit design feasible. Apart from good environmental stability a key feature that makes circuit design with the fabricated ISO TFTs interesting is the fact that the initial threshold voltage of the devices are negative. This allows for the TFT to be above threshold at $V_{GS} = 0$ V which can be achieved by short-circuiting the gate to the source of the TFT. As observed in the transfer characteristics, setting $V_{GS} = 0$ V biases the ISO TFT to just above threshold voltage.

Fig. 6a shows a common source amplifier based on ISO TFTs with Fig. 6b illustrating the micrograph. The high transconductance of the driver along with the significant load impedance posed by the load TFT operating in subthreshold offer high gain. Based on the current through the TFT, the output voltage swing would be large enough to offer high gain. This concept is illustrated by viewing three operating points P1, P2 and P3 in Fig. 6b.

The circuit is of particular interest for large signal operation as a digital inverter. Normally, when NMOS devices are used as the load and driver, the digital output is not rail-to-rail due to the single threshold voltage drop offered by the load when the output goes high. However, since the threshold voltage of the fabricated ISO TFTs are negative, the output is seen to vary rail to rail. Fig. 6c shows the output of the circuit used as a digital inverter with the input varied from -5 V to $+5$ V.

V. CONCLUSION

Thin film transistors are presented drawing on a relatively new class of amorphous oxide semiconductor based on indium oxide doped with silicon oxide for the channel layer. The TFTs are fabricated using an all-photolithographic process at temperatures not exceeding 200°C, which makes the process compatible to plastic substrates. The devices showed good stability behavior under electrical and illumination stress, with effects persistent photoconductivity associated with negative bias illumination stress compensated using a nanosecond time duration positive gate pulse. Based on the developed ISO process, an all-TFT amplifier has been designed, fabricated and characterized yielding good small signal gain as well as large signal operation as a digital inverter by virtue of depletion mode operation.

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