Received 26 June 2020; revised 5 August 2020; accepted 6 August 2020. Date of publication 10 August 2020; date of current version 21 August 2020.
The review of this article was arranged by Editor M. J. Kumar.

Digital Object Identifier 10.1109/JEDS.2020.3015492

Investigation of Negative DIBL Effect and Miller Effect for Negative Capacitance Nanowire Field-Effect-Transistors

WEIXING HUANG [1,2], HUILONG ZHU [1], ZHENHUA WU [1], XIAOGEN YIN [1,2], QIANG HUO [1,2], KUNPENG JIA [1], YANGYANG LI [1,2], AND YONGKUI ZHANG [1]

1 Key Laboratory of Microelectronics Device and Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China
2 University of Chinese Academy of Sciences, Beijing 100049, China

CORRESPONDING AUTHORS: H. ZHU (e-mail: zhuhuilong@ime.ac.cn); K. JIA (e-mail: jiakunpeng@ime.ac.cn); AND Z. WU (e-mail: wuzhenhua@ime.ac.cn)

This work was supported in part by the Academy of Integrated Circuit Innovation under Grant Y7YC01X001, and in part by NSFC under Grant 91964202.

ABSTRACT In this study, the negative DIBL (N-DIBL), negative differential resistance (NDR), and Miller effect of a negative capacitance nanowire filed-effect-transistor (negative capacitance (NC) NWFET) were analyzed by employing the custom-built SPICE model. In the simulation, the minimum subthreshold swing (SS) reduced to 40 mV/decade with negligible hysteresis, and the on-current amplified by approximately three times. The N-DIBL effect was analyzed by building a model, and the results indicated that the N-DIBL is negatively correlated with the SS. Hence, it is indispensable to make trade-offs between the N-DIBL and SS in NC NWFET applications. Moreover, the Miller effect of a NCFET-based inverter was investigated for the first time. The Miller effect of the NC NWFET-based inverter was considerably improved owing to a high on-current and negative internal gate voltage (when external gate voltage is set to 0V), which is beneficial for high-speed circuit building based on NC NWFETs. The overshoot of the NC NWFET-based inverter is ∼43.1% less than that of the NWFET-based inverter, and the propagation delay of the NC NWFET-based inverter is ∼73.1% less than that of the NWFET-based inverter at ferroelectric thickness $T_{FE} = 3$nm.

INDEX TERMS Negative capacitance, nanowire FETs, SPICE model, negative DIBL, miller effect.

I. INTRODUCTION

Recently, to develop advanced CMOS technology in the sub-3-nm node range, negative capacitance field-effect-transistors (NCFETs) have attracted more attention owing to their exceptional performance and excellent process compatibility with existing CMOS technology [1]–[5]. Actually, nanowire field-effect-transistors with negative capacitance (NC) (NC NWFETs) have been considered the most promising candidates for sub-3-nm node [6]–[7]. Due to the enormous complexity of NC NWFETs, it is quite important to investigate the unconventional effects of NC NWFETs. In this study, the negative DIBL (N-DIBL) and negative differential resistance (NDR) of NC NWFETs were analyzed with a custom-built SPICE model. The undoubted negative correlation between N-DIBL and subthreshold swing (SS) makes a trade-off between N-DIBL and SS necessary.

Moreover, owing to the input-to-output coupling capacitance, the CMOS gate output voltage will be beyond the supply voltage range at the transition edge, which is called overshoot/undershoot. That is known as the Miller effect. For the CMOS gate using conventional long channel transistors, the miller effect is seldom of importance in digital circuits and is only of major importance in analog circuits. However, with the scaling of CMOS technology into deep sub-micrometer features sizes, the miller effect becomes significant and thus begin to be considered in CMOS gate analysis. In fact, with the scaling of the transistor, the influence of the Miller effect in high-speed circuits becomes non-negligible, which leads to circuit

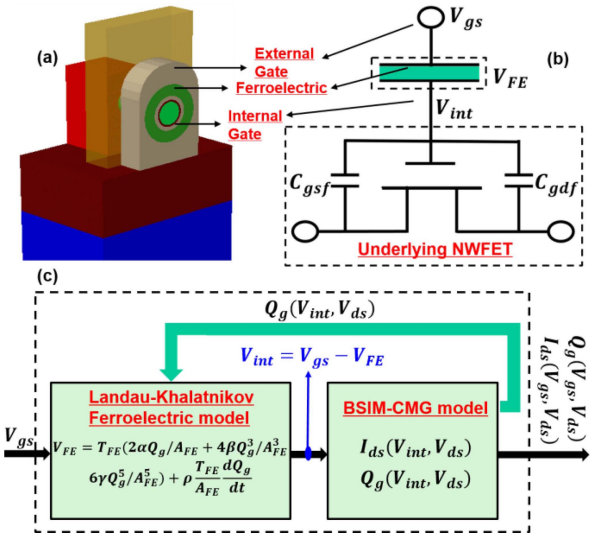

FIGURE 1. **(a) NC NWFET device structure, (b) NC NWFET device equivalent circuit diagram, and (c) Self-consistent simulation SPICE model for NC NWFET device. Underlying NWFET modeled with industry standard BSIM-CMG model. LK model governing ferroelectric voltage to be a dependent on charge while NWFET charge depends on voltage. This system is self-consistently solved in the model.**

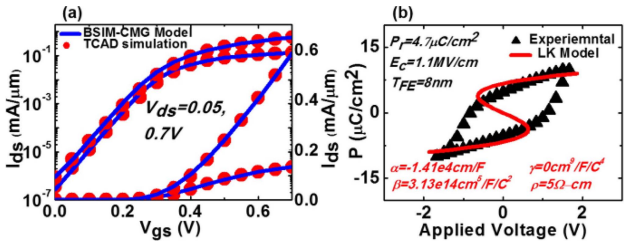

FIGURE 2. **(a) Our underlying NWFET model validation: agreement between TCAD simulation and BSIM-CMG model, (b) Measured polarization vs. voltage for $Hf_{0.6}Zr_{0.4}O_2$ films (Experiemntal) and the fitting results (LK Model).**

performance degradation [8]–[10] because it suffers from an increasing significant propagation delay [11] and high-κ layer leakage [12]. In this study, the Miller effect of a NCFET-based inverter was investigated for the first time, and we found that the Miller effect of the NC NWFET-based inverter was considerably improved owing to the high on-current and negative internal gate voltage (V_{int}) (when external gate voltage is set to 0V).

In this work, a transient simulation was performed to analyze the hysteretic behavior of NC NWFETs for device-level analysis, and a simple model was built to investigate the N-DIBL effect. A transient inverter simulation was performed to analyze the Miller effect of NC NWFET-based and the underlying NWFET-based inverters.

II. SPICE MODEL AND SIMULATION METHOD

A schematic of the NC NWFET device structure and equivalent circuit diagram of the NC NWFET are presented in Fig. 1 (a)–(b). In our SPICE model, fringe capacitance was taken into account as shown in Fig. 1 (b). We obtained

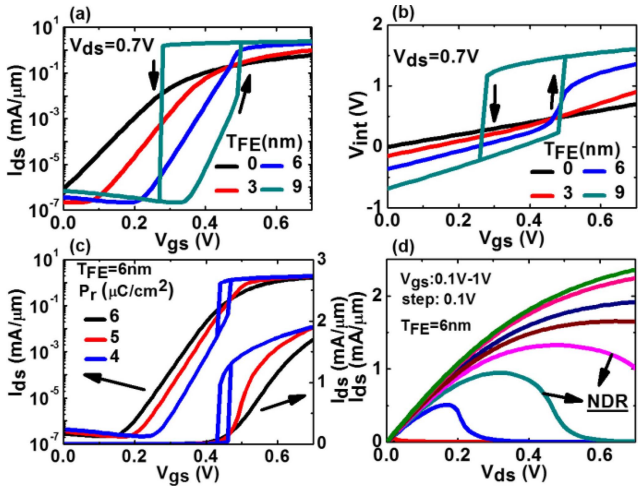

FIGURE 3. **The characteristics of a NC NWFET: (a) $I_{ds} - V_{gs}$ characteristics of NC NWFETs for different T_{FE}, (b) V_{int} characteristics of NC NWFETs for different T_{FE}, (c) $I_{ds} - V_{gs}$ characteristics of NC NWFETs for different P_r, and (d) NDR effect at $T_{FE} = 6$ nm.**

a parasitic capacitance between internal gate and source electrodes (and similarly gate and drain electrodes) in underlying NWFET to be ~0.02fF from TCAD simulation. The NC and underlying NWFET are in series (Fig. 1 (b)). Thus, the charge balance between the ferroelectric capacitance (C_{FE}) and gate capacitance of the underlying NWFET (C_{MOS}) was applied in the simulation, and the amount of charge on C_{MOS} was equal to that on the C_{FE}. Figure 1 (c) presents self-consistent simulation SPICE model for NC NWFET device, and this modeling approach has been used in the previous work [13].

The schematic of self-consistent compact model is shown in Fig. 1 (c). It shows that the Landau-Khalatnikov (LK) model is self-consistently solved with the three-dimensional device electrostatics using the industry standard NWFET compact model BSIM-CMG. First, we extract the parameters for underlying NWFET and an excellent agreement between TCAD simulation and BSIM-CMG model can be seen from Fig. 2 (a). Next, we extract the ferroelectric parameters. The ferroelectric parameters, which were used in the LK model, were extracted from our experimental $Hf_{0.6}Zr_{0.4}O_2$ data as shown in Fig. 2 (b). The values of α, β, γ, and ρ have been presented in the Fig. 2(b). Based on Landau-Ginzburg-Devonshire phenomenological theory, if ferroelectric material undergoes a second order phase transition, then $\alpha < 0, \beta > 0$ and $\gamma = 0$ in Landau equation. Moreover, the value of ρ was estimated as mentioned in [14]–[16].

BSIM-CMG is a compact model for the class of common multi-gate FETs [17]. Physical surface-potential-based formulations are derived for both intrinsic and extrinsic models with finite body doping. The surface potentials at the source and drain ends are solved analytically with poly-depletion and quantum mechanical effects. BSIM-CMG include physical effects of real device, such as Quantum Mechanical Effects (QME), Short-channel Effects (SCE),

threshold voltage roll-off, DIBL, SS degradation, Channel length modulation and so on. These physical effects of real device are of a great significance to short channel device which is applied for sub-3nm node. An accurate underlying NWFET model is very important to develop a model for NC NWFETs because the LK equation depends on the charge of the underlying NWFET. The charge of underlying NWFET is affected by QME and SCE, and LK equation depends on the charge of underlying NWFET. Hence, in aggressively scaled devices of 3nm node and beyond QME and SCE are important to NC effect (N-DIBL, NDR, sub-SS).

The parameters for the BSIM-CMG model were calibrated from TCAD-simulated underlying NWFETs in the sub-3-nm node range. In TCAD simulation, based on IRDS 2017 [18], the physical gate length and channel diameter of underlying NWFETs were set to 12nm and 6nm respectively at sub-3nm node. The gate oxide thickness (IL) of underlying NWFET is 0.8nm. The doped silicon (As/1e20cm^{-3} for nNWFET and B/1e20cm^{-3} for pNWFET) was used as source/drain. The source and drain doping slopes were generated by rapid thermal annealing (RTA) at 1100℃. The undoped silicon was used as channel material. Moreover, the lumped series resistance is set to 4000Ω to model source/drain contact and source/drain epi-diffused resistance.

In TCAD simulation, the quantum confinement and the ballistic transport was addressed on a physical level by implementing 2D Schrodinger-Poisson solver, combined with the conventional drift-diffusion equation solver for low-field region and phase-space subband Boltzmann transport equation solver for saturation region respectively. *k·p* based multi-subbands electronic structures are calculated for electrostatics. As compared to conventional TCAD framework, the physical level modeling has advantages that it captures the subband variations under strong confinement and considers multiple carrier scattering mechanisms, phonon scattering, and surface roughness scattering directly, rather than empirical mobility models. Overall verification of above physics-based models was shown in our previous work [19]–[20] by comparing with the measurement data of the in-house 5nm node SOI nanowire [21]. Furthermore, this validated TCAD framework can well reproduce the published data of the state-of-the-art 7-nm node FinFET [22] and fairly guarantee the accuracy of our SPICE model.

III. RESULTS AND DISCUSSION

The electrical characteristics of the NC NWFETs with different ferroelectric thicknesses (T_{FE}) (T_{FE} = 0 nm represents for underlying NWFET) are presented in Fig. 3 (a). Clearly, as T_{FE} increases, the switching characteristics become steeper owing to the greater voltage amplification in V_{int} provided by NC. However, the NC NWFET is unstable when T_{FE} is larger than a certain critical thickness. To understand the hysteresis characteristics of $I_{ds}-V_{gs}$, the total gate capacitance (C_{total}) of the NC NWFET was analyzed using the following equation:

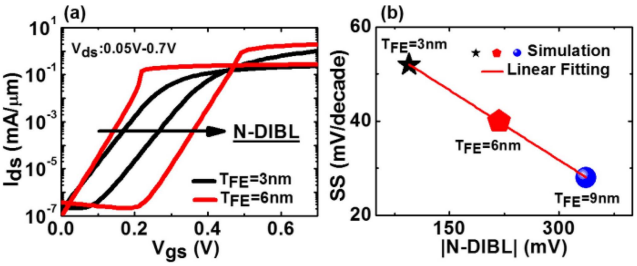

FIGURE 4. (a) The N-DIBL effect of NC NWFETs at T_{FE} = 3nm and 6nm, (b) the N-DIBL is negatively correlated with the SS for NC NWFETs.

$$C_{total} = \frac{|C_{FE}| * C_{MOS}}{|C_{FE}| - C_{MOS}} \tag{1}$$

Here, C_{FE} is the ferroelectric capacitance, and C_{MOS} is the gate capacitance of the underlying NWFET. In this study, when T_{FE} = 6 nm, the $|C_{FE}|$ was larger than C_{MOS}. Thus, C_{total} was positive, and the NC NWFET was stable. However, when T_{FE} > 6 nm, the $|C_{FE}|$ was less than C_{MOS}. Therefore, C_{total} was negative, and the NC NWFET was unstable, resulting in hysteresis in the transfer curve. The V_{int} characteristics of the NC NWFET for different ferroelectric thickness are presented in Fig. 3 (b). V_{int} increased with the increasing of T_{FE} thank to greater voltage amplification. Fig. 3 (c) shows $I_{ds} - V_{gs}$ characteristics of NC NWFET with different remanent polarization (P_r). NC effects increased with the decreasing of Pr owing to decreased $|C_{FE}|$.

Moreover, some unconventional effects arise in the NC NWFET electrical properties owing to the existence of NC. An unconventional effect is the NDR effect, as presented in Fig. 3 (d). The NDR effect in the NC NWFET originated from the coupling of the drain voltage to the V_{int} *via* the gate to drain capacitance, leading to the current loss of the transistor [14], [23].

Another unconventional effect is the N-DIBL effect. Fig. 4 (a) presents the N-DIBL effect, which is opposite from the DIBL effect in a conventional transistor. The threshold voltage (V_t) of the NC NWFET increases with an increased drain voltage (V_{ds}). Evidently, the V_{ds} has a similar effect on the channel potential as the gate voltage (V_{gs}) owing to the existence of coupling capacitance from the drain to the channel. Thus, V_{gs} and V_{ds} combined determine the channel potential barrier height. This understanding gives us a simple model for the N-DIBL effect:

$$V_t = V_{t-long} - \delta V_{ds} \frac{C_d}{(|C_{FE}|C_{ox})/(|C_{FE}| - C_{ox})} \tag{2}$$

where V_{t-long} is the threshold voltage of a long-channel transistor, when the coupling capacitance from the drain to the channel equals 0. δ is proportionality factor. $(|C_{FE}|C_{ox})/(|C_{FE}| - C_{ox})$ is the gate dielectric capacitance of a NC NWFET, which includes ferroelectric capacitance C_{FE} and internal gate dielectric capacitance C_{ox}. It is worth nothing that the $(|C_{FE}|C_{ox})/(|C_{FE}| - C_{ox})$ is not C_{total}, because

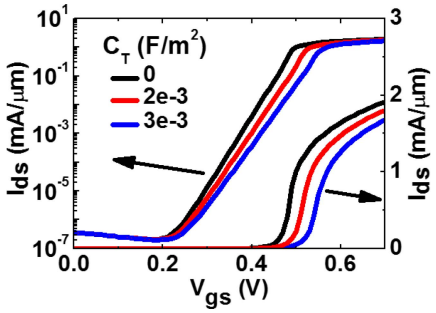

FIGURE 5. The effects of internal gate traps on NC NWFET characteristics.

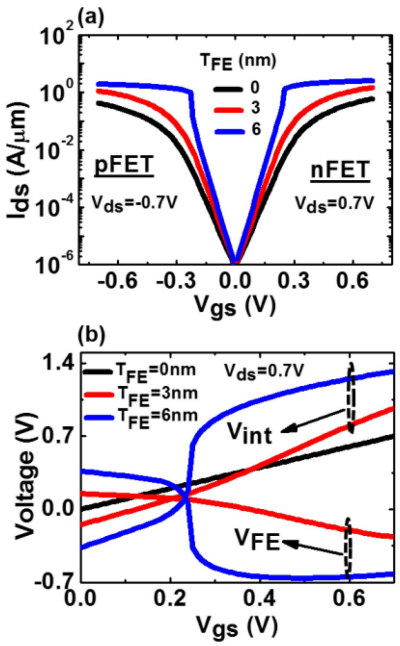

FIGURE 6. (a) $I_{ds} - V_{gs}$ characteristics of a NC NWFET for different T_{FE} at same off-current and (b) voltage amplification characteristics of the NC NWFET for different T_{FE} (for NC n-NWFET).

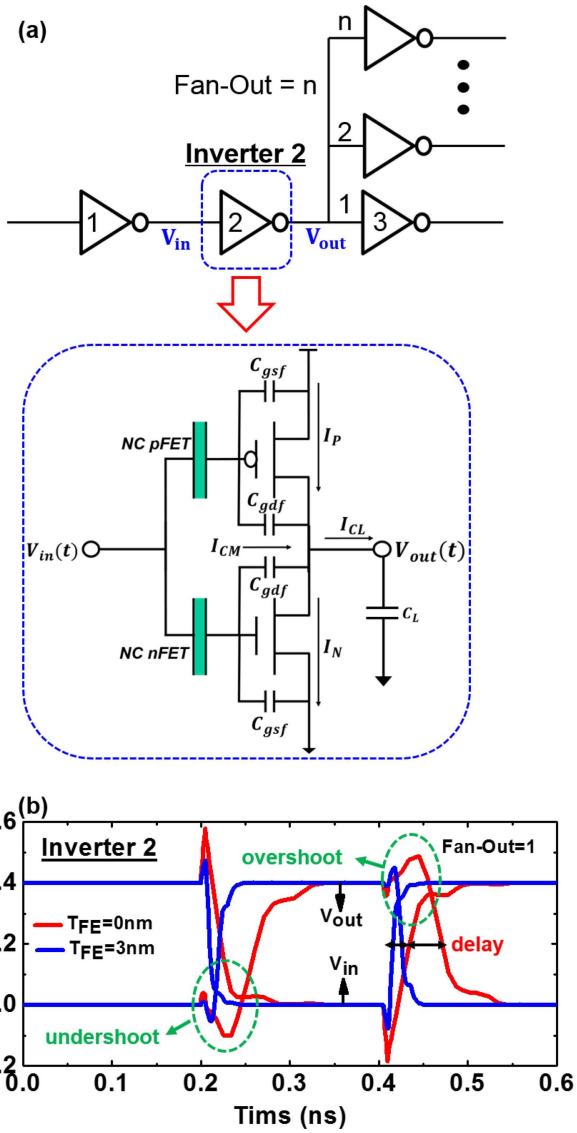

FIGURE 7. (a) Circuit schematic of a NC NWFET-based inverter chain, and the Inverter 2 is used for analysis to use a real input signal, (b) transient responses of the NC NWFET-based inverter (T_{FE} = 3nm) and underlying NWFET-based inverter (T_{FE} = 0nm) at Fan-Out = 1.

the former does not contain channel silicon capacitance. The $(|C_{FE}|C_{ox})/(|C_{FE}| - C_{ox})$ of the NC NWFET must be a negative value for the NC effect. Thus, the second item in Equation (2) becomes a positive value, and the N-DIBL effect is observed. Physically, the N-DIBL effect originated from an increase in the channel potential barrier owing to the drain voltage distribution effect between coupling capacitance C_d and gate dielectric capacitance $(|C_{FE}|C_{ox})/(|C_{FE}| - C_{ox})$. Of note, the N-DIBL decreases with a decrease in T_{FE}, as presented in Fig. 4 (a) owing to the increase in $|(|C_{FE}|C_{ox})/(|C_{FE}| - C_{ox})|$; however, the SS of NC NWFETs increases with a decrease in T_{FE}, as presented in Fig. 3 (a). Thus, the N-DIBL and SS have a negative correlation as shown in Fig. 4 (b). Therefore, trade-offs between SS and N-DIBL are indispensable for the application of NCFETs.

Moreover, it is likely that charges will be trapped in the internal gate of NC NWFET. In our SPICE model, a parasitic capacitance (C_T), which can accept and release channel charge, was introduced to simulate internal gate trap effect. The SS and Ion degraded with increase in trap charges because of well known effects of charge trapping such as drift in threshold voltage as shown in Fig. 5".

Moreover, compared with the underlying NWFET, the V_t of the NC NWFET increases with an increase in T_{FE} at the same metal gate work function (WF), as presented in Fig. 3 (a). Thus, it is necessary to adjust V_t to a suitable value in practical applications by adjusting the WF. Figure 6 (a) presents the $I_{ds} - V_{gs}$ characteristics of the NC NWFET for different T_{FE} at same off-current. Finally, WF = 4.37/4.22/4.0 eV and WF = 4.81/4.96/5.17 eV were selected for the NC n-NWFET and NC p-NWFET, respectively, for NC NWFET-based inverter building. For NC n-NWFET and NC p-NWFET, TiAlC and TiN can be used to adjust the

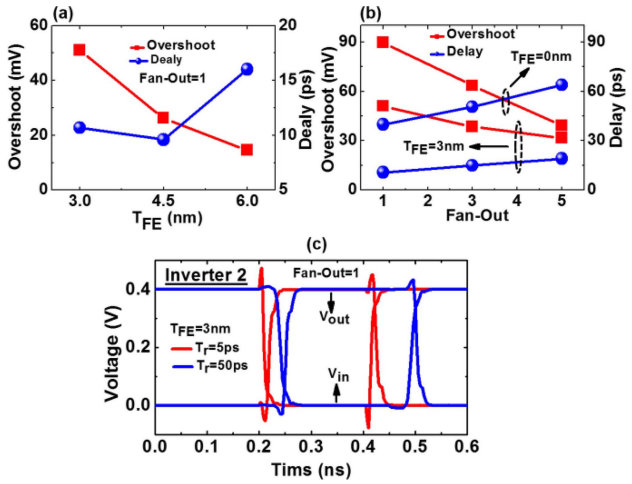

FIGURE 8. (a) The influence of T_{FE} on miller effect at Fan-Out = 1, (b) the influence of Fan-Out on miller effect at T_{FE} = 0nm and 3nm, (c) the influence of input slew rate on miller effect at T_{FE} = 3nm and Fan-Out = 1.

WFs, respectively. Figure 6 (b) presents the voltage amplification in a NC NWFET for different T_{FE} (for a NC n-NWFET). When the V_{gs} is equal to 0 V, the V_{int} is equal to −0.37 V. Thus, the V_{int} will accelerate the discharge of the Miller capacitance of the underlying NWFET to improve the Miller effect, which is similar to negative gate voltage drive technology.

To analyze the Miller effect of NC NWFETs, the transient responses of NC NWFET-based and underlying NWFET-based inverters were examined. Figure 7 (a) presents a circuit schematic of a NC NWFET-based inverter chain. It is worth nothing that the Inverter 2 is used for analysis to use a real input signal.

Figure 7 (b) shows that both NC NWFET-based inverter (T_{FE} = 3nm) and NWFET-based inverter (T_{FE}=0nm) suffer from overshoot/undershoot of the output signal. Of note, based on previous works [14], [24], NCFET has greater advantage at small supply voltage, so, supply voltage is set to 0.4V. The overshoots of the NC NWFET-based and NWFET-based inverters are 89.53 and 50.98 mV, respectively. The overshoot of the NC NWFET-based inverter is ∼43.1% less than that of the NWFET-based inverter. Moreover, the propagation delay of the NC NWFET-based inverter is ∼73.1% less than that of the NWFET-based inverter. Of note, the improved propagation delay will increase the maximum working frequency (f_{max}) of the inverter. In this study, the f_{max} of the inverter increased ∼2X due to the improved Miller effect by using NC. The Miller effect of the NC NWFET-based inverter was considerably improved owing to the high on-current and nonzero V_{int}. The larger on-current can accelerate the charging of miller capacitance C_M and load capacitance C_L to improve the Miller effect. The negative V_{int} can accelerate the discharge of C_M to improve the Miller effect.

Figure 8 (a) presents the influence of T_{FE} on miller effect at Fan-Out=1. The overshoot value of NC NWFET-based inverter decreases with the increasing of T_{FE} owing to increased NC effect. However, the delay value of inverter increased at T_{FE} = 6nm owing to increased ferroelectric resistance R_{FE} ($R_{FE} = \rho T_{FE}/A_{FE}$). Figure 8 (b) presents the influence of Fan-Out on miller effect at T_{FE} = 0nm and 3nm. The overshoot value of inverter decreases with the increasing of Fan-out owing to increased load capacitance. However, increased load capacitance results in increasing of delay. Figure 8 (c) presents the influence of input slew rate on miller effect at TFE=3nm and Fan-Out = 1. The overshoot decreases and delay increases for increase in input rise time T_r.

IV. CONCLUSION

This paper presents a comprehensive analysis of ultra-small NC NWFETs at sub-3nm node. In this letter, the N-DIBL, NDR, and Miller effect of a NC NWFET were analyzed by employing the custom-built SPICE model. The analysis indicated that the N-DIBL and SS have a negative correlation; thus, trade-offs between N-DIBL and SS were proposed. The Miller effect of the NCFET-based inverter was investigated for the first time. Our analysis revealed that the Miller effect of the NC NWFETs-based inverter was considerably improved owing to the high on-current and negative internal gate voltage, which is beneficial for high-speed circuit building based on NC NWFETs. The overshoot of the NC NWFET-based inverter is ∼43.1% less than that of the NWFET-based inverter, and the propagation delay of the NC NWFET-based inverter is ∼73.1% less than that of the NWFET-based inverter at T_{FE} = 3nm.

REFERENCES

[1] K.-S. Li *et al.*, "Sub-60mV-swing negative-capacitance FinFET without hysteresis," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2015, pp. 22.6.1–22.6.4, doi: 10.1109/IEDM.2015.7409760.

[2] Z. H. Zhang *et al.*, "FinFET with improved subthreshold swing and drain current using 3-nm ferroelectric ferroelectric $Hf_{0.5}Zr_{0.5}O_2$," *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 367–370, Mar. 2019, doi: 10.1109/LED.2019.2891364.

[3] A. I. Khan *et al.*, "Negative capacitance in short-channel FinFETs gernally connected to an epitaxial ferroelectric capacitor," *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 111–114, Jan. 2016, doi: 10.1109/LED.2015.2501319.

[4] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplication for low power nanoscale devices," *Nano Lett.*, vol. 8, no. 2, pp. 405–410, 2008, doi: 10.102/nl071804g.

[5] Z. Y. Zhu *et al.*, "Negative-capacitance characteristics in a steady state ferroelectric capacitor made of parallel domains," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1176–1179, Aug. 2017, doi: 10.1109/LED.2017.2721954.

[6] W. X. Huang *et al.*, "Simulations of VNW-FETs with adjustable spacer-like negative capacitors based on experimental data," *ECS J. Solid-State Sci.*, vol. 8, no. 2, pp. 38–42, Mar. 2019, doi: 10.1149/2.0211902jss.

[7] S. Y. Lee *et al.*, "Experimental demonstration of stacked Gate-All-Around poly-Si nanowires negative capacitance FETs with internal gate featuring seed layer and free of post-metal annealing process," *IEEE Electron Device Lett.*, vol. 40, no. 11, pp. 111–114, Nov. 2019, doi: 10.1109/LED.2019.2940696.

[8] L. Bisdounis, "Analytical modeling of overshooting effect in sub-100 nm CMOS inverters," *J. Circuits, Syst. Comput.*, vol. 20, no. 7, pp. 1303–1321, Nov. 2011, doi: 10.1142/S0218126611007967.

[9] J. Segura and C. F. Hawkins, *CMOS Electronics: How It Works, How It Fails*. Hoboken, NJ, USA: Wiley, Apr. 2004, pp. 107–110, doi: 10.1002/0471728527.ch4.

[10] F. Farbiz, A. Appaswamy, A. A. Salman, and G. Boselli, "Overshootinduced failures in forward-biased diodes: A new challenge to highspeed ESD design," in *Proc. IEEE Int. Rel. Phys. Symp.*, Apr. 2013, pp. 2B.1.1–2B.1.8, doi: 10.1109/IRPS.2013.6531946.

[11] Z. Huang, A. Kurokawa, M. Hashimoto, T. Sato, J. Minglu, and Y. Inoue, "Modeling the overshooting effect for CMOS inverter delay analysis in nanometer technologies," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 29, no. 2, pp. 250–260, Feb. 2010, doi: 10.1109/TCAD.2009.2035539.

[12] G. X. Wan *et al.*, "Overshoot stress on ultra-thin HfO_2 high-k layer and its impact on lifetime extraction," *IEEE Electron Device Lett.*, vol. 36, no. 12, pp. 1267–1270, Dec. 2015, doi: 10.1109/LED.2015.2490719.

[13] S. Khandelwal, J. P. Duarte, A. I. Khan, S. Salahuddin, and C. Hu, "Impact of parasitic capacitance and ferroelectric parameters on negative capacitance FinFET characteristics," *IEEE Electron Device Lett.*, vol. 38, no. 1, pp. 142–144, Jan. 2017, doi: 10.1109/LED.2016.2628349.

[14] S. Gupta, M. Steiner, A. Aziz, V. Narayanan, S. Datta, and S. K. Gupta, "Device-circuit analysis of ferroelectric FETs for low-power logic," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3092–3100, Aug. 2017, doi: 10.1109/TED.2017.2717929.

[15] A. I. Khan *et al.*, "Negative capacitance in a ferroelectric capacitor," *Nat. Mater.*, vol. 14, no. 2, pp. 182–186, 2015.

[16] C. Hsu, C. Pan, and A. Naeemi, "Performance analysis and enhancement of negative capacitance logic devices based on internally resistive ferroelectrics," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 765–768, Feb. 2018, doi: 10.1109/LED.2018.2820118.

[17] *BSIM Group in UC Berkeley*. Accessed: Jun. 2019. [Online]. Available: http://bsim.berkeley.edu/models/bsimcmg/

[18] *International Roadmap for Devices and Systems (IRDS TM) 2017 Edition*. Accessed: Jun. 2019. [Online]. Available: https://irds.ieee.org/editions/2017

[19] Q. Huo *et al.*, "A novel general compact model approach for 7-nm technology node circuit optimization from device perspective and beyond," *IEEE J. Electron Devices Soc.*, vol. 8, no. 1, pp. 295–301. Mar. 2020, doi: 10.1109/JEDS.2020.2980441.

[20] Q. Huo *et al.*, "Physics-based device-circuit cooptimization scheme for 7-nm technology node SRAM design and beyond," *IEEE Trans. Electron Devices*, vol. 67, no. 3, pp. 907–914, Jan. 2020, doi: 10.1109/TED.2020.2964610.

[21] Q. Zhang *et al.*, "Novel GAA Si nanowire p-MOSFETs with excellent short-channel effect immunity via an advanced forming process," *IEEE Electron Device Lett.*, vol. 39, no. 4, pp. 464–467, Apr. 2018, doi: 10.1109/LED.2018.2807389.

[22] S. Narasimha *et al.*, "A 7nm CMOS technology platform for mobile and high performance compute application," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2017, pp. 29.5.1–29.5.4, doi: 10.1109/IEDM.2017.8268476.

[23] J. R. Zhou *et al.*, "Negative differential resistance in negative capacitance FETs," *IEEE Electron Device Lett.*, vol. 39, no. 4, pp. 622–625, Apr. 2018, doi: 10.1109/LED.2018.2810071.

[24] W. X. Huang *et al.*, "Investigation of device-circuit for negative capacitance vertical nanowire FETs based on SPICE model," *Semicond. Sci. Technol*, vol. 35, no. 8, May 2020, Art. no. 085018, doi: 10.1088/1361-6641/ab8e0e.