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Characterization and Modeling of 0.18μm Bulk CMOS Technology at Sub-Kelvin Temperature

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ABSTRACT Previous cryogenic electronics studies are mostly at 77K and 4.2K. Cryogenic characterization of a 0.18μm standard bulk CMOS technology (operating voltages: 1.8V and 5V) is presented in this paper. Several NMOS and PMOS devices with different width to length ratios (W/L) were extensively tested and characterized under various bias conditions at sub-kelvin temperature. In addition to devices dc characteristics, the kink effect and current overshoot phenomenon are observed and discussed at sub-kelvin temperature. Especially, the current overshoot phenomenon in PMOS devices at sub-kelvin temperature is shown for the first time. The transfer characteristics of MOSFET devices (1.8V W/L = 10μm/10μm) at sub-kelvin temperature are modeled using the simplified EKV model. This work facilitates the CMOS circuits design and the integration of CMOS circuits with silicon-based quantum chips at extremely low temperatures.

INDEX TERMS Cryogenic CMOS, characterization, modeling, kink effect, current overshoot, sub-Kelvin temperature.

I. INTRODUCTION

Cryogenic CMOS (cryo-CMOS) has been researched in recent years due to the rise of quantum chip and quantum computer research [1], [2]. CMOS circuits integrated with quantum bits on the same substrate or standalone CMOS circuits working at extremely low temperatures can improve the scalability of quantum chips, system integration and performance [3], [4]. However, cryo-CMOS circuits face several challenges such as refrigeration power, interconnection, and device modeling. For instance, the valid temperature for BSIM3 [5] or BSIM4 [6] model is from −40°C to 125°C. The characteristics of MOSFET devices change due to the freeze-out effect at low temperatures.

At present, CMOS technologies ranging from 0.35μm to 28nm have been characterized and modeled at the liquid nitrogen temperature (77K) and the liquid helium temperature (4.2K) [7]–[9]. Moreover, the characteristic testing [10] and modeling [11] at sub-kelvin temperature have further revealed the cryo-temperature device picture.

This paper contains the characteristics of 0.18μm MOSFET devices, particularly, the kink effect and current overshoot phenomenon of MOSFET devices at sub-kelvin temperature. We developed a compact model for transfer characteristics of large size devices based on the simplified EKV model. The compact model can be used for estimating the power consumption of MOSFET devices and simulating CMOS circuits design at sub-kelvin temperature.

II. CRYOGENIC MEASUREMENT SETUP

Several transistors with different gate oxide thicknesses (TOX) and different sizes were tested at around 270mK, as shown in Table 1. The metal layers in the back end of line (BEOL) are made of aluminum. The tested chip and chip-carrier were connected with Al-wire bonding. The ^{3}He

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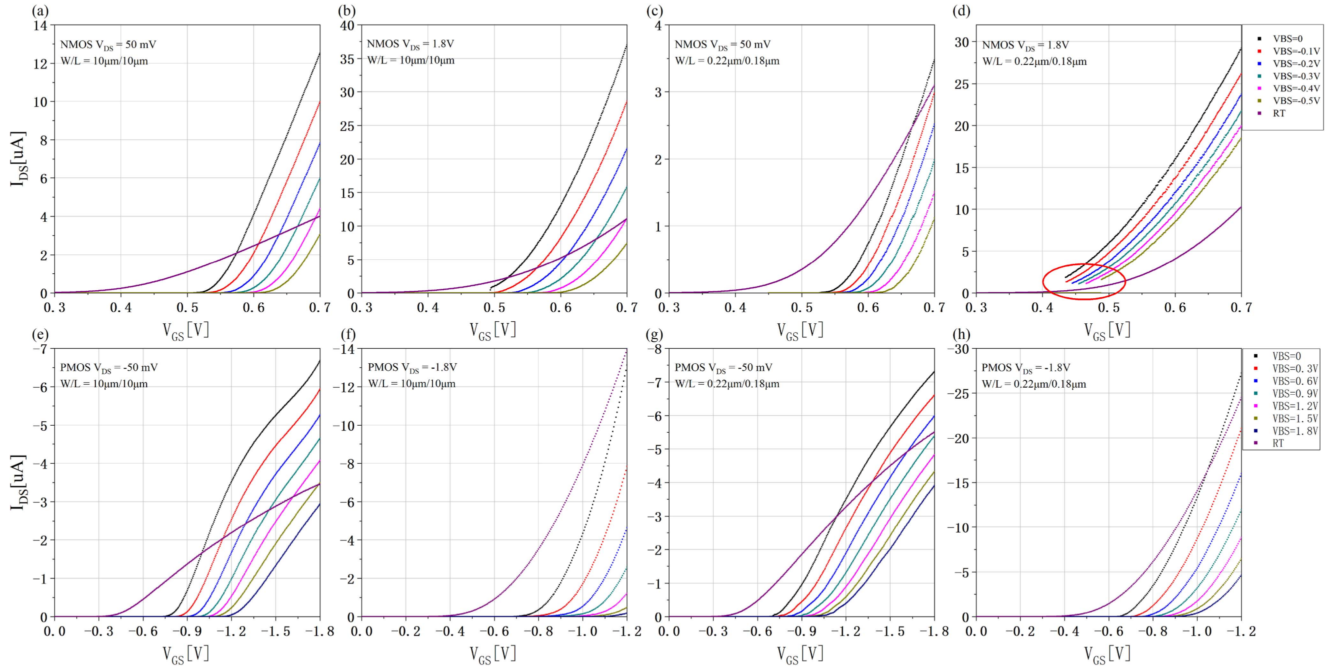

FIGURE 1. Transfer characteristics of thin TOX MOSFET devices at sub-kelvin temperature (forward scan). Purple lines are for $V_{BS} = 0V$ at room temperature (RT). (a-d) Transfer characteristics of the large size NMOS device (W/L = 10μm/10μm) and the small size NMOS device (W/L = 0.22μm/0.18μm),$V_{GS} = 0.3V \rightarrow 0.7V$ ($V_{GS} = 0.45V \rightarrow 0.7V$ for c) step=$1mV$, $V_{BS} = 0V \rightarrow -0.5V$ step= $-0.1V$, $V_{DS} = 50mV$ or $1.8V$. (e-h) Transfer characteristics of the large size PMOS device (W/L = 10μm/10μm) and the small size PMOS device (W/L = 0.22μm/0.18μm), $V_{GS} = 0V \rightarrow -1.2V$ or $-1.8V$ step= $-5mV$, $V_{BS} = 0V \rightarrow 1.8V$ step=0.3V, $V_{DS} = -50mV$ or $-1.8V$.

TABLE 1. Summary of characterized devices.

Technology	SMIC 0.18μm Bulk CMOS 1P6M Process			
Voltage and TOX	1.8V Thin		5V Thick	
Type	NMOS	PMOS	NMOS	PMOS
W/L[μm/ μm]	10/10	10/10	10/10	10/10
	10/0.6	10/0.6	10/2	10/2
	10/0.2	10/0.18	10/0.65	10/0.5
	10/0.18	10/0.16	10/0.5	10/0.45
	10/0.16	0.22/0.18	0.3/0.6	
	0.22/0.18			

refrigerator was used to cool devices. The devices under test (DUT) were put into the dual in-line package (DIP) socket at the bottom of the refrigerator. The DIP socket was connected to BNC connectors at the top of the refrigerator via cables. The bottom of the DIP socket was connected to the ^{3}He pot through the copper. An internal vacuum chamber was built around the sample, and a temperature sensor was used to characterize the ^{3}He pot (and DUT) temperature in the vacuum chamber. The sample was inserted into the cryostat to cool down to around 270mK. All MOSFET electrical measurements were performed using the Keysight B1500A semiconductor device analyzer. The interconnection between the DUT and B1500A was realized through BNC cables and BNC Triax to BNC adapters.

Testing of the characteristics at around 270mK should limit the power of devices, limited by the cooling power (40μW). We observed that the temperature fluctuated during the test, from 264mK to 274mK. When the temperature changed dramatically beyond 274mK, we waited for the temperature to drop below 270mK, changed bias voltages and re-measured to ensure that the device worked at around 270mK.

For 1.8V MOSFET, transfer characteristics in linear ($|V_{DS}| = 50mV$) and saturation regions ($|V_{DS}| = 1.8V$) for different substrate bias voltages were measured on various devices in Table 1. V_{GS} was appropriately reduced to limit current and ensure temperature stability in Fig. 1, except Fig. 1 (e,g). When the V_{BS} was sufficient during the test, no obvious transfer curve could be observed in Fig. 1(a-b). So the V_{BS} was under 0 to −0.5V. For 5V MOSFET, bias voltages changed. Characteristics in other bias voltages were also measured at around 270mK. In addition to the above normal measurements (hold time = 0s, delay time = 0s), the output characteristics were measured which were in different hold time (time after the measurement trigger until starting delay time) and delay time (time after the hold time until starting measurement). For details of hold time and delay time, please see [12, Figs. 4–6].

III. CHARACTERIZATION

A. TRANSFER CHARACTERISTICS

Fig. 1 and Fig. 2 show the transfer characteristics of large and small thin TOX MOSFET devices. Fig. 3 shows the transfer characteristics of the thick TOX NMOS (W/L=0.3μm/0.6μm) and PMOS (W/L=10μm/10μm) in

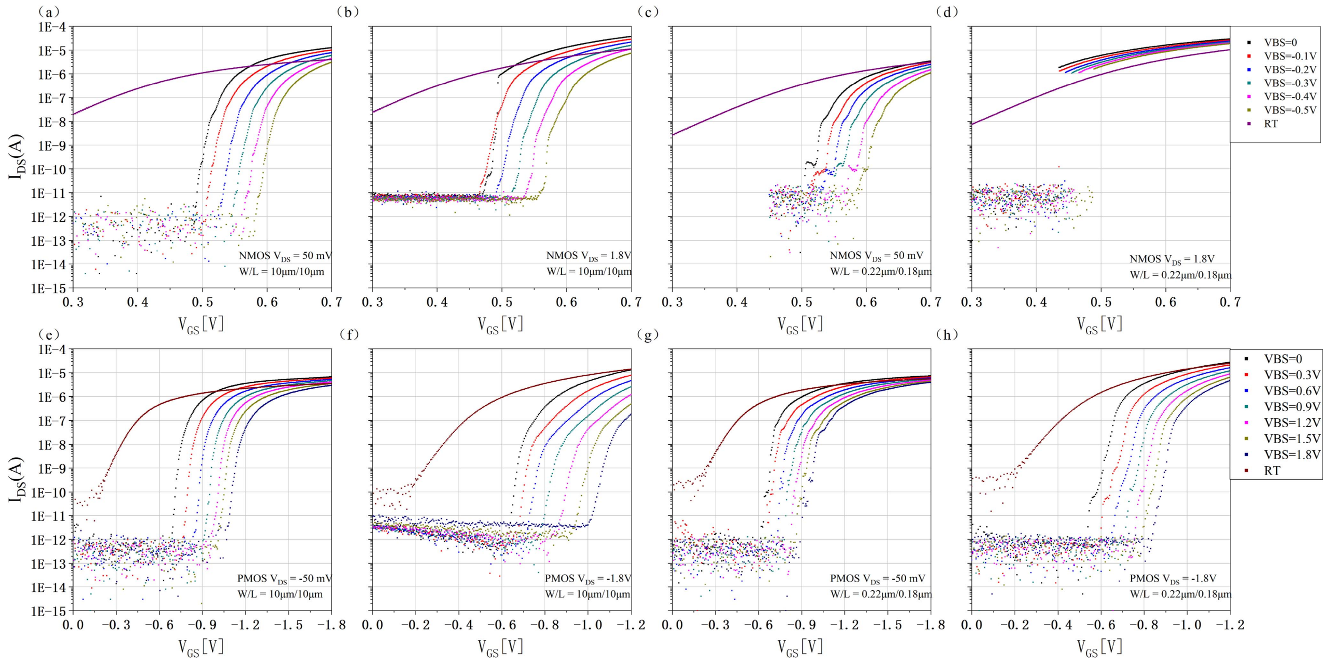

FIGURE 2. **Transfer characteristics of thin TOX MOSFET devices at sub-kelvin temperature. The semilog plot is for Fig. 1.**

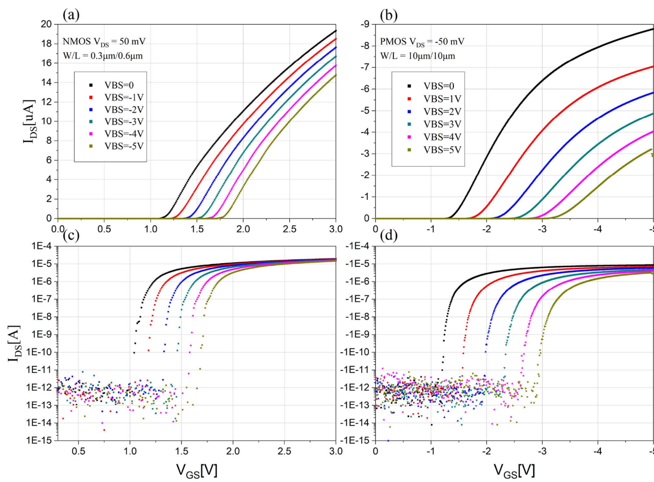

FIGURE 3. **Transfer characteristics of thick TOX MOS at sub-kelvin temperature (forward scan). (a,c) Transfer characteristics of the small size NMOS device(W/L = 0.3μm/0.6μm), $V_{GS} = 0V \rightarrow 3V$ step=10mV, $V_{BS} = 0V \rightarrow -5V$ step= $-1V$, $V_{DS} = 50mV$; (b,d) Transfer characteristics of the large size PMOS device(W/L = 10μm/1μm), $V_{GS} = 0V \rightarrow -5V$ step= $-10mV$, $V_{BS} = 0V \rightarrow 5V$ step=1V, $V_{DS} = -50mV$.**

linear region. The drain current is still depending on the V_{GS} and W/L. The threshold voltage (V_{th}) changes with substrate bias voltage. Transfer characteristics are similar to the usual results for MOSFET. Fig. 1(a,b) give transfer characteristics of the large NMOS device at sub-kelvin temperature. For the small NMOS device in Fig. 1(c,d), the V_{th} decreases rapidly because of drain induced barrier lowering (DIBL) effect [13], [14]. The DIBL effect is also shown in Fig. 1(g,h).

Fig. 1(d) and Fig. 2(d) show an abnormal phenomenon about current step: when the gate to source voltage (V_{GS}) reaches V_{th}, I_{DS} suddenly changes into micro-amperes (μA) current. For $V_{BS} = 0$ in Fig. 1(b) and Fig. 2(b), we can observe the current step phenomenon also. For thin and thick TOX devices, we have observed the abnormal phenomenon in NMOS but not in PMOS. For NMOS transfer characteristics in the saturation region, the electric field between drain and source is very high, and channel electron can get sufficient speed and produce electron-hole pairs when the channel appears. For PMOS devices, channel holes can not get sufficient speed under the same electric field between drain and source and have the lower impact-ionization multiplication factor compared to those of electrons [15] is another factor. This phenomenon is more obvious when the channel is short for the same high $|V_{DS}|$. The abnormal phenomenon prohibits the use of small NMOS devices in the saturation region for extremely low-power circuits.

Compared with [11, Fig. 12], the hysteresis also occurs for the thick TOX NMOS (W/L = 10μm/0.6μm, 10μm/0.5μm), however the hysteresis does not obviously occur for the thin TOX NMOS (W/L = 10μm/10μm).

B. OUTPUT CHARACTERISTICS AND KINK EFFECT

We have plotted in Fig. 4(a-d) the output characteristics of thin and thick TOX MOSFET devices, obtained at sub-kelvin temperature. We choose the current-limiting method to keep the temperature stable. These curves (forward and backward scan) in Fig. 4 show the kink effect. The kink effect can occur on MOSFET devices at sub-kelvin temperatures when the $|V_{DS}|$ becomes sufficiently high [16]. For bulk silicon NMOS devices at low temperatures, channel electron

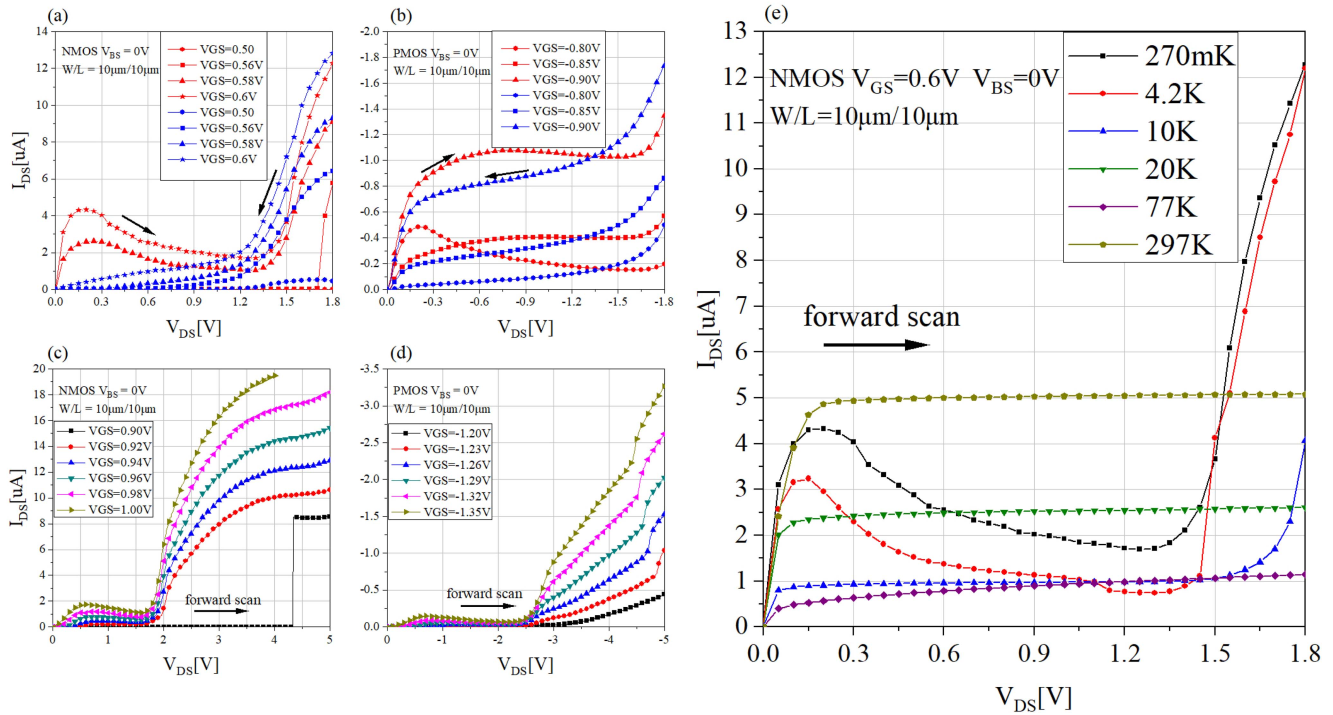

FIGURE 4. (a,b) Output characteristics of thin TOX MOS at sub-kelvin temperature, the forward(backward) scan data is represented by red(blue) lines and dots. (c,d) Output characteristics of thick TOX MOS at sub-kelvin temperature with forward scan. (e) Output characteristics of the large thin TOX NMOS device(W/L = 10μm/10μm) at temperatures from 297K down to 270mK, $V_{DS} = 0V \rightarrow 1.8V$ step=50mV, $V_{GS} = 0.6V$, $V_{BS} = 0V$, delay time=0s.

can gain enough energy and produce electron-hole pairs by impact ionization when the V_{DS} is higher than a certain value. The electrons pass through the channel to the drain, and the holes migrate towards the floating substrate. The floating substrate potential increases due to the accumulation of holes, until the substrate-source junction forms forward bias [16], [17]. The V_{th} reduces with the increase of substrate potential. As the $|V_{DS}|$ increases, the V_{th} decreases, leading to increased drain-source current (I_{DS}).

Compared to PMOS devices, the kink effect in NMOS devices appears at lower $|V_{DS}|$ voltage, and the amplification of NMOS is bigger. Considering the higher impact-ionization multiplication factor of electrons compared to that of holes, NMOS devices are more affected at sub-kelvin temperature compared to PMOS devices.

I_{DS} under forward scan is larger than I_{DS} under back scan at small V_{DS} in Fig. 4(a), the opposite is true at large V_{DS}. A similar phenomenon occurs for PMOS in Fig. 4(b). Besides, we observed the current overshoot phenomenon in Fig. 4 using the forward scan. For forward scan results of thin TOX PMOS, the current overshoot occurs obviously while the test begins. The kink effect and current overshoot phenomenon at cryogenic temperatures are related to varying V_{th} with V_{DS}. As shown in Fig. 4(e), the kink effect and current overshoot phenomenon attenuate and disappear with the temperature increasing.

Moreover, the curve for $V_{GS} = 0.9$ V in Fig. 4 (c) has a strange behavior, I_{DS} increases sharply from a few pA to 8.5uA. When V_D is large enough, the frozen carriers are activated. The PN junction between the drain and the substrate is under reverse bias, and an avalanche breakdown occurs, causing the above behavior.

C. CURRENT OVERSHOOT AND DISCUSSION

The current overshoot phenomenon occurred in Fig. 4(e) at temperatures below 10K other than 15K [18] or 25K [19]. This phenomenon is related to the charge state of traps in the Si/SiO_2 interface. The Si/SiO_2 interface traps are silicon dangling-bonds at the interface. In the case of on state NMOS devices (forward scan), it can be seen that positive charging of traps leads to the noticeable increase of the current at the beginning of the curves in Fig. 5(a). The V_{th} decreases in the linear region for NMOS devices owing to the positive charge trapped in the interface traps. When $|V_{DS}|$ is sufficiently high after reaching pinch-off point, the trapped charges in the interface can be released at sub-kelvin temperature [18]. The V_{th} increases and the amplitude of I_{DS} curves decreases in the saturation region with the increasing $|V_{DS}|$, as shown in Fig. 5(a,b).

We measured the current overshoot with various delay times and two scan models. In Fig. 5(c), the maximum amplitude of curves is 7.59μA for 0s delay time, and the peak value decreases when the scan delay time increases. Predictably, the peak will disappear at the sufficient scan delay time. We do not observe the current overshoot in Fig. 5(d), plotted results with backward scan model. For PMOS devices, the current overshoot phenomenon also occurred at sub-kelvin temperatures in Fig. 5(e,f). The

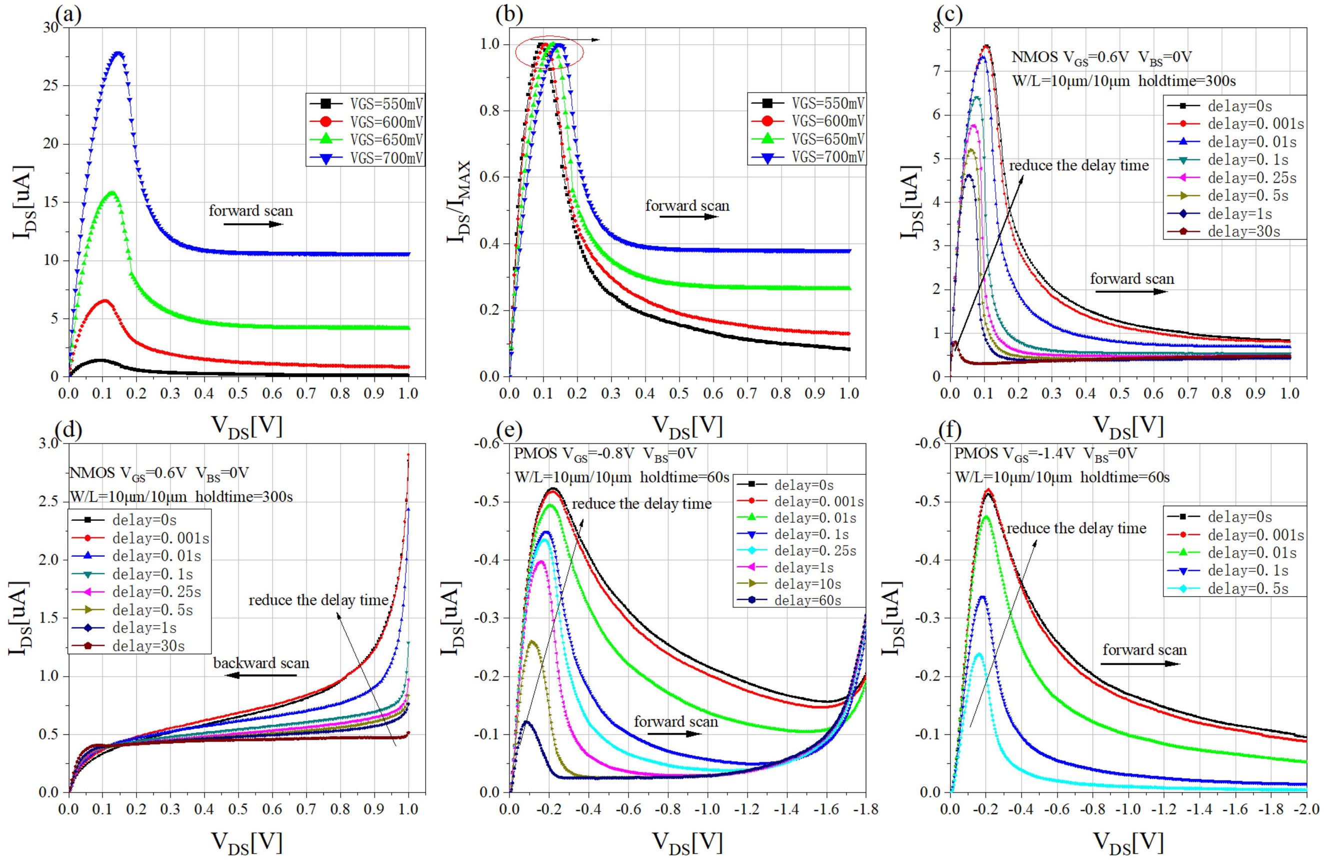

FIGURE 5. Current overshoot phenomenon in the thin TOX NMOS (a-d) device(W/L = 10μm/10μm) and PMOS (e,f) devices(W/L = 10μm/10μm) and at sub-kelvin temperature. (a) I_{DS}-V_{DS} curves for different V_{GS}; (b) I_{DS}/I_{MAX}-V_{DS} curves, normalized by I_{MAX} which is the maximum current for each curves in (a); (c) forward scan with different delay time; (d) backward scan with different delay time; (e) forward scan for the large thin TOX PMOS device with different delay time; (f) forward scan for the large thick TOX PMOS device with different delay time.

relation between the current overshoot phenomenon and the scan delay time implies the charge state of traps in the Si/SiO_2 interface [10], [18]. Self-heating is another explanation of current overshoot, however, these results do not support this explanation.

IV. MODELING

A. EKV MODEL FOR LARGE DEVICES

The EKV MOSFET model is appropriate to MOSFET devices in low-voltage and low-current applications [20]. And this model is compact and accurate with a few parameters [21], [22]. We choose the EKV 2.6 model to describe transfer characteristics of thin TOX large MOSFET devices for the following reasons. First, the output characteristics of MOSFET devices are abnormal at sub-kelvin temperature because of the kink effect and current overshoot. Second, the data of thick TOX large devices is insufficient due to the inequality between the test data and the current limit value caused by the limitation of the cooling power. For large MOSFET devices, the intrinsic model parameters in Table 2 can describe their transfer characteristics accurately, while their short and narrow channel effects are ignored. The value of parameters in Table 2 is for thin TOX PMOS devices.

TABLE 2. The intrinsic model parameters.

Name(unit)	Description	Value
TOX(m)	oxide thickness	4.27e-009
XJ(m)	junction depth	1.6e-007
DW(m)	channel width correction	-1.6e-008
DL(m)	channel length correction	7.6e-008
NSUB(cm^{-3})	channel doping	1.0196e+017
UCRIT(V/m)	longitudinal critical field	2.0e+6
VTO(V)	nominal threshold voltage	-
KP(A/V^2)	transconductance parameter	-
GAMMA($\sqrt{V}$)	body effect parameter	-
THETA($1/V$)	mobility reduction coefficient	-

Parameters of TOX, XJ, DW, DL, and NSUB are from BSIM4 model [23], and the parameter UCRIT can be set as default. The value of PHI(bulk Fermi potential) parameter is calculated with NSUB parameter. The value of T_{nom} is -272.88K (270mK), which is the nominal temperature of model parameters. We ignore the intrinsic parameters temperature dependence in the EKV model because T_{nom} is set as 270mK equal to test temperature. Equations of interest

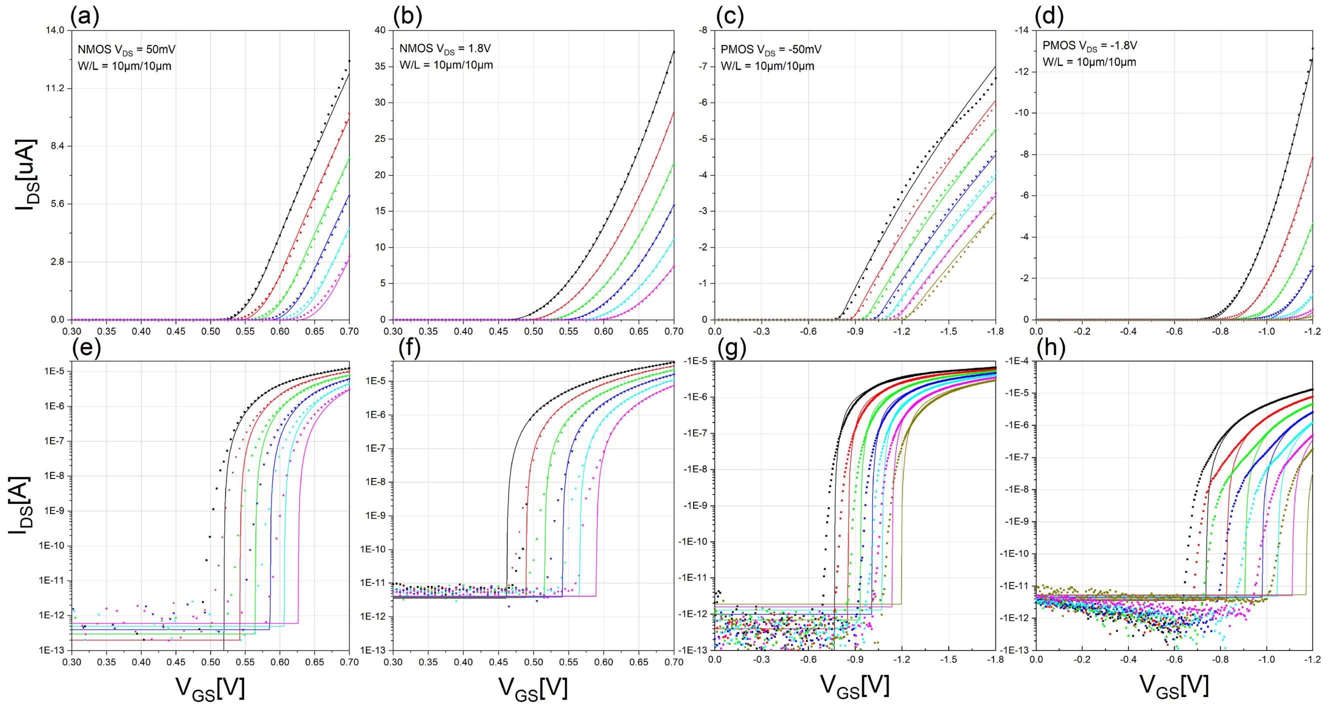

FIGURE 6. I_{DS}-V_{GS} **curves of large thin TOX NMOS (a,b,e,f) and PMOS (c,d,g,h) devices at sub-kelvin temperature measured (symbols) and simulated (solid lines). The bias condition is same to 1. Model parameters are given in Table 3 (NMOS) and Table 4 (PMOS).**

are presented below [22], [24], [25].

$$PHI = 2V_t \times \ln\left(\frac{NSUB \times 10^6}{n_i(T_{nom})}\right) \quad (1)$$

where $n_i(T_{nom})$ is intrinsic carrier concentration,

$$V_t = \frac{kT}{q} \quad (2)$$

The expression of I_{DS} is

$$I_{DS} = I_F - I_R \quad (3)$$

I_F is the forward current and I_R is the reverse current as given by the following formula.

$$I_{F(R)} = I_S \times \ln^2\left[1 + \exp\left(\frac{V_G - VTO - nV_{S(D)}}{2nV_t}\right)\right] \quad (4)$$

where the specific current

$$I_S = 2n\beta V_t, n = 1 + \frac{GAMMA}{2\sqrt{V_p + PHI + 4V_t}} \quad (5)$$

Considering the mobility reduction due to vertical field,

$$\beta = KP \times \frac{L_{eff}}{W_{eff}} \times \frac{1}{1 + THETA \times V_P} \quad (6)$$

where V_P is the pinch-off voltage for large devices.

B. PARAMETERS EXTRACTION AND MODELING

The parameters extraction was performed by BSIMProPlus with semi-empirical methods. We imported the test data of thin TOX large MOSFET devices into the software and set value of TOX, XJ, etc. The degree of agreement described as RMS (root-mean-square) Error between the simulation data and the test data changed with VTO, KP, GAMMA and THETA. After these parameters had been adjusted properly, the RMS Error declined to less than 5% (Fig. 6). The RMS Error calculation is shown in Eq. (7).

$$RMS\,Error = \sqrt{\frac{1}{N} \times \sum_{i=1}^{n}\left(\frac{I_{measi} - I_{calci}}{I_{threshold}}\right)^2} \times 100 \quad (7)$$

where N is the number of data, I_{measi} is measured data and I_{calci} is simulated (extracted) data. $I_{threshold}$ can be easily changed to reflect good or bad results. The value of $I_{threshold}$ is set to the maximum measured value according to the BSIMProPlus manual.

The value of |VTO| in Table 3 and Table 4 decreases from linear region to saturation region, which means that the $|V_{th}|$ of large devices varies with operating modes. This explains the kink effect. Comparison between the values of parameters in the linear region with those in the saturation region, shows that the numerical difference of NMOS is greater than that of PMOS. This proves that NMOS devices are more affected at sub-kelvin temperature compared to PMOS devices.

TABLE 3. Parameters for the large thin TOX NMOS device.

Region	linear	saturation
VTO(V)	0.5208	0.46403
GAMMA($\sqrt{V}$)	0.50534	0.6024
KP(A/V^2)	0.0017217	0.0017958
THETA($1/V$)	0.462	0.31198
RMS(%)	1.05	0.19

TABLE 4. Parameters for the large thin TOX PMOS device.

Region	linear	saturation
VTO(V)	-0.7676	-0.74
GAMMA($\sqrt{V}$)	0.66736	0.675
KP(A/V^2)	0.00018393	0.0001806
THETA($1/V$)	0.32242	0.37118
RMS(%)	1.52	0.38

V. CONCLUSION

The SMIC 0.18μm bulk CMOS technology is tested and characterized at sub-kelvin temperature. It is demonstrated that standard bulk CMOS devices can still operate at sub-kelvin temperature. The kink effect and current overshoot phenomenon have been shown and explained. A compact model has been proposed based on the EKV2.6 model to describe transfer characteristics of thin TOX large devices at 270mK. The accuracy of the model in the subthreshold region can be further optimized. This work contributes to the research on the characteristics of devices and the design of cryogenic CMOS circuits for quantum chips. Further research will be aimed at determining the relationship between current overshoot and delay time and modeling output characteristics of large devices.

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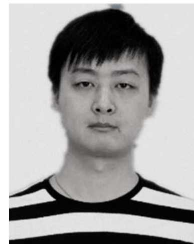

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