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Third Generation PRESiCE™ Technology for Manufacturing SiC Power Devices in a 6-Inch Commercial Foundry

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This work was supported by DOE and PowerAmerica to create a non-proprietary process for manufacturing SiC power devices at a commercial foundry to promote commercial adoption of SiC power devices.

ABSTRACT A third-generation PRESiCE™ technology has been qualified for manufacturing SiC power devices in a commercial foundry using 6 inch wafers. JBS diodes, power MOSFETs, and JBSFETs with 1.2 kV ratings were fabricated using this technology with good yields. Conventional device structures similar to commercially available products were used in this work to perform the process qualification. Extensive measurements on devices from three process qualification lots demonstrate excellent parametric distributions within a wafer, between wafers within a lot, and between wafers from the three lots. The electrical characteristics of the JBS diodes, power MOSFETs and JBSFETs manufactured with PRESiCE™ are similar to those of commercial products.

INDEX TERMS Silicon carbide, 4H-SiC, MOSFET, JBSFET, JBS diode, wafer maps, parametric distributions, wafer lots, manufacturing technology, yield.

I. INTRODUCTION

Rently, silicon carbide (SiC) power devices have become commercially available because this material has a high avalanche breakdown field, high mobility for electrons, and better thermal conductivity than silicon [1]. SiC power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) with 1.2 kV ratings have been commercialized to reduce switching losses by replacing Si IGBTs. They enable reduction of passive component size, weight, and cost in applications such as photovoltaic and electric vehicle inverters. A higher manufacturing cost relative to Si IGBTs for SiC power MOSFETs remains an impediment to market adoption. Manufacturing cost reduction is achievable for SiC power devices by utilizing high volume Si foundries. Most (up to 80 %) of the process steps for SiC power MOSFETs are already available in a Si foundry. They require upgrading with higher temperature equipment for gate oxidation and ion-implant annealing tailored for SiC material.

This strategy has been supported by the Department of Energy (DOE) sponsored PowerAmerica Institute at the X-Fab foundry located in Lubbock, TX. Many companies have ported their previously developed proprietary SiC power device manufacturing process flow to X-Fab for building commercial products since 2015 [2], [3]. Other companies interested in entering the SiC power device market without SiC power device process know-how have been precluded from entering the market. Cost reduction can be achieved by generating greater wafer volume at a foundry. This can be enabled by a non-proprietary process at the foundry that can be utilized by more companies to manufacture their products. Such process technology was engineered by North Carolina State University (NCSU) in 2016 with the support of PowerAmerica for manufacturing SiC power devices at X-Fab. Improvements to the process were then achieved in subsequent years to reduce the cost of wafer fabrication.

SiC Junction Barrier controlled Schottky (JBS) rectifiers and power MOSFETs are now available as commercial products from many companies. Their cross-sections are illustrated in Fig. 1. The JBS diode is a Schottky rectifier with an integrated P^+ region to shield the contact [4]. This approach greatly reduced the leakage current in the reverse blocking mode allowing commercialization of devices. The SiC power

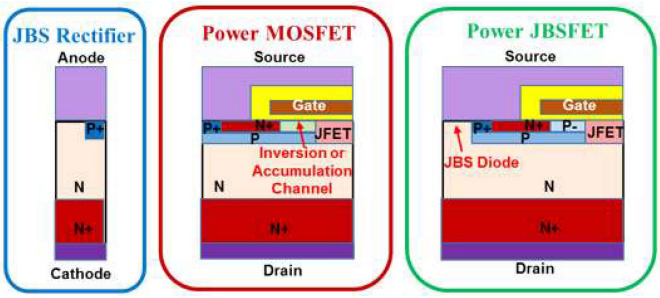

FIGURE 1. Three types of SiC power devices that can be manufactured using the Gen-3 PRESiCE™ technology.

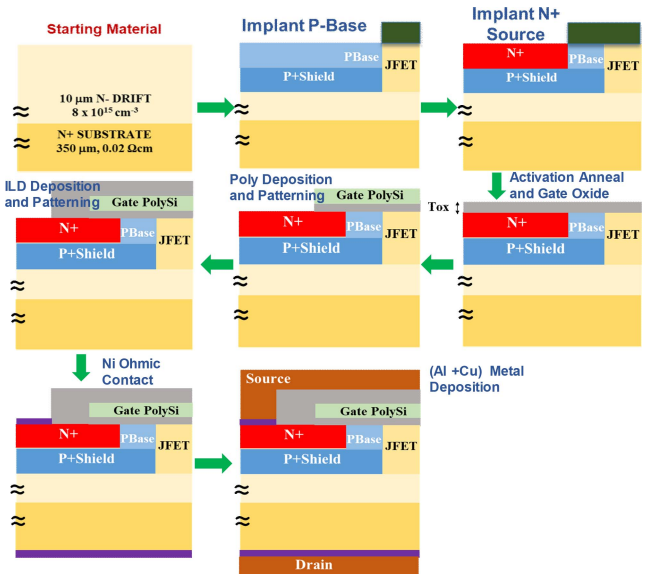

FIGURE 2. PRESiCE™ technology process sequence for manufacturing the SiC power MOSFETs.

MOSFET structure shown in Fig. 1 contains a P-shielding region to suppress reach-through breakdown. It also creates a potential barrier in the JFET region to reduce the electric field in the gate oxide allowing reliable operation [4]. To the author's knowledge, commercially available products use this structure with an inversion-channel region. Reduced on-resistance has been experimentally demonstrated by using an accumulation-channel structure [5]. The Junction Barrier Schottky Field Effect Transistor (JBSFET), shown in Fig. 1, is a power MOSFET structure in which the JBS rectifier has been integrated to improve circuit performance and reduce cost [6], [7]. This is a new potential product under consideration by many companies. A detailed description of the electrical characteristics of the devices used for performing the process qualification in this paper has been published in previous papers and compared with other devices in the literature [5].

This paper describes a third-generation (Gen-3) process technology created by NCSU that allows manufacturing SiC JBS rectifiers, power MOSFETs, and JBSFETs. The Gen-1 technology, named PRESiCE™ for 'PRocess Engineered for manufacturing SiC Electronic-devices', was described in a previous publication [8]. Improvements to this technology were made by performing the hot ion-implant steps more uniformly using in-house equipment to create the Gen-3 technology.

II. MANUFACTURING PROCESS

A 10-mask process is used for the NCSU PRESiCE™ technology. The foundry design rules are 1.0 µm for the minimum feature size and an alignment tolerance of 0.2 µm. All the device structures were designed to satisfy these rules.

Fig. 2 illustrates the basic steps used for manufacturing SiC power MOSFETs with the PRESiCE™ technology. The illustrated ion-implant process steps shown in Fig. 2 are the P-base ion implant and the N^+ source implant that determine the channel length with a non-self-aligned process. In addition, the process includes the JTE ion-implant for the edge termination, the JFET ion-implant across the entire active area, and a P^+ contact ion-implant to the P^+ shielding region located orthogonal to the cross-section. They are not shown in Fig. 2 in the interest of space. The process qualification was performed for 1.2 kV rated devices by epi specification: drift region thickness = 10 µm and doping concentration = 8 x 10^{15} cm^{-3}. Hot ion-implantations were performed at 600°C with an oxide hard mask for the P-base and N^+ source regions. The implants were annealed at 1600°C with a carbon cap to activate the dopants. Despite using a non-self-aligned process with alignment tolerance of 0.2 µm, the yield and parametric distributions were excellent for 0.5 µm channel length devices as discussed in subsequent sections. A self-aligned process can also be used to make SiC power MOSFETs but its discussion is outside the scope of this paper.

The process for making the SiC JBSFETs has been previously described in detail [6], [7]. In this case, an opening is made to the middle of the polysilicon gate window where the N^+ source and P^+ shielding regions are excluded as shown in Fig. 1. A nickel contact metal layer is then used to simultaneously form a Schottky contact to the exposed drift region and ohmic contacts to the N^+ source and P^+ contact regions. The JBS diodes were fabricated with the cross-section shown in Fig. 1 using the P^+ contact region used in the power MOSFET structures.

III. PROCESS QUALIFICATION METHODOLOGY

Three consecutive process lots (Lot 1, 2 and 3) were manufactured at a commercial foundry X-Fab, TX, with identical process steps to qualify the Gen-3 PRESiCE™ process technology. A Signatone semi-automated probe station was used with a B1505 Keysight Curve Tracer to obtain extensive wafer-level data on all the devices on each wafer.

The JBS diode on-state voltage drop and leakage current were documented. For the power MOSFETs and JBSFETs, the on-resistance, threshold voltage, and gate-drain capacitance were acquired. In addition, the third quadrant voltage drop was obtained for the JBSFETs. Its value should be

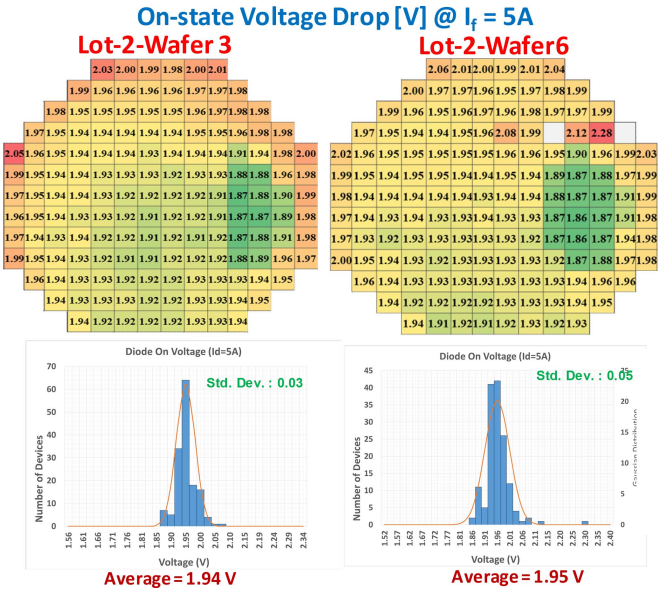

FIGURE 3. On-State Voltage Drop for SiC JBS rectifiers at 5 A: Within-Wafer and Wafer-to-Wafer-within-a-Lot distribution data.

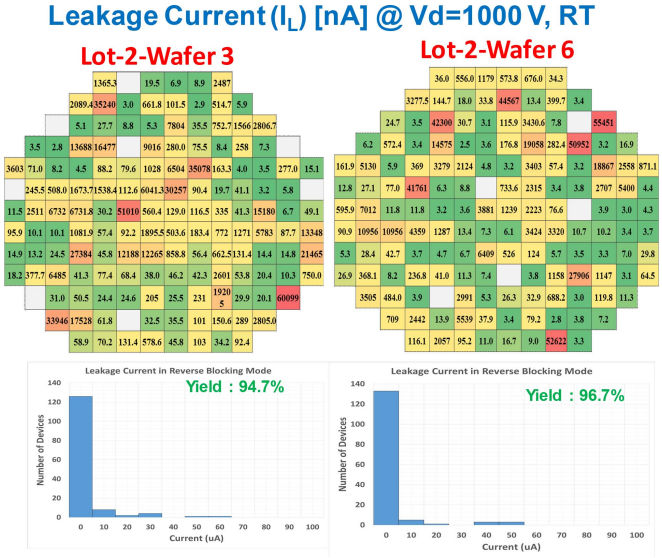

FIGURE 4. Leakage currents measured for SiC JBS rectifiers at 1000V reverse bias: Within-Wafer and Wafer-to-Wafer-within-a-lot variation.

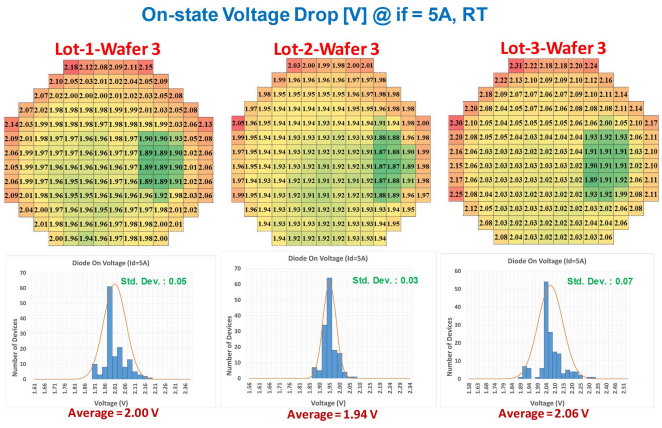

FIGURE 5. On-State Voltage Drop for SiC JBS rectifiers at 5 A: Lot-to-Lot variation.

less than 2.5 V to ensure inactivation of the P-N body-diode within the MOSFET structure. Wafer maps were created for each parameter to examine the yield. Statistical distribution of the measured parameters were plotted to document the average value and the standard deviation. The leakage current data provided in this paper is taken at 1000 V for the 1.2 kV rated devices. Very little change in leakage current is observed between 1000 V and 1200 V for the linear cell MOSFET devices discussed in this paper as shown in a previous publication [5]. It starts increasing rapidly beyond 1400 V.

The process qualification was achieved by examining the distribution for each device parameter: (a) within a wafer; (b) wafer-to-wafer within a lot; and (c) wafer-to-wafer from lot-to-lot. The parametric spread (typical and maximum or minimum values) given in commercial product datasheets served as the benchmark to determine the yield and quality of the process. A breakdown voltage above 1600 V was found for all the fabricated devices, well above the 1.2 kV rating, as demonstrated in the blocking characteristics shown in previous technical publications on these devices [5], [6]. The yield was not determined by this device parameter due to the hybrid-Junction Termination Extension (JTE) edge termination applied to all the devices [9].

IV. WAFER MAPS AND PARAMETRIC DISTRIBUTIONS

A. JBS RECTIFIERS

The JBS rectifier is a Schottky rectifier with a P-N junction, as shown in Fig. 1, used to suppress large leakage currents during the reverse blocking mode [4]. A nickel Schottky contact was used for the devices in this work.

Within-Wafer and Wafer-to-Wafer-Within-a-Lot Data: Wafer maps and statistical distribution data for the on-state voltage drop for JBS rectifiers are shown in Fig. 3 for two wafers from Lot 2. The distribution is uniform for each wafer. It has an average value of 1.94 V with a standard deviation = 0.03 V for the 150 devices measured on wafer 3. A similar very uniform distribution is observed across wafer 6 in Fig. 3 with an average value = 1.95 V and a standard deviation = 0.05 V for 150 devices on this wafer. Comparing the data from the two wafers, it can be concluded that the variation of the on-state voltage drop from Wafer-to-Wafer-within-a-Lot is also very small.

Fig. 4 shows wafer maps of the leakage currents measured at 1000 V for the JBS rectifiers on wafers 3 and 6 from Lot 2. Note that the values are given in nA. The statistical distribution of the leakage current is given below the wafer maps. The leakage current is low (well below 100 mA used in datasheets).

Lot-to-Lot Distribution Data: Data on the on-state voltage drop for the JBS rectifiers from one wafer from each of the three lots is shown in Fig. 5. A uniform distribution is

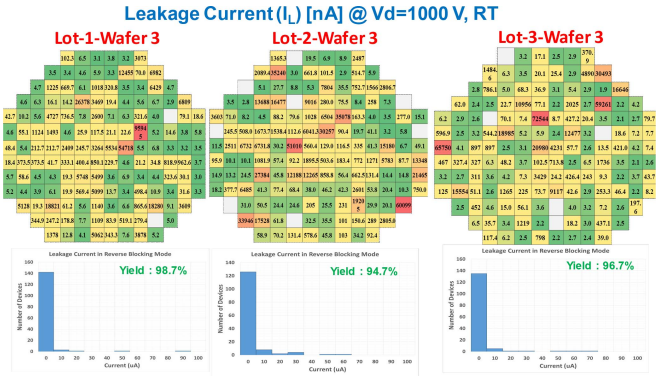

FIGURE 6. Leakage currents measured for SiC JBS rectifiers at 1000V reverse bias: Lot-to-Lot variation of Leakage Current.

observed for each wafer. The average values for the three wafers are 2.00 V, 1.94 V, and 2.06 V. A standard deviation of 0.03-0.07 V is observed for 150 devices on each wafer. It can be concluded from this data that Lot-to-Lot variations of on-state voltage drop are very small.

Leakage current (measured at 1000 V) maps for JBS rectifiers on wafers from the three lots are shown in Fig. 6. The statistical distribution of the leakage current is given at the bottom of the wafer maps. The leakage current is in the nA range, well below the 100 μA used in datasheets.

Summary: Based up on the measured data, the yield is found to be above 90 % for the JBS rectifiers manufactured using the Gen-3 PRESiCE™ technology. The leakage current for Schottky rectifiers is often a yield limiting factor. The leakage currents for JBS diodes made with the Gen-3 PRESiCE™ technology are well below the industry standard leakage current of 100 μA. The on-state voltage drop for these JBS diodes is about 2 V which is suitable for their use as antiparallel diode with Si Insulated Gate Bipolar Transistors (IGBTs) and SiC power MOSFETs. The Gen-3 PRESiCE™ technology can therefore be used to fabricate commercial JBS diode products in the foundry.

B. POWER MOSFETS

Since the 1.2 kV rated Power MOSFETs were found to have excellent breakdown voltages (> 1600 V) and low (nA range) leakage currents, these device parameters did not limit the yield. Consequently, the distributions for three other parameters (on-resistance, threshold voltage, and gate-drain capacitance) are reported here. Power MOSFET datasheets provide the typical value for on-resistance and a maximum value that is 30% greater. In the case of the threshold voltage, maximum and minimum values that are 30% above and below the typical value are also cited. For the gate-drain capacitance, just the typical value is given in datasheets. When qualifying the Gen-3 PRESiCE™ technology, these metrics were used to define the yield.

Within-Wafer and Wafer-to-Wafer-Within-a-Lot Data: Wafer maps for the on-resistance of SiC power MOSFETs are shown in Fig. 7 for two wafers from Lot 3. The statistical

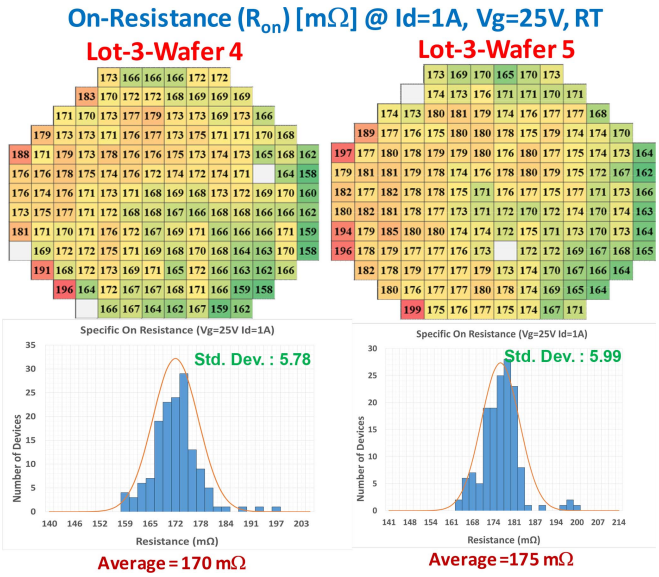

FIGURE 7. On-resistance measured for SiC power MOSFETs: Within-Wafer and Wafer-to-Wafer-within-a-Lot variation of On-Resistance.

distribution is shown below the wafer maps. The distribution observed for wafer 4 has an average value of 170 mΩ with standard deviation of only 6 mΩ for 150 devices. A similar tight distribution is seen for wafer 5 an average value of 175 mΩ for 150 devices. Considering the data from both wafers, it can be concluded that variations from Wafer-to-Wafer-within-a-Lot are acceptable.

The threshold voltage of a power MOSFET must be sufficiently large, typically >2 V, to prevent circuit voltage spikes from inadvertently turning on the devices. It must also be sufficiently low to allow using reasonable gate drive voltages, typically 20-25 V, for SiC power MOSFETs. Wafer maps for threshold voltage variation are shown in Fig. 8 for two wafers from Lot 3. The statistical distribution is shown below the wafer maps. The distribution is uniform across wafer 4: a standard deviation < 0.15 V with an average value of 3.94 V for the 150 MOSFETs. For wafer 5, the standard deviation is also < 0.15 V with an average value of 3.95 V for 150 MOSFETs indicating excellent uniformity within industry standards. Using the data from both wafers, it can be concluded that variations from Wafer-to-Wafer-within-a-Lot are also sufficiently low for manufacturing the MOSFETs.

In inverters used for EV motor drive applications, the switching losses are determined by the gate-drain capacitance (C_{GD}) of a power MOSFET. A smaller C_{GD} reduces the transition time for the drain voltage resulting in lower switching energy loss. Wafer maps for the C_{GD}, measured at a drain bias of 1000 V, are shown in Fig. 9 for two wafers from Lot 3. The statistical distribution is shown below the wafer maps. The C_{GD} for wafer 4 has a standard deviation < 0.6 pF with an average value of 10.38 pF for 150 MOSFETs. In the case of wafer 5, the standard deviation is < 0.3 pF with an average value of 9.90 pF for 150 MOSFETs. This confirms very

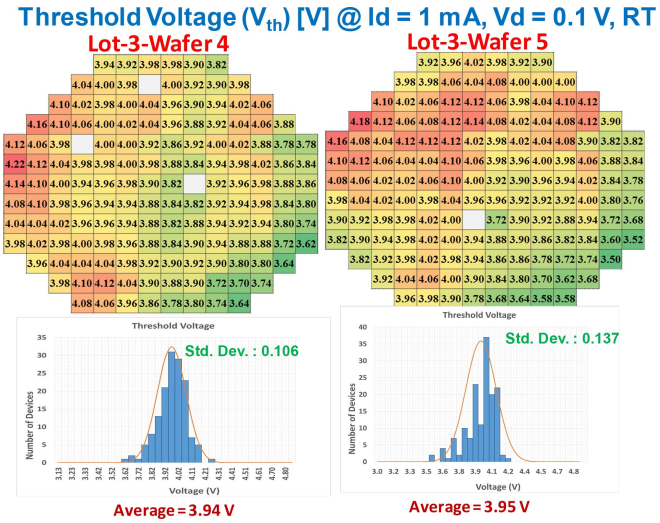

FIGURE 8. Threshold voltage measured for SiC power MOSFETs: Within-Wafer and Wafer-to-Wafer-within-a-Lot.

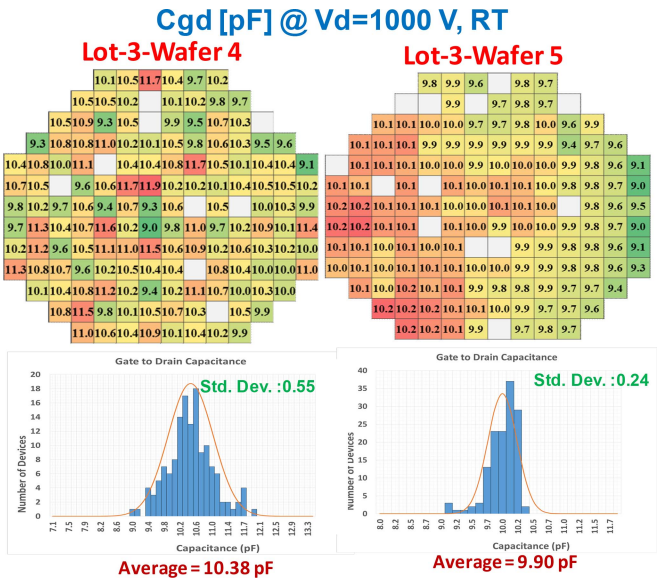

FIGURE 9. Gate-Drain Capacitance measured for SiC power MOSFETs: Within-Wafer and Wafer-to-Wafer-within-a-Lot.

small variations in the capacitance across a wafer. Using the data from the two wafers, it can be concluded that the C_{GD} variations from Wafer-to-Wafer-within-a-Lot are acceptable.

Lot-to-Lot Distribution Data: Wafer maps of the on-resistance of the SiC power MOSFETs measured for wafers from three lots are shown in Fig. 10. The corresponding statistical distribution is provided below the wafer maps. The distribution is very uniform within each wafer. The average values are 181 mΩ, 164 mΩ, and 175 mΩ for the three wafers, with a standard deviation < 6 mW for 150 MOSFETs on each wafer. The data confirms that on-resistance variations on wafers from three Lots fall within the specifications in datasheets and are therefore not a yield limiting factor.

Wafer maps of the threshold voltage variation of SiC power MOSFETs for wafers from three lots are shown in

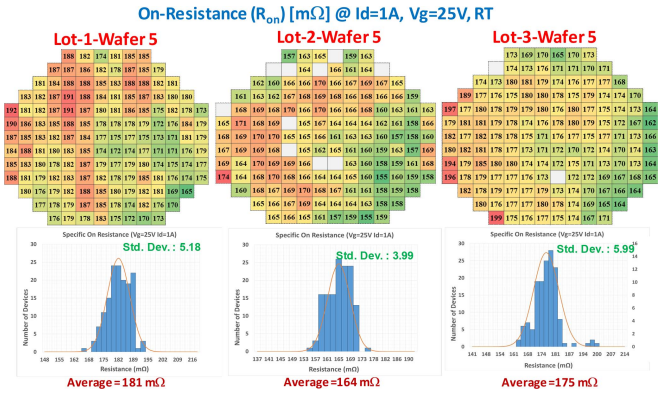

FIGURE 10. On-Resistance measured for SiC power MOSFETs: Lot-to-Lot variation.

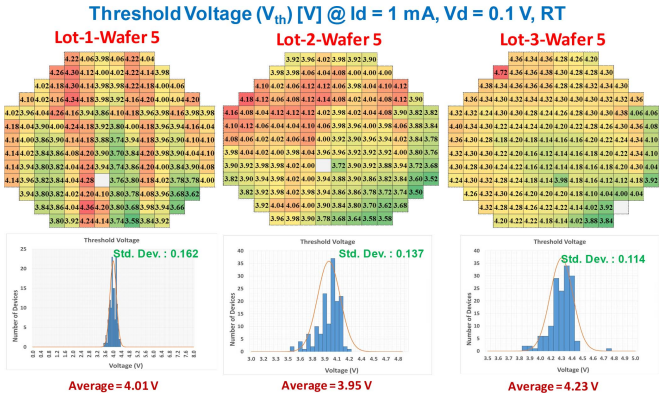

FIGURE 11. Threshold Voltage measured for SiC power MOSFETs: Lot-to-Lot variation.

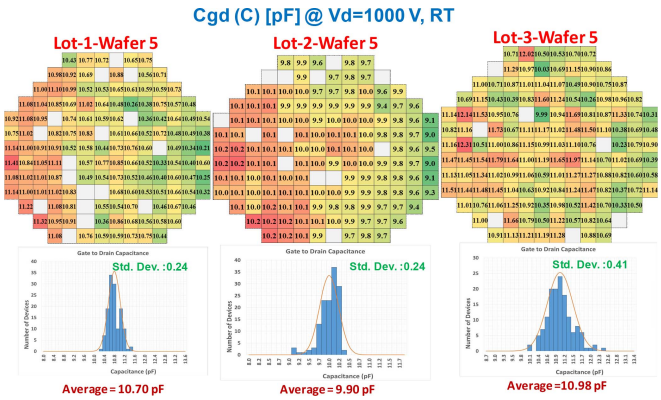

FIGURE 12. Gate-Drain Capacitance measured for SiC power MOSFETs: Lot-to-Lot variation.

Fig. 11 with the statistical distribution below each wafer map. There is very little variation from lot to lot: a standard deviation < 0.2 V with an average value of 4.0 V for 150 MOSFETs on each wafer. From this data. It can be concluded that Lot-to-Lot threshold voltage variations are not a yield limiting factor.

Wafer maps and statistical distributions of the gate-drain capacitance (C_{GD}) are shown in Fig. 12 for wafers from three

lots. A very uniform distribution is observed from Lot-to-Lot: a standard deviation < 0.5 pF with an average value of about 10 pF for 150 MOSFETs within each wafer. This parameter is therefore not a yield limiting factor.

Summary: From the measured data on power MOSFETs manufactured using the PRESiCE™ technology, it can be concluded that the maximum on-resistance for 90 % of the devices are less than 1.3x of the typical value, demonstrating a yield of above 90%. The threshold voltage for the SiC power MOSFETs is within +/−30 % of the typical value as required by datasheets.

C. POWER JBSFETS

The JBS diode and MOSFET structures discussed in the previous sections have been integrated into a single monolithic device called the JBSFET [6], [7]. The JBSFET cross-section, shown in Fig. 1, contains a JBS diode formed by making a gap in the P-shielding region. A Schottky contact is made to the drift region using Nickel metallization silicided at 900°C. The process simultaneously makes good ohmic contacts to the P^+ and N^+ regions. The Schottky contact size is optimized to achieve an on-state voltage drop of below 2.5 V in the third quadrant to by-pass the P-N body diode in the MOSFET while avoiding large leakage current in the blocking mode.

The on-resistance of the JBSFET is larger than that of the MOSFET for the same die size due to a reduced channel density. To compensate for this, an accumulation-channel was used instead of the inversion-channel in the MOSFETs. The accumulation layer mobility has been found to be 30 % larger than the inversion layer mobility in 4H-SiC MOSFETs [5]. Process qualification was performed like discussed for the power MOSFET in the previous section. This paper reports distributions for the on-resistance, threshold voltage, leakage current, and third quadrant on-state voltage drop for accumulation-channel JBSFETs. The capacitance distributions for JBSFETs are not shown because they resemble those discussed in the previous section for the power MOSFETs.

Lot-to-Lot Distribution Data: Wafer maps and statistical distributions of the on-resistance for the SiC power JBSFETs are shown in Fig. 13 for wafers from three lots. The average values are 250 mΩ, 232 mΩ, and 268 mΩ for the three wafers. The on-resistance is uniform within each wafer. The standard deviation is < 20 mΩ for 150 JBSFETs on each wafer. From the data, it can be surmised that variations in on-resistance from Lot-to-Lot are very small and that this is not a yield limiting factor.

Wafer maps of the threshold voltage for the SiC power JBSFETs are shown in Fig. 14 for wafers from three lots. The average value for the threshold voltage for accumulation-channel devices is smaller than for inversion-channel devices. The distribution is very tight from Lot-to-Lot with a standard deviation of about 0.1 V from an average value of 2.4 V for 150 JBSFETs in each wafer. From the data, it can be surmised that threshold voltage variations from Lot-to-Lot

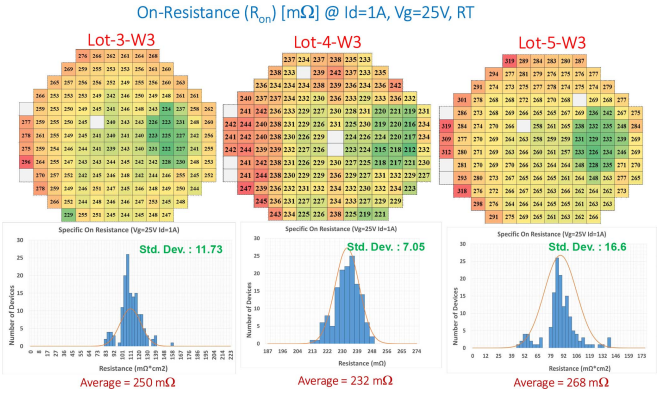

FIGURE 13. On-Resistance measured for SiC power JBSFETs: Lot-to-Lot variation.

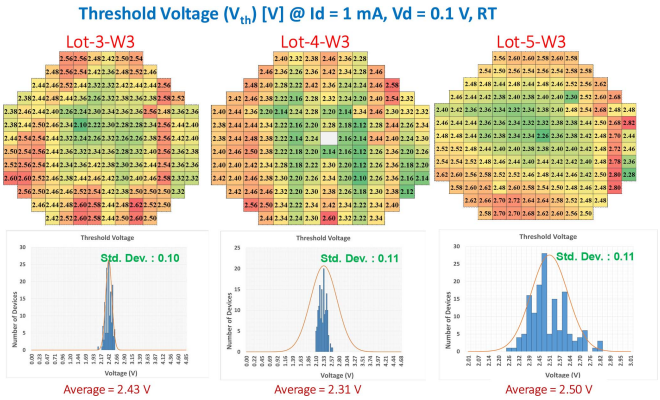

FIGURE 14. Threshold Voltage for SiC power JBSFETs: Lot-to-Lot variation.

are very small and that this parameter is not a yield limiting factor.

Schottky diodes are well known to produce high leakage currents when blocking large voltage [10]. This problem is particularly severe for SiC devices due to large Schottky barrier lowering and tunneling effects. The shielding of the Schottky contact by the P^+ regions is critical to suppressing the leakage current in products. Consequently, the leakage current can become the yield limiting factor in JBSFETs due to the integrated Schottky contact.

The purpose for integration of the JBS diode into the power MOSFET structure is to provide a path for current to by-pass the body-diode in the third quadrant. This requires designing the JBS diode such that its on-state voltage drop is below 2.5 V, which is significantly below the 3.5 V required to obtain current flow via the body diode. Wafer maps and statistical distributions for the on-state voltage drop in the third quadrant are shown in Fig. 15 for wafers from three lots. The average on-state voltage ranges from 2.2 to 2.4 V ensuring that the body-diode activation is suppressed.

Wafer maps and statistical distributions of leakage current at 1000 V for JBSFETs are shown in Fig. 16 for wafers from three lots. It can be observed from the data that the magnitude of the leakage current is in the nA range, well below typical datasheet specifications of 100 μA, in spite

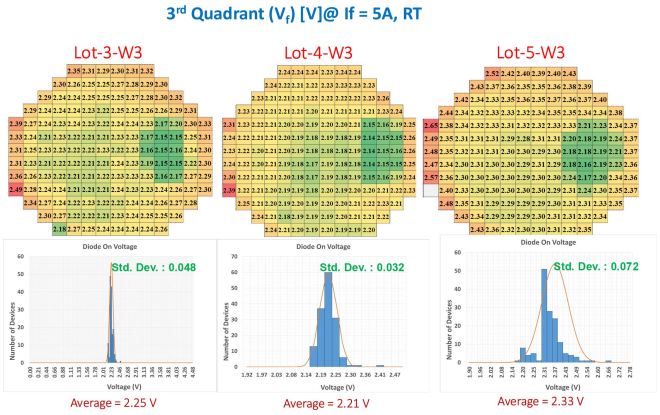

FIGURE 15. SiC power JBSFETs manufactured using Gen-3 PRESiCE™ technology: Lot-to-Lot variation of 3rd Quadrant Voltage Drop.

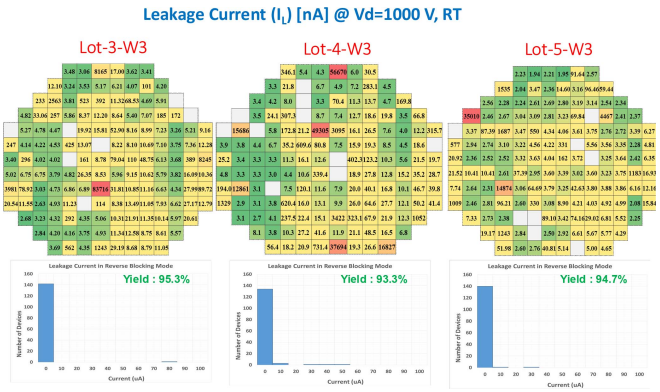

FIGURE 16. SiC power JBSFETs manufactured using Gen-3 PRESiCE™ technology: Lot-to-Lot variation of Leakage Current.

of integration of the JBS diode. This outcome is achieved with the proper choice of the width of the Schottky contact within the JBSFET cells. The yield is found to be above 90 % for the JBSFETs

Summary of SiC power JBSFET Distribution Data: The above data demonstrates that the PRESiCE™ technology is capable of producing SiC JBSFETs with maximum on-resistance well within the 30% limit, with yields above 90%. The threshold voltage variation for these SiC power JBSFETs falls within the +/− 30% of the typical value. The third quadrant current flow via the integrated JBS diode keeps the on-state voltage drop below 2.5 V as desired while simultaneously not incurring a high leakage current through the Schottky contact. These features meet the criteria for manufacturing SiC JBSFET products.

V. CONCLUSION

A third-generation PRESiCE™ technology has been developed by NCSU at a 6 inch commercial foundry, X-Fab, to manufacture 1.2 kV SiC JBS rectifiers, power MOSFETs, and JBSFETs. This technology was developed over a three year time frame with funding from the PowerAmerica Institute created by the Department of Energy in 2015. The Gen-3 technology was qualified by running three consecutive process lots. The wafer maps and parametric distributions obtained for the fabricated devices show excellent control of uniformity across each wafer, from wafer-to-wafer within a lot, and wafer-to-wafer from lot-to-lot. The overall yield for the all the different types of devices manufactured using the PRESiCE™ technology exceeds 90 % at a die size of 3 mm x 3 mm. These excellent results were achieved by using strict process control protocols at the foundry and by using all in-house processes compared with performing the hot ion-implants at an external service. A shorter version of this paper was published at the EDTM 2020 conference [11].

ACKNOWLEDGMENT

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