Received 15 April 2020; revised 5 July 2020 and 29 July 2020; accepted 2 August 2020. Date of publication 4 August 2020; date of current version 18 August 2020.
The review of this article was arranged by Editor S. Reggiani.

Digital Object Identifier 10.1109/JEDS.2020.3014252

Design and Simulation of High Performance Lattice Matched Double Barrier Normally Off AlInGaN/GaN HEMTs

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This work was supported in part by the Ministry of Science and Technology, Taiwan, under Grant MOST 108-2221-E-009-008 and Grant MOST 108-3017-F-009-001, and in part by the "Center for mmWave Smart Radar Systems and Technologies" under the Featured Areas Research Center Program within the framework of the Higher Education Support Project by the Ministry of Education in Taiwan.

ABSTRACT A novel lattice matched double barrier $Al_{0.72}In_{0.16}Ga_{0.12}N/Al_{0.18}In_{0.04}Ga_{0.78}N/GaN$ normally-off high electron mobility transistor (HEMT) is designed and simulated by solving a set of thermodynamic transport equations. Using the experimentally calibrated physical models with bearing mobility degradation by surface roughness in account, the recess gate and double barrier of the proposed device achieves a maximum drain current density ($I_{D,max}$) of 1149 mA/mm and a maximum transconductance ($g_{m,max}$) of 358 mS/mm with a positive threshold voltage (V_{th}) of 0.2 V. The small polarization charge of first barrier is responsible for positive V_{th}. $I_{DS,max}$ in the double barrier HEMT at high gate bias condition is due to injection of electrons from upper 2DEG which is almost impossible at lower gate voltage because of insufficient energy to cross the barrier. The injection of electrons is further supported by the second peak in the g_m curve at low gate bias $V_G = 1$V. The outcome of this study suggests that the proposed device will be beneficial for high-frequency and high-power electronic applications.

INDEX TERMS AlInGaN, double barrier, gate recess, lattice matched, normally-off HEMT, mobility, power amplifier, resistance, threshold voltage, transconductance.

I. INTRODUCTION

Gallium nitride (GaN) based high electron mobility transistors (HEMTs) have made substantial progresses in diverse applications, such as wireless communications, satellite communications, and radar systems [1]. AlGaN/GaN HEMTs are promising to fulfill the demand of high-output-power density for extending the detection range in advanced communications and radar systems. They are able to achieve extremely high-power density of 51 W/mm in the L-band and 40 W/mm in S-band [2]. Currently, AlInGaN barrier has been considered as an effective way to boost the 2DEG density and improve the drain current density and transconductance (g_m) because of its low sheet resistance and large spontaneous polarization. The reduced sheet resistance, high sheet carrier density and high electron mobility of the quaternary AlInGaN barrier come up with higher output power density in GaN-based HEMT [3]. Simultaneously, a thinner barrier layer helps to strengthen the gate modulation capability which results in suppressing the short-channel effect. Hence, AlInGaN barrier is useful to improve the operational frequency of devices [4]. Although ornamented by plethora of crucial high performance outcomes, normally-on operation is one of the fundamental limitations of GaN-based HEMTs. This shortcoming limits device characteristics for practical applications [5] because power switching applications demand normally-off transistors to

TABLE 1. List of the adopted device parameters.

	Calibrated Sample	Sample I	Sample II
Al composition %	73	31	18 (1st barrier) 72 (2nd barrier)
In composition %	12	7	4 (1st barrier) 16 (2nd barrier)
Gate Length (nm)	160	160	160
Gate drain space (μm)	2	2	2
Barrier thickness (nm)	8.5	8.5	8.5 (1st barrier) 5 (2nd barrier)
Recess depth (nm)	-	-	9
GaN thickness (μm)	1.9	1.9	1.9
Spacer layer thickness (nm)	1.24	1.24	1.24
Cap layer thickness (nm)	2	2	2

guarantee a safe and low-cost operation in power electronic systems [6]. Various techniques, such as use of recess gate [7], fluoride ion implantation [8], *p*-type gate material [9] and cascade [10] have been applied to obtain normally-off HEMTs. Unfortunately, the above mentioned normally-off HEMTs have been encountered with drastic reduction of current density which is detrimental to the performance of devices [11].

In this work, lattice matched double barrier devices are computationally studied in order to improve the current density and transconductance of the GaN-based HEMT. Additionally, the second barrier is modified in order to make device operated in normally-off mode. The device has been designed in such a way that both AlInGaN barriers are lattice matched with GaN.

II. DEVICE STRUCTURE AND METHODOLOGY

Since validation of the models is indispensable to know the accuracy of output results, the experimental outcomes from AlInGaN/GaN HEMT are first used to calibrate the physical and transport simulation models. Schematics of the AlInGaN/GaN HEMT used to validate the simulation results is shown in Fig. 1(a). The details of adopted device parameters are listed in Table 1. The calibrated parameters of the physical models are used to study the electrical characteristic of the single barrier $Al_{0.36}In_{0.08}Ga_{0.56}N$/GaN HEMT (Sample I), and the proposed double barrier $Al_{0.72}In_{0.16}Ga_{0.12}N/Al_{0.18}In_{0.04}Ga_{0.78}N$/GaN HEMT with a 9-nm-thick recess gate (Sample II) which are shown in Figs. 1(b) and (c), respectively. The growth is initiated with 1.3 mm AlGaN buffer and 1.9 mm an unintentionally doped GaN layer. An AlN spacer layer (1.24 nm) is deposited to enhance the electron mobility by minimizing the alloy disorder scattering and increase the 2DEG carrier density. Finally, 2 nm GaN cap layer is deposited after 8.5 nm InAlGaN barrier is grown. The brief fabrication process is described in Fig. 1(c). The fabrication is started with defining the active area of the devices and then it is isolated by etching it down to the buffer layer. Then, Ti/Al/Ni/Au multilayered ohmic contacts are promptly deposited. The contacts are then annealed at a high temperature to prevent reaction of

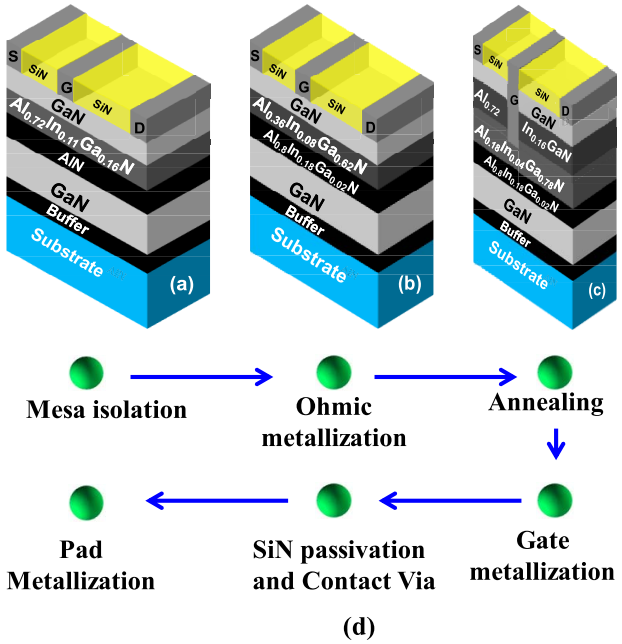

FIGURE 1. Schematic plots of (a) calibrated AlInGaN/AlN/GaN, (b) the single barrier HEMT (Sample I), (c) the double barrier HEMT (Sample II), and (d) a process flow.

deposited metal with the surface which ensures that a low-resistance contact is made to the 2DEG. After annealing, Ni/Au gate metals are then formed by depositing a passivation dielectric layer in the channel area and etching a slot for the gate contact. The gate contact metal Schottky contact is formed by e-beam deposition. Then metallization of contact pads is done. Finally, the SiN passivation layer is deposited to avoid current slump and degradation of properties of fabricated devices as well as to increase performance. The adopted structural parameters are listed in Table 1.

To estimate the electrical characteristic of the device, a set of semiconductor transport equations consisting of the Poisson equation, the electron and hole current continuity equations are solved numerically together with the self-heating equation, where the polarization, the high-electric-field saturation, and the mobility degradation due to impurity and other scattering are considered properly. Furthermore, barrier tunneling, the interface fixed charge at the interfaces between the barrier layer and nitride layer and the acceptor buffer trap at GaN buffer are also activated. Additionally, thermionic current is calculated at high bias condition by using thermionic emission model. Since barriers are polarization matched with GaN, the piezoelectric polarization was neglected in double barrier HEMT due to lattice matched barrier. Similarly, recess gate is addition technology used in proposed HEMT, mobility attributed to surface roughness scattering was additionally solved with high priority. The details of mobility parameters used during simulation are listed in Table 2 and dependency of mobility of the device on surface roughness and correlation length were explained in our earlier works [13]–[14]. Since ohmic contact resistance plays a vital role in the device performance, low ohmic

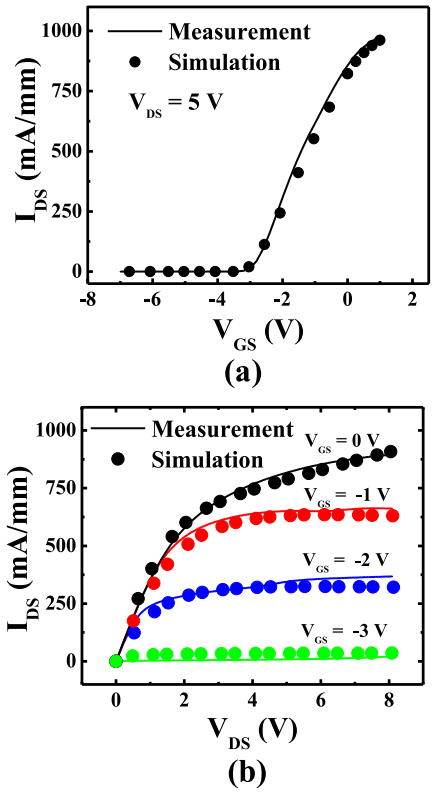

FIGURE 2. Plots of the measured and simulated (a) transfer characteristics at V_{DS} = 5 V, and (b) output characteristics of the calibrated structure.

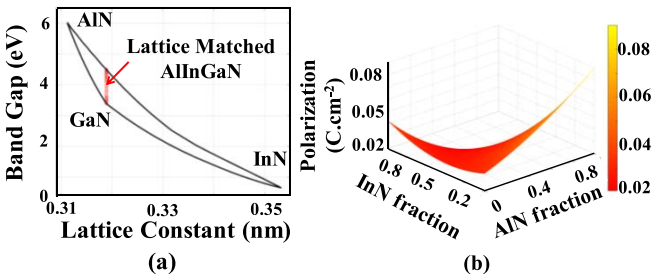

FIGURE 3. (a) The band gap vs lattice constant profile of the III-Nitride materials where red line represent lattice matched AlInGaN, and (b) variation of the polarization with AlN and InN fraction in AlInGaN.

contacts are set up by designing n-type heavily doped GaN and AlInGaN regions under that source and drain. The doping density in these regions is an order of 10^{20} cm^{-3}. The device characteristics are numerically simulated by solving the aforementioned device equations [15]–[16]. To provide the best accuracy of device simulation for both structures, calculated results are carefully calibrated with the measured data by adjusting the physical parameters.

III. RESULTS AND DISCUSSION

The Schottky barrier height at Ni/Au and semiconductor interface is calculated by $\phi_b = \phi_m - \chi$, where ϕ_m is the work function of metal and χ is the electron affinity of semiconductor. The calculated Schottky barrier height of the device is 1.1 eV. Characteristics of the reference AlInGaN/GaN

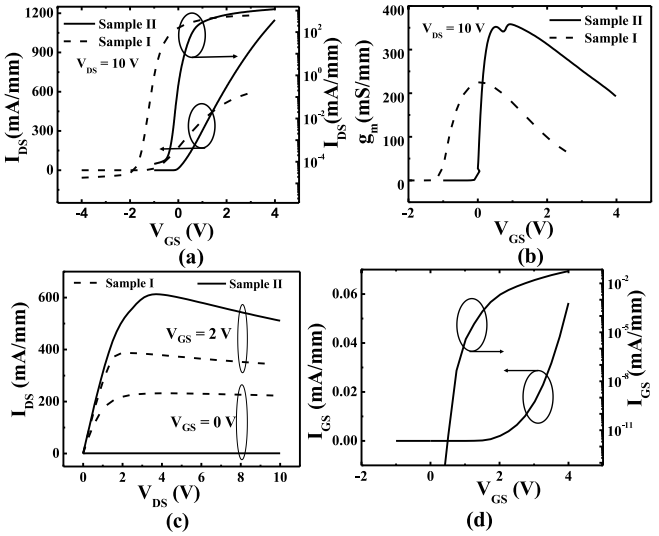

FIGURE 4. (a) $I_{DS}-V_{GS}$ at V_{DS} = 10 V, (b) g_m at V_{DS} = 10 V, (c)$I_{DS}-V_{DS}$ curves of single and double barrier AlInGaN/GaN HEMTs, and (d) $I_{GS}-V_{GS}$ curves of double barrier AlInGaN/GaN HEMTs at V_{DS} = 10 V.

HEMT are determined by the ven der pauw Hall effect measurement. The measured electron mobility, 2DEG, and sheet resistance are 1,920 cm^2/V.s, 1.2 $\times$ 10^{13}cm^{-2}, and 270 Ω/sq, respectively. In good agreement between the simulated and measured transfer characteristics at $V_{DS} = 5$ V of the AlInGaN/GaN HEMT is shown in Fig. 2(a). It reveals that the transport and physical models which we solved during the simulation can properly account for the physical phenomena of device. Its accuracy was further verified from the simulated dc characteristics with respect to different gate voltages, as shown in Fig. 2(b). The measured and simulated maximum drain current ($I_{DS,max}$) at $V_{DS} = 5$ V and $V_{GS} = 1$ V were 975 mA/mm and 961 mA/mm, respectively, when $V_{th} = -3.3$ V. Before designing the HEMT, possible composition of Al, In and Ga of AlInGaN for lattice matched with GaN and their band gap was calculated by using the Vegard's law [17],

$$a_{AlInGaN} = xa_{AlN} + ya_{GaN} + (1 - x - y)a_{InN}, \quad (1)$$

and

$$E_g = xE_{g,AlN} + yE_{g,GaN} + zE_{g,InN} - xy(1 - z)b_{AlGaN} - xz(1 - y)b_{AlInN} - yz(1 - x)b_{InGaN}, \quad (2)$$

where x, y, and z are Al, Ga and In composition in AlInGaN layer, $a_{AlN} = 0.311$ nm, $a_{GaN} = 0.318$ nm [18] and $a_{InN} = 0.353$ nm [19] are lattice constant, $E_g(AlN)$, $E_g(GaN)$ and $E_g(InN)$ are band gaps of AlN, GaN and InN respectively and b_{AlGaN}, b_{AlInN} and b_{InGaN} are bowing parameters of AlGaN, AlInN and InGaN respectively. The parameters used to calculate band gap are listed in Table 3. The calculated band gap and lattice constant the sets of AlInGaN which are lattice matched with GaN, plotted in Fig. 3(a). $Al_{0.72}In_{0.16}Ga_{0.12}N$, $Al_{0.36}In_{0.08}Ga_{0.56}N$, and $Al_{0.18}In_{0.04}Ga_{0.78}N$ are some AlInGaN compound which

TABLE 2. Mobility parameters used in simulation [13].

Parameter	Value
δ (V/s)	$5\text{x}10^{14}$
η (v^2/cm s)	$5.8\text{x}10^{30}$
μ_{max}(cm^2/ V s)	1500
Cr (cm^{-3})	$9.6\text{x}10^{16}$
γ	2.45
B (cm/s)	$9\text{x}10^{7}$

TABLE 3. Bowing parameters in eV, expressed as $bx = \alpha + \beta x + \gamma x^2$ for the ternary alloys [17].

Alloy	α	β	γ
AlInN	6.9	-8	3
AlGaN	0.75	-0.07	0
InGaN	1.74	-0.68	0

are lattice matched used to design the normally-off HEMT device as the spontaneous polarization of the AlInGaN is only the function of Al composition and is expressed as [20],

$$P_{sp}^{AlInGaN} = xP_{sp}^{AlN} + yP_{sp}^{GaN} + zP_{sp}^{InN} + xyu_{AlGaN} + xzu_{AlInN} + yzu_{InGaN}, \quad (3)$$

where, P_{sp} is spontaneous polarization of respective material. The values of u_{AlGaN}, u_{InGaN}, and u_{AlInN} obtained by solving the equations, tabulated in Table 4, and the required basic parameters were from [20]. The spontaneous polarization, as shown in Fig. 3(b), demonstrates that P_{sp} of AlInGaN layer mainly depends on AlN fraction. Higher the AlN fraction, larger the P_{sp} of AlInGaN. Similarly, for lattice matched barrier layer, the sheet charge density (σ) depends only on spontaneous polarization (piezoelectric polarization can be neglected) is defined as [21]

$$\sigma(x) = P_{sp}^{GaN} - P_{sp}^{AlInGaN}. \quad (4)$$

The simulated $I_{DS,max}$ and g_m of the proposed double barrier AlInGaN / GaN HEMT are plotted in Fig. 4(a) and 4(b). The results shows that the simulated $I_{DS,max}$ and $g_{m,max}$ of Sample II were 1149 mA/mm (at $V_{DS} = 10$ V, $V_{GS} = 4$ V) and 358 mS/mm, respectively, which were 94% and 57% larger than that of Sample I with a shift of V_{th} from -1.2 V to 0.2 V. The I_{on}/I_{off} ratios of both devices are in the order of 10^7 which is remarkable for GaN-based HEMTs. The magnitude of V_{th} is defined as the gate voltage at which the drain current is 1 mA/mm. Notably, larger V_{th} can be tuned by optimizing the composition of Al and In of the barrier. According to our simulation, not shown here, deviation of V_{th} of the explored double barrier HEMT is within 5% when the lattice temperature varies from 300 to 400K.

Furthermore, g_m of the double barrier HEMT shows peculiar characteristics with two peaks observed at $V_{GS} = 0.5$ and 1 V, respectively. The second peak indicates that carriers are injected into channel at the gate voltage larger than 1 V which is responsible for high level of the drain current [22]. Notably, the *Vth* is a function of the interface charge, the conduction band offset, and the dielectric constant as expressed

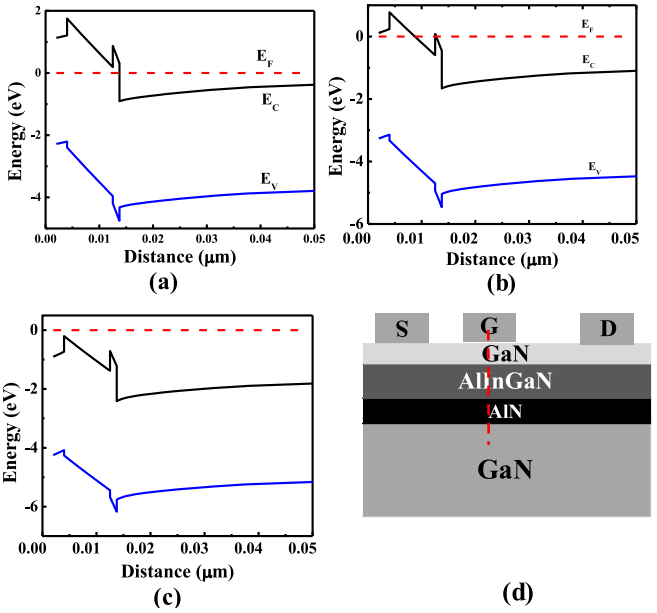

FIGURE 5. Plots of the conduction and valence band profiles of the sample I at (a) $V_{GS} = 0$ V, (b) $V_{GS} = 1$ V, (c) $V_{GS} = 2$ V, and (d) cut region of the HEMT to observe the band profiles.

TABLE 4. Adopted spontaneous polarization and other parameters used to calculate Eq. 3 [20].

Parameters	Value
P_{sp} (GaN)	0.034 C/m^2
P_{sp} (AlN)	0.09 C/m^2
P_{sp} (InN)	0.042 C/m^2
u_{AlGaN}	$4P_{sp,AlGaN}(x = 0.5)$-$2(P_{sp,AlN}$-$P_{sp,GaN})$
	$4P_{sp,AlGaN}$=-0.09x-0.034(1-x)+0.021x(1-x)
u_{AlInN}	$4P_{sp,AlInN}(x = 0.5)$-$2(P_{sp,AlN}$-$P_{sp,InN})$
	$4P_{sp,AlGaN}$=-0.09x-0.042(1-x)+0.07x(1-x)
u_{InGaN}	$4P_{sp,AlGaN}(x = 0.5)$-$2(P_{sp,AlN}$-$P_{sp,GaN})$
	$4P_{sp,AlGaN}$=-0.042x-0.034(1-x)+0.037x(1-x)

below [21]

$$V_{th} = \phi_b - \frac{\Delta E_c}{q} - \frac{\sigma(x)}{\varepsilon}d, \quad (5)$$

where, $\varepsilon(x)$ and d represent the dielectric constant and thickness of barrier layer respectively. Smaller Al fraction in AlInGaN results in smaller $\sigma(x)$, and ΔE_c which is the crucial factor for positive shift of V_{th}, as shown in Eq. 5. Therefore, positive V_{th} of Sample II is due to the lower polarization of the first barrier because of the recess gate. Interestingly, I_{DS}-V_{DS} curves in Fig. 4(c) show that the drain current of Sample II at $V_{GS} = 0$ V and $V_{GS} = 1$V are smaller than that of Sample I whereas the drain current of Sample II is larger at $V_{GS} = 2$ V. By considering the thermionic emission, Fig. 4(d) shows the simulated $I_{GS} - V_{GS}$ curves at $V_{DS} = 10$ V. The I_{GS} increases sharply when V_G increases, but the I_{GS}/I_{DS} ratio of about 10^{-5} at $V_{GS} = 4$ V which is engineering acceptable for device technologies [23]–[24]. Notably, electron can't flow from the source to the drain because of the upper 2DEG is cut by the recess gate. At low gate voltage, owing to lack of sufficient energy to crossover the potential barrier, the electrons appearing at the upper

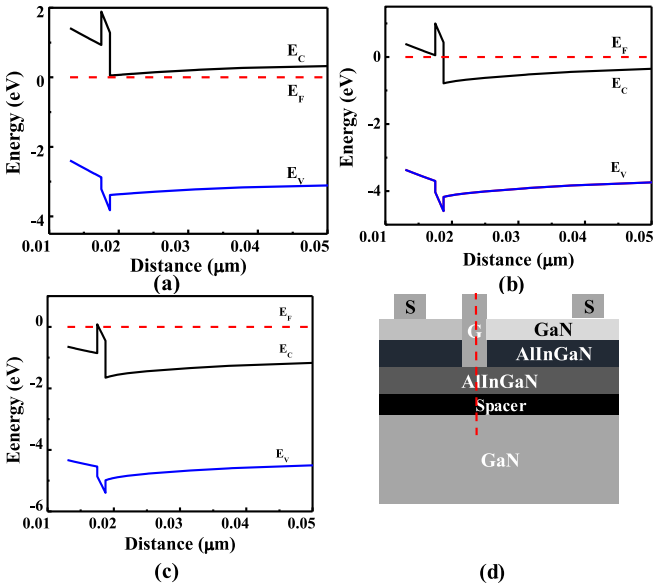

FIGURE 6. Plots of the conduction and valence band profiles of the sample II at (a) $V_{GS} = 0$ V, (b) $V_{GS} = 1$ V, (c) $V_{GS} = 2$ V, and (d) cut region of the HEMT to observe the band profiles.

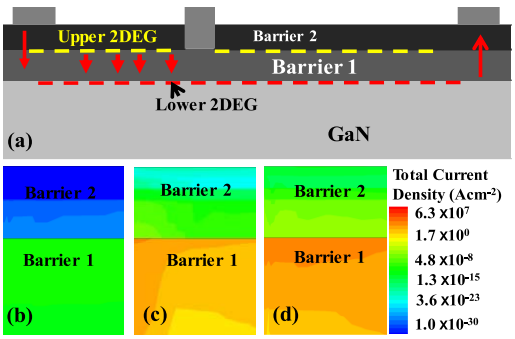

FIGURE 7. Plots of (a) the current flow in Sample II, and the total current density at (b) $V_{GS} = 0$ V, (c) $V_{GS} = 1$ V, and (d) $V_{GS} = 2$ V of the double barrier HEMT.

2DEG do not flow to the lower 2DEG. Therefore, the device behaves like a single channel HEMT and the total current of Sample II is less than that of Sample I and $V_{GS} = 0$ V and $V_{GS} = 1$ V. The conduction and valence band profiles of Samples I and II at $V_{GS} = 0$, 1, and 2 V, shown in Figs. 5 and 6, show that the conduction band moves lower so that the Fermi level goes up. This indicates that carriers in the 2DEG increase with V_{GS}. In contrary, at the higher V_{GS}, the voltage difference between the upper and lower 2DEG is large enough to overcome the potential barrier and the carriers flow to lower 2DEG [25], as shown in Fig. 7(a). At this point, the effective resistance decreases with the current increases because it behaves like resistors connected in parallel [25]. Therefore, the carrier density of Sample II under the gate is lower than that of Sample I at $V_{GS} \leq 1$ V, as shown in Figs. 7(b), and (c), which is significantly higher than that at large V_{GS} of 2 V, as shown in Fig. 7(d). In Sample II, the effective reduction of channel resistance offers

TABLE 5. Comparison among recent reports.

	Published year	$g_{m,max}$ (mS/mm)	V_{th} (V)	$I_{DS,max}$ (mA/mm)
Ref. [22]	2007	70	1	200
Ref. [26]	2018	60	0.4	356
Ref. [27]	2018	70	1.3	500
Ref.[28]	2017	345	-2.03	1200
Ref. [2]	2019	488	-0.8	1058
Calibrated Sample	-	-	-3.3	975
This Work	**-**	**358**	**0.2**	**1149**

considerable improvement in the conducting electrons. In this case, the second channel also contributes to the total current. Therefore, the proposed double barrier normally-off $Al_{0.72}In_{0.16}Ga_{0.12}N/Al_{0.18}In_{0.04}Ga_{0.78}N/GaN$ recess gate HEMT having barrier perfectly lattice matched with GaN shows unexpectedly improved output performance with significantly larger $I_{DS,max}$, $g_{m,max}$ and positive V_{th} than previously reported data for normally-off AlGaInN/GaN HEMTs, as listed in Table 5.

IV. CONCLUSION

An innovative and novel lattice matched double barrier $Al_{0.72}In_{0.16}Ga_{0.12}N/Al_{0.18}In_{0.04}Ga_{0.78}N/GaN$ normally-off HEMT was proposed and its electrical characteristics has been computationally studied by solving experimentally calibrated thermodynamic equation with appropriate physical models. The device offers significantly larger current density and transconductance in comparison to single barrier HEMT with positive threshold voltage. Interestingly, carriers are injected to 2DEG at higher gate voltage in the double barrier HEMT which results in significantly larger drain current and transconductance. The second barrier has no contribution in the total current of the device due to the insufficient energy to overcome the barrier at $V_{GS} = 0$ V. However, $V_{GS} \geq 2$ V, the electron carriers at $Al_{0.72}In_{0.16}Ga_{0.12}N/Al_{0.18}In_{0.04}Ga_{0.78}N$ interface will accumulate enough energy to flow toward $Al_{0.18}In_{0.04}Ga_{0.78}N/GaN$ and the total current of HEMT is significantly high which is also defined by the double peak in the transconductance curve. Hence, the proposed device comes up with surprisingly large drain current density and positive threshold voltage. Finally, the novel quaternary barrier e-mode HEMT has its merits for advanced high-frequency and high-power applications. It is because the achieved high current density and good scalability of AlInGaN barrier can effectively boost the high-frequency performance [29]; moreover, the normally-off operation of the explored double barrier device (i.e., Sample II) is crucial in high-power electronics [2], [5].

REFERENCES

[1] K. Omika *et al.*, "Operation mechanism of GaN-based transistors elucidated by element-specific X-ray Nanospectroscopy," *Sci. Rep.*, vol. 8, Sep. 2018, Art. no. 13268, doi: 10.1038/s41598-018-31485–4.
[2] T. Ohki *et al.*, "An over 20-W/mm S-band InAlGaN/GaN HEMT with SiC/diamond-bonded heat spreader" *IEEE Electron Device Lett.*, vol. 40, no. 2, pp. 287–290, Feb. 2019, doi: 10.1109/LED.2018.2884918.

[3] W. Wang *et al.*, "Improvement of power performance of GaN HEMT by using quaternary InAlGaN barrier," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 360–364, Feb. 2018, doi: 10.1109/JEDS.2018.2807185.

[4] J.-H. Hwang, S.-M. Kim, J. M. Woo, S.-M. Hong, and J.-H. Jang, "GaN HEMTs with quaternary $In_{0.05}Al_{0.75}Ga_{0.2}N$ Schottky barrier layer," *Phys. Status Solidi A*, vol. 213, no. 4, pp. 889–892, Feb. 2016, doi: 10.1002/pssa.201532566.

[5] F. Roccaforte, G. Greco, P. Fiorenza, and F. Iucolano, "An overview of normally-off GaN-based high," *Materials*, vol. 12, no. 10, p. 1599, May 2019, doi: 10.3390/ma12101599.

[6] N. M. Shrestha, Y. Li, and E. Y. Chang, "Step buffer layer of $Al_{0.25}Ga_{0.75}N/Al_{0.08}Ga_{0.92}N$ on P-InAlN gate normally-off high electron mobility transistors," *Semicond. Sci. Technol.*, vol. 31, Jun. 2016, Art. no. 075006, doi: 10.1088/0268-1242/31/7/075006.

[7] L. Yang *et al.*, "Improvement of subthreshold characteristic of gate-recessed AlGaN/GaN transistors by using dual-gate structure," *IEEE Trans. Electron Devices*, vol. 64, no. 10, pp. 4057–4064, Oct. 2017, doi: 10.1109/TED.2017.2741001.

[8] C.-H. Wu *et al.*, "Normally-OFF GaN MIS-HEMT with F-doped gate insulator using standard ion implantation," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 893–899, Jul. 2018, doi: 10.1109/JEDS.2018.2859769.

[9] Y. Shi *et al.*, "Carrier transport mechanisms underlying the bidirectional VTH shift in p-GaN gate HEMTs under forward gate stress," *IEEE Trans. Electron Devices*, vol. 66, no. 2, pp. 876–882, Feb. 2019, doi: 10.1109/TED.2018.2883573.

[10] D. Y. Jung *et al.*, "Design and evaluation of cascode GaN FET for switching power conversion systems," *ETRI J.*, vol. 39, no. 1, pp. 62–68, Nov. 2017, doi: 10.4218/etrij.17.0116.0173.

[11] L. Sayadi, G. Iannaccone, S. Sicre, O. Häberlen, and G. Curatola, "Threshold voltage instability in p-GaN gate AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 6, no. 6, pp. 2454–2460, Jun. 2018, doi: 10.1109/TED.2018.2828702.

[12] Y.-Z. Liu, W.-C. Ho, I. Sanyal, and J.-I. Chyi, "Fabrication of 0.25 μm T-gate AlInGaN/AlN/GaN HEMTs by I-line optical lithography," in *Proc. CSW*, Nara, Japan, 2019, doi: 10.1109/ICIPRM.2019.8819182.

[13] N. M. Shrestha, Y. Li, T. Suemitsu, and S. Samukawa, "Electrical characteristic of AlGaN/GaN high-electron-mobility transistors with recess gate structure," *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 1694–1698, Apr. 2019, doi: 10.1109/TED.2019.2901719.

[14] C.-H. Chen, Y. Li, C.-Y. Chen, Y.-Y. Chen, S.-C. Hsu, and W.-T. Huang, "Mobility model extraction for surface roughness of SiGe along (110) and (100) orientations in HKMG bulk FinFET devices" *Microelectron. Eng.*, vol. 109, pp. 357–359, Sep. 2013, doi: 10.1016/j.mee.2013.03.131.

[15] K. C. Shoo, C.-I. Kuo, Y. Li, and E. Y. Chang, "Novel metamorphic HEMTs with highly doped InGaAs source/drain regions for high frequency applications," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2594–2598, Oct. 2010, doi: 10.1109/TED.2010.2062521.

[16] Y. Li and S.-M. Yu, "A numerical iterative method for solving Schrödinger and Poisson equations in nanoscale single, double and surrounding gate metal-oxide-semiconductor structures," *Comput. Phys. Commun.*, vol. 169, pp. 309–312, Jul. 2005, doi: 10.1016/j.cpc.2005.03.069.

[17] I. Gorczyca, T. Suski, N. E. Christensen, and A. Svane, "Band gap bowing in quaternary nitride semiconducting alloys," *Appl. Phys. Lett.*, vol. 98, Aug. 2011, Art. no. 241905, doi: 10.1063/1.3597795.

[18] W. Qian, M. Skowronski, and G. R. Rohrer, "Structural defects and their relationship to nucleation of GaN thin films," in *Proc. MRS Symp.*, vol. 423. Pittsburgh, PA, USA, 1996, pp. 475–486, doi: 10.1557/PROC-423-475.

[19] M. E. Levinshtein, *Properties of Advanced Semiconductor Materials GaN, AlN, InN, BN, SiC, SiGe*, New York, NY, USA: Wiley, 2001, pp. 49–66.

[20] D. Godwinraj, H. Pardeshi, S. K. Pati, N. M. Kumar, and C. K. Sarkar, "Polarization based charge density drain current and small-signal model for nano-scale AlInGaN/AlN/GaN HEMT devices," *Superlattice Microstructures*, vol. 54, pp. 188–203, Feb. 2013, doi: 10.1016/j.spmi.2012.11.020.

[21] Z. Wang, B. Zhang, W. Chen, and Z. Li, "A closed-form charge control model for the threshold voltage of depletion- and enhancement-mode AlGaN/GaN devices," *IEEE Trans. Electron Devices*, vol. 60, no. 5, pp. 1607–1612, May 2013, doi: 10.1109/TED.2013.2252466.

[22] Y. Uemoto *et al.*, "Gate injection transistor (GIT)—A normally-off AlGaN/GaN power transistor using conductivity modulation," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3393–3399, Dec. 2007, doi: 10.1109/TED.2007.908601.

[23] K. Zhang, C. Kong, J. Zhou, Y. Kong, and T. Chen, "High-performance enhancement-mode Al_2O_3/InAlGaN/GaN MOS high-electron mobility transistors with a self-aligned gate recessing technology," *Appl. Phys. Exp.*, vol. 10, Jan. 2017, Art. no. 024101, doi: 10.7567/APEX.10.024101.

[24] H.-S. Kim, M.-J. Kang, J. J. Kim, K.-S. Seo, and H.-Y. Cha, "Effects of recessed-gate structure on AlGaN/GaN-on-SiC MIS-HEMTs with thin AlO_xN_y MIS gate," *Materials*, vol. 13, no. 7, p. 1538, Mar. 2020, doi: 10.3390/ma13071538.

[25] T. Palacios *et al.*, "Use of double-channel heterostructures to improve the access resistance and linearity in GaN-based HEMTs," *IEEE Trans. Electron Devices*, vol. 53, no. 3, pp. 562–565, Mar. 2013, doi: 10.1109/TED.2005.863767.

[26] M. Tao *et al.*, "Characterization of 880 V normally off GaN MOSHEMT on silicon substrate fabricated with a plasma-free, self-terminated gate recess process," *IEEE Trans. Electron Devices*, vol. 65, no. 4, pp. 1453–1457, Apr. 2018, doi: 10.1109/TED.2018.2808345.

[27] J. Gao *et al.*, "Gate-recessed normally OFF GaN MOSHEMT with high-temperature oxidation/wet etching using LPCVD Si3N4 as the mask," *IEEE Trans. Electron Devices*, vol. 65, no. 5, pp. 1728–1733, May. 2018, doi: 10.1109/TED.2018.2812215.

[28] H. S. Yoon *et al.*, "Characterization of 0.18-μm gate length AlGaN/GaN HEMTs on SiC fabricated using two-step gate recessing," *J. Korean Phys. Soc.*, vol. 71, pp. 360–364, Sep. 2017, doi: 10.3938/jkps.71.360.

[29] R. Wang *et al.*, "Quaternary barrier InAlGaN HEMTs with f_T/f_{max} of 230/300 GHz," *IEEE Trans. Electron Devices*, vol. 34, no. 3, pp. 378–380, Mar. 2013, doi: 10.1109/LED.2013.2238503.