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Comparative Study on Dynamic Characteristics of GaN HEMT at 300K and 150K

YANGQIAN WANG^{1,2,3}, YITIAN GU^{1,2,3}, XING LU⁴ (Member, IEEE), HUAXING JIANG⁵ (Member, IEEE),
HAOWEN GUO¹, BAILE CHEN¹, KEI MAY LAU⁵ (Life Fellow, IEEE), AND XINBO ZOU¹ (Member, IEEE)

¹ School of Information Science and Technology, ShanghaiTech University, Shanghai 201210, China

² Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China

³ University of Chinese Academy of Sciences, Beijing 100049, China

⁴ School of Electronics and Information Technology, Sun Yat-sen University, Guangzhou 510006, China

⁵ Electronic and Computer Engineering Department, Hong Kong University of Science and Technology, Hong Kong 999077

CORRESPONDING AUTHORS: X. ZOU AND X. LU (e-mail: zouxb@shanghaitech.edu.cn; lux86@mail.sysu.edu.cn)

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ABSTRACT Dynamic characteristics of GaN HEMT grown on a native substrate were systematically investigated at 300K and 150K. Transfer and output characteristics of the GaN HEMT were measured after various off-state stressing conditions and recovery durations. In addition, a high-speed scheme was employed to finish the measurement within 75 μ s, and to ensure maximum preservation of stressing/recovery consequences. The threshold voltage instability and current collapse commonly observed at room temperature were mostly diminished at 150K, which was attributed to reduced number of electrons through the metal-semiconductor contact and insufficient number of carriers overcoming the capture potential barrier. Two pulsed I - V measurements, including evaluations with various off-state quiescent bias points and “on-the-fly” on-resistance sampling, confirmed an inefficient electron capture process at 150K, with a time constant larger than dozens of seconds. The output characteristic comparison between hard switch and soft switch at 150K provided direct experimental evidence for electron capture promotion by hot carriers.

INDEX TERMS Cryogenic temperatures, dynamic performance, GaN HEMT, low temperature electronics.

I. INTRODUCTION

Study on behaviors of semiconductor devices and circuits at cryogenic temperatures are of great importance for electronics used in space explorations, cryo-imaging, and future data centers [1]–[3]. III-N high electron mobility transistor (HEMT), by virtue of its chemical stability, large critical electrical field, and polarization-induced 2DEG, is attractive for environmental extremes of temperature, radiation and so on [4], [5].

There have been some reports about III-N HEMT performance at cryogenic temperatures as low as 15K [6]–[10]. Lin *et al.* studied the kink effect by comparing the pulsed and DC I - V curves from 100K to 300K. DC

measurement results of InAlGaN/GaN HEMTs at cryogenic temperatures have been reported by Dogmus *et al.* However, dynamic performance of GaN HEMT after exposure to negative/positive gate bias with/without large drain-source bias has not been reported yet for cryogenic temperatures. Dynamic on-resistance degradation [11], [12], which is widely observed for GaN HEMTs grown on a variety of substrates, has been regarded as one of the major obstacles of GaN HEMT for practical applications. It was reported that the dynamic on-resistance was significantly increased at higher temperatures [13], suggesting a low operation temperature is likely to favorably mitigate the dynamic on-resistance increase. However, quantitative assessment of

dynamic performance, including measurement of threshold voltage shift and possible dynamic on-resistance increase of GaN HEMT at low temperatures is still yet to be known.

Hot electron effect has been identified as one of the reasons of dynamic on-resistance increase [14]–[16]. The experimental evidence of hot electron effects was obtained previously utilizing electroluminescence (EL) techniques [17], [18]. However, the study of hot electron effects was often carried out at room temperatures or above [19], at which the hot electron induced trap effects are mixed with already-existed traps. Thus, a quantitative understanding of hot electron effect itself is still unclear. Cryogenic temperature created an ideal environment to study hot electron effects in GaN HEMT, as the trap behaviors are expected to be greatly suppressed while hot electron induced effects would thus be possibly unmasked separately. In addition, the average kinetic energy of electrons injected into the channel is enhanced at a lower temperature due to higher carrier mobility. Thus, a low driving voltage would be sufficient to trigger hot carrier injection, and self-heating effects [20] would be greatly mitigated.

In this context, a systematic comparative study of dynamic performance of GaN HEMT was performed at 300K and 150K. I - V characteristics of GaN HEMT upon various negative/positive gate bias & recovery conditions were summarized; switching-mode pulsed I - V measurements with different off-state voltage, stressing duration, and drain-gate-delay (DGD) time at 300K and 150K were analyzed. The output characteristic comparison between hard switch and soft switch at 150K help quantitatively determine consequences induced purely by hot electron effects.

II. EXPERIMENTAL

The sample used in this study was GaN-based HEMT grown on a native GaN substrate. As shown in Fig. 1 (a), the epitaxial structure includes a 2 μm undoped GaN layer, a 1 nm AlN spacer, and a 20 nm undoped $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ barrier. The 270- μm -thick n-type GaN substrate has a resistivity of 0.04 $\Omega\cdot\text{cm}$ and a dislocation density of $\sim 10^7 \text{ cm}^{-2}$. The fabrication of the HEMT started with Cl_2 -based inductively coupled plasma (ICP) etching. Then, Ti/Al/Ni/Au (20/150/50/80 nm) was deposited by e-beam evaporation and annealed at 850 $^\circ\text{C}$ for 30 s in N_2 ambient to form Ohmic contact on the AlGaN barrier, as the source/drain terminals. Finally, a Ni/Au (20/200 nm) Schottky metal was deposited as the gate. It is noted that the studied HEMT device was finished without any advanced passivation layers to examine possible trap behaviors at 150K.

The gate width/length of the device in this study was 20 μm /0.8 μm , and the distance between gate to drain and to source were both 1 μm ($L_g = 0.8\mu\text{m}$, $L_{gd} = L_{gs} = 1\mu\text{m}$, $W_g = 20\mu\text{m}$). In “fast” I - V measurements, various negative/positive gate bias w/o source-drain bias & recovery time was applied onto the device before high-speed sweeping I - V measurement was performed on the device. The total sweeping measurement period was set to be merely 75 μs

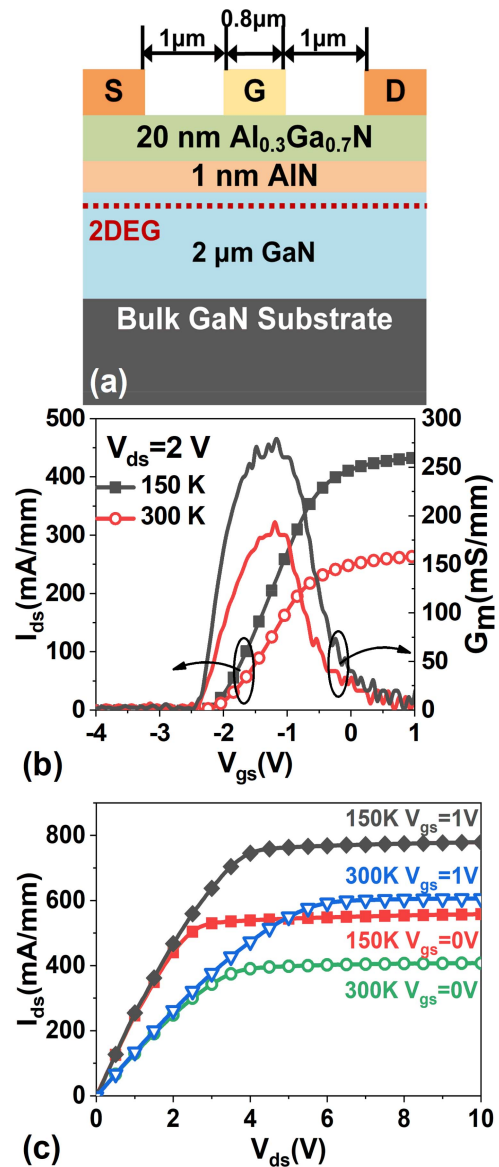


FIGURE 1. (a) Schematic cross section of GaN-based HEMT. (b) Transfer characteristics at 150K and 300K. (c) Output characteristics at 150K and 300K.

to highly preserve the effects induced by negative/positive bias and off-state stressing. For pulsed I - V measurements, the pulse width was set to be 20 μs to pinpoint the characteristics at various quiescent bias points and after exposure to certain amount of stressing time.

III. RESULTS AND DISCUSSIONS

A. FAST I - V MEASUREMENTS

Fig. 1 (b) and (c) show transfer curves and output curves of the GaN HEMT at 150K and 300K without any pre-stressing conditions. Using the 10 mA/mm standard, the threshold voltage V_{th} was barely shifted ($\Delta V_{th} = 0.05 \text{ V}$) as the decrease of the temperature down to 150K. The device exhibited much higher peak transconductance ($g_m = 280 \text{ mS/mm}$) and larger saturation current (770 mA/mm at

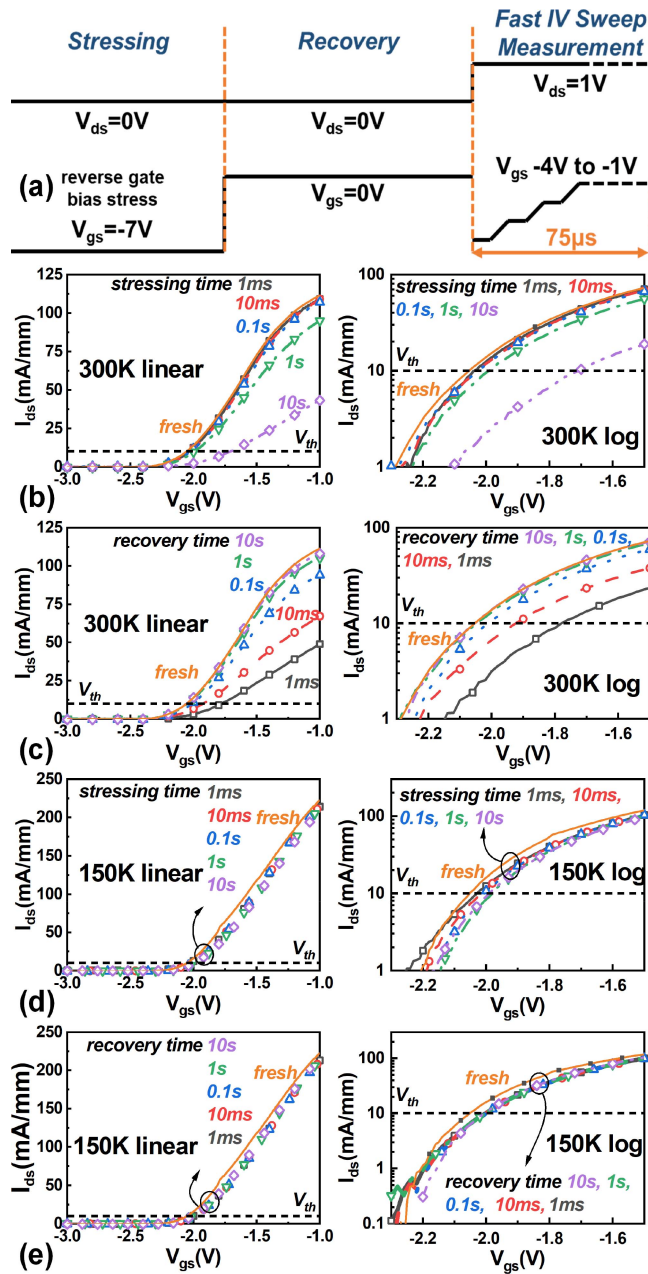


FIGURE 2. (a) Schematic three-phase “stress-recovery-measurement” procedure. (b, d) NBTI measurements with various reverse gate bias stressing duration ($V_{gs} = -7V$) at 300K and 150K. (c, e) NBTI measurements with various recovery duration after reverse gate bias stress ($V_{gs} = -7V$, 10s) for 300K and 150K.

$V_{gs} = 1V$) at 150K than that at 300K ($g_m = 200$ mS/mm, $I_{ds} = 606$ mA/mm at $V_{gs} = 1V$). This is mainly attributed to the enhancement of electron mobility in the 2DEG channel as a result of reduced thermal lattice vibration scattering at low temperatures [21].

Fig. 2 summarized negative bias threshold instability (NBTI) measurement results at 300K and 150K. Fig. 2 (a) schematically shows the “stress-recovery-measurement” waveforms. In this measurement, only a negative gate voltage was applied without large drain bias

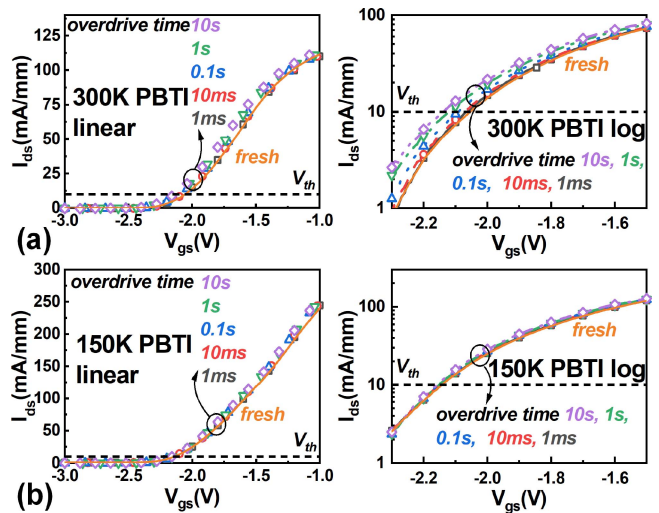


FIGURE 3. PBTI tests with various overdrive gate voltage ($V_{gs} = 2V$) duration at 300K and 150K.

($V_{ds} = 0V$), so that buffer-related charge-trapping process could be minimized. As shown in Fig. 2 (b), at 300K V_{th} was found gradually shifted positively after being exposed to reverse gate bias stress ($V_{gs} = -7V$) for a duration from 1ms to 10s. For the latter case, ΔV_{th} was determined to be 0.38V, together with degradation of transconductance. The positive V_{th} shift has been extensively studied and was attributed to the electron passing through the Schottky contact, e.g., via Frenkel-Poole emission (FPE) [22], and charge-trapping effects [23] occurred in the AlGaN barrier and the whole device surface due to the same potential difference for gate-source terminals and gate-drain terminals [13], [24]. While in a recovery experiment [Fig. 2 (c)], the sample was pre-stressed with $V_{gs} = -7V$ for a fixed 10s, then the V_{th} was gradually recovered to original $-2.08V$ when extending the “rest time” from 1ms to 10s. It was found that after 1s recovery time the device was almost fully recovered to its initial status. It’s a reverse process of charge-trapping, engaging the same set of traps. The traps which captured electrons would thermally emit electrons during the recovery duration, resulting in mitigation of virtual gate effect and negative shift of V_{th} at 300K [18].

While at 150K, the threshold voltage shift was limited to be only 0.14 V using the same reverse gate bias stressing conditions as above, indicating a much stabilized threshold voltage at low operation temperature of 150K [Fig. 2 (d)]. Furthermore, the transconductance was not compromised as extending the negative gate bias duration. The phenomenon was attributed to lowered electron thermal energy in the following two processes: (i) the number of electron through metal-semiconductor contact, reaching the trap states of AlGaN as well as continuum electronic states was much reduced at 150K [25], [26]; (ii) the number of electrons capable of overcoming the capture energy barrier [27], was much reduced as well due to limited thermal energy of electrons, where the capture energy barrier height was

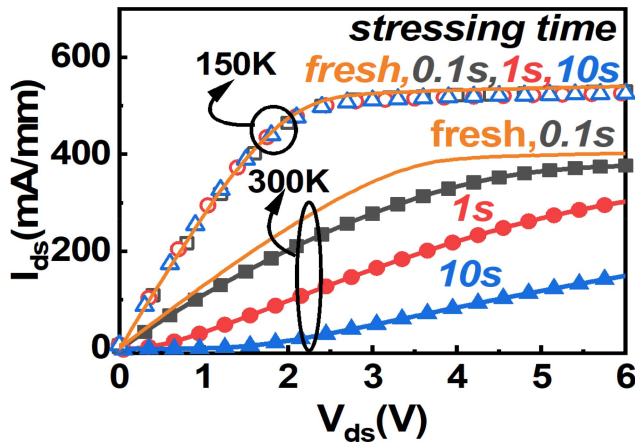


FIGURE 4. Dependence of output characteristics ($V_{gs} = 0V$) degradation on pre-stress duration at 300K and 150K.

regarded as unchanged at 150K [28]. And the phenomenon matched well with previous reports that the trapping time constant associated with the traps would be greatly prolonged as decreasing the temperature [13], [29]. Thus, chances for charge-trapping went quite low for the experimental conditions ($V_{gs} = -7V$ at 150K). As a result, with inefficient carrier-trapping under the pre-stressing condition, the transfer curves of the GaN HEMT tend to overlap with each other, independent of “rest time” from 1ms to 10s at 150K [Fig. 2 (e)].

Fig. 3 showed positive bias threshold instability (PBTI) measurement results at 300K and 150K. In PBTI measurement, fast IV scans were performed immediately upon applying a positive 2V on the gate for a certain amount of time from 1ms to 10s while V_{ds} was kept grounded. As shown in Fig. 3 (a), at 300K a negative V_{th} shift of 0.05 V was observed after positive gate biasing for 10s, indicating a modest de-trapping process of electron traps in the AlGaIn layer and whole device surface [13]. Upon the depletion of the traps, the V_{th} was negatively shifted. While at 150K [Fig. 3 (b)] the transfer characteristics were overlaid with each other and a consistent V_{th} was observed. This can be attributed to the fact that the thermal-assisted de-trapping process was also greatly suppressed at 150K.

Fig. 4 shows the output characteristics of GaN HEMT after exposure to off-state stressing ($V_{gs} = -7V$, $V_{ds} = 10V$) for various amount of time. At 300K, as the stressing time was extended from 0.1s to 10s, the on-resistance in the linear region was greatly enlarged from 11 ohm-mm to 89 ohm-mm with 36.6% saturation current collapse (C.C.) due to charge-trapping effects in the AlGaIn barrier and gate-to-drain access region. While at 150K, the phenomenon of current collapse was typically diminished due to reduced number of electrons through the Schottky contact and captured by traps, which well agreed with the phenomenon observed in Fig. 2. The results indicated that for low temperature application, the GaN HEMT could show a much stabilized performance and alleviated current collapse without employing complex surface passivation techniques.

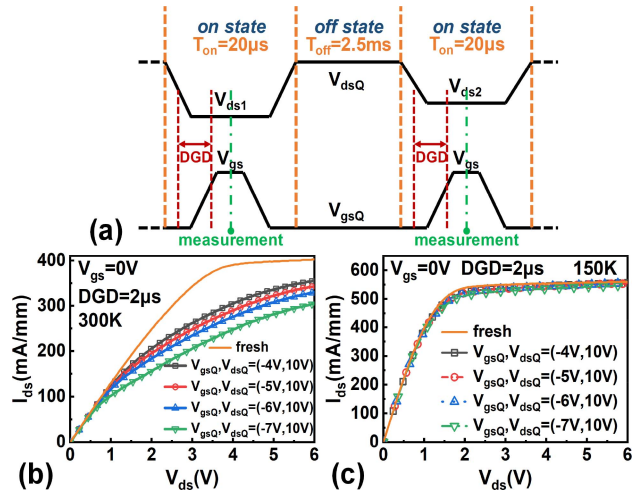


FIGURE 5. (a) Schematic waveforms of the pulsed I-V measurement used in Part B, DGD was defined as the delay from V_{ds} got halved to $V_{gs} = V_{th}$. (b, c) Pulsed $I_{ds} - V_{ds}$ characteristics of the GaN-based HEMTs under various quiescent bias at 300K and 150K.

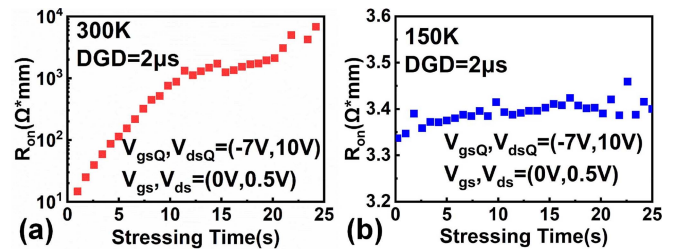


FIGURE 6. (a, b) Dependence of dynamic R_{on} increase on off-state stressing duration at 300K and 150K.

B. PULSED I-V MEASUREMENTS

Fig. 5 (a) schematically showed the pulsed I-V waveforms used in switching-mode measurements. It also consisted of three phases: i) off-state stress phase: pulsed V_{gsQ} below V_{th} was applied with high drain bias V_{dsQ} ; ii) transient phase: V_{gs} was increased to be above V_{th} , while V_{ds} was dropped to relatively lower bias range; drain-gate-delay (DGD) was defined to be the time difference between V_{ds} was halved and V_{gs} reached V_{th} . Thus, a negative/positive DGD value denotes hard-switch and soft-switch mode, respectively. iii) the third phase was on-state measurement phase and the drain bias could be set as various values as needed.

Fig. 5 (b) show the pulsed $I_{ds} - V_{ds}$ characteristics of the GaN HEMTs under various quiescent bias V_{gsQ} and V_{dsQ} at 300 K. In this experiment, DGD was set as 2 μs that a soft switch mode was employed. The current collapse and dynamic R_{on} increase became more significant as the reverse gate bias was enlarged while V_{dsQ} remained as 10 V. This was because electron trapping in the gate-to-drain access region was enhanced as the increase of V_{dgQ} bias as well as high lateral electrical field [30]. Thus, negative charge accumulation lead to a partially depleted 2DEG in the channel [31]. While at 150K, as shown in Fig. 5 (c), the change of V_{gsQ} from $-4V$ to $-7V$ has a negligible impact

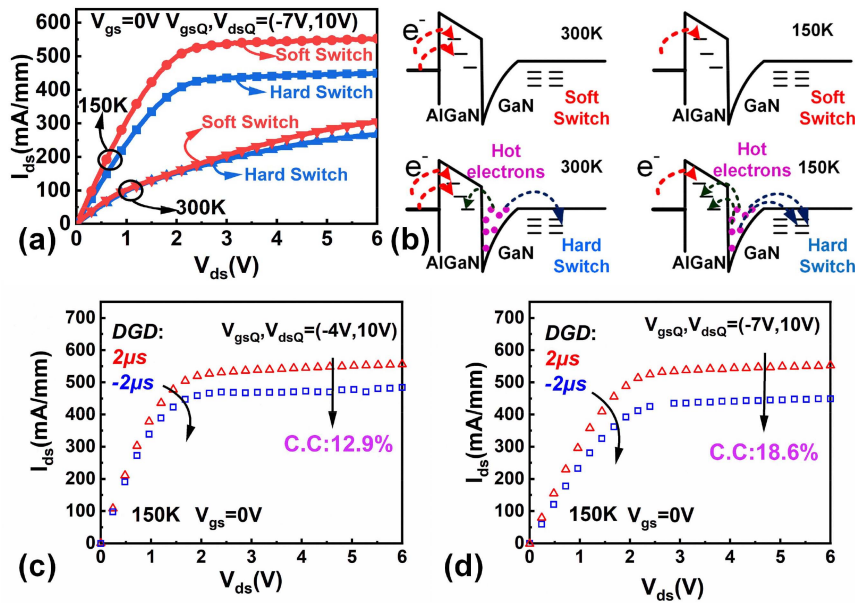


FIGURE 7. (a) Pulsed $I_{ds} - V_{ds}$ characteristics of the GaN-based HEMTs under hard switch (DGD < 0) and soft switch (DGD > 0) at 300K and 150K. (b) Schematic band diagrams of the AlGaN/GaN HEMT under the soft switch conditions and under the hard switch conditions at 300K and 150K. (c, d) Pulsed $I_{ds} - V_{ds}$ under two different quiescent bias (V_{gsQ}, V_{dsQ}) at 150K.

on the dynamic performance of GaN-based HEMTs using the same quiescent bias, leading to a current collapse free device performance. This was attributed to a very inefficient electron capture process which holds a long capture time constant [29].

In order to investigate the time-dependent trapping process, a so-called “on-the-fly” on-resistance measurement was performed. The device was subject to stressing condition ($V_{gsQ}, V_{dsQ} = -7\text{ V}, 10\text{ V}$) while the variation of R_{on} was recorded by switching the device to on-state using 20- μs short pulses repeatedly without perturbing the stress process. The dynamic R_{on} was evaluated in the linear region where $V_{gs} = 0\text{ V}$ and $V_{ds} = 0.5\text{ V}$. At 300K, as seen in Fig. 6 (a), the dynamic R_{on} was significantly increased as the stressing time was prolonged up to 25s. The R_{on} was increased from initial 8.4 ohm-mm to nearly 10^4 ohm-mm after 25 seconds stressing. After 25s, the measured current and dynamic on-resistance reached saturated 10^{-2} mA/mm and 10^4 ohm-mm. This could be understood as the process of injection of electrons into traps under the gate and in the gate-drain access region. While at 150K, as the off-state stressing duration was extended up to 25 seconds, the variation of the on-resistance was greatly suppressed, in the range of (3.396 ± 0.005) ohm-mm only, suggesting a current collapse-free performance and a much prolonged time constant (at least several dozens of seconds) of the trapping process at 150K.

In addition to soft-switch operations, the device was also subject to hard switching conditions for comparisons. Fig. 7 (a) depicts output characteristics with drain-gate-delay (DGD) time of 2 μs (soft switch) and -2 μs (hard switch) at 300K and 150K. At 300K, the slightly lower drain

current obtained from the hard-switch approach was regarded to be associated with hot electron effects as the difference was only observed at high V_{ds} bias range.

While for 150K, as discussed above and shown in Fig. 5 (c), overlaid I-V curves were obtained using a soft switch scheme, confirming a current-collapse-free device performance and traps being transparent to the device if there were any at 150K. However, under a hard switch scheme, current collapse was observed that the dynamic on-resistance was greatly enlarged and the saturation current was significantly compromised at low temperatures. At 150K, the average kinetic energy of electrons was enhanced due to boosted carrier mobility as well as high electrical field applied during the voltage transition. Thus, those electrons injected into the channel received sufficient energy to overcome the capture potential barrier [32] to have themselves trapped, which was not observed for soft-switch mode due to insufficient kinetic electron energy. This phenomenon is consistent with the observation that “the on-resistance increase induced by hot-electrons was decreased at higher temperatures”, as reported in [33], where experiments were performed above room temperatures. Schematic band diagrams describing the above soft switch conditions and hard switch conditions were shown in Fig. 7 (b).

Fig. 7(c, d) displays pulsed $I_{ds} - V_{ds}$ curves under two different quiescent bias (V_{gsQ}, V_{dsQ}) to further investigate hot electron effects at 150K. As V_{gsQ} was enlarged from -4V to -7V while keeping $V_{dsQ} = 10\text{ V}$, the saturation current collapse was increased from 12.9% to 18.6%. The degraded C.C. as increase of gate reverse bias also suggested the existence of capture potential barrier because injected electrons with higher kinetic energy resulted in a larger number of

electrons being trapped. The evidence from this study pointed towards the conclusion that hot electrons was the main mechanism of current collapse and dynamic on-resistance increase by promoting carrier capture at 150K.

IV. CONCLUSION

Dynamic characteristics of GaN HEMT grown on a native GaN substrate was investigated at 300K and 150K. A “stress-recovery-measurement” scheme was firstly used to assess the dynamic performance after various off-state stressing conditions and recovery durations. A fast I-V sweeping measurement method was utilized to ensure the measurement completion within 75 μ s during which the stressing/recovery effects were highly preserved. Much stabilized threshold voltage and diminished current collapse at 150K indicated the electron trapping effects commonly observed at 300K were greatly suppressed. Two pulsed I-V measurements, including evaluations with various off-state quiescent bias points and “on-the-fly” on-resistance sampling further confirmed an alleviated trapping effect and reduced number of trapped electrons at a low temperature. The results indicated that for low temperature soft switching applications, the GaN HEMT could show a much stabilized threshold voltage and alleviated current collapse without employing complex surface passivation techniques. At 150K, current collapse was only observed using a hard switch scheme, providing experimental observation and evidence to electron capture promotion induced by highly energetic hot electrons.

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