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ESD Improvements on Power N-Channel LDMOS Devices by the Composite Structure of Super Junctions Integrated With SCRs in the Drain Side

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ABSTRACT This paper studies a composite power n-channel lateral-diffused MOSFET device with a super junction (SJ) and parasitic silicon-controlled rectifier structure (nLDMOS-SJ-SCR) in the drain side, which can be used for electrostatic discharge (ESD) and latch-up (LU) reliability enhancements of 60-V power electronics. For ESD and LU protection considerations, the drain side with an SJ structure integrated with *p-n-p-* and *n-p-n*-arranged types of nLDMOS-SCR transistors is demonstrated. According to the experimental data, the layout of the SJ structure in the drain side has positive effects on ESD and LU capabilities. The layout type of nLDMOS-SJ with a pillar width W = 9μm has the highest secondary breakdown current (I_{t2}) values; the ESD (LU) improvement was 46.3% (13.3%) compared with the nLDMOS reference sample. Meanwhile, an nLDMOS-SJ with a pillar width W = 27μm has the highest figure of merit (FOM) value. By contrast, an embedded *p-n-p-*(*n-p-n-*)arranged type SCR structure was added into the drain side once again. Initially, it has a positive (negative) effect on the ESD reliability. Furthermore, the ESD (figure of merit; FOM) improvement was 37.9% (13.72%) of the corresponding nLDMOS-SJ device for nLDMOS-SJ-SCR (*p-n-p*) with W = 27μm. Overall, an nLDMOS-SJ device integrated with the *p-n-p*-arranged-type SCR in the drain side is a favorable choice for ESD and LU improvements.

INDEX TERMS Electrostatic discharge (ESD), latch-up (LU), n-channel lateral-diffused MOSFET (nLDMOS), secondary breakdown current (I_{t2}), silicon controller rectifier (SCR), super junction (SJ).

I. INTRODUCTION

Recently, power integrated components in the power system or module integrations have gained attention. High voltage (HV) lateral-diffused metal–oxide–semiconductor field-effect transistor (LDMOS) components are often used in smart power ICs, such as switching power supplies, automotive electronics, RF power amplifiers, mobile telecommunications, LED drivers, and LCD displays [1]–[16]. For a high operating-voltage requirement, this power component requires a favorable range of reliability ability. If a power integrated circuit (PIC) is stressed by a noise transient and/or an electrostatic discharge (ESD) pulse, it may lead to the destruction of HV components caused by ESD or electrical over-stress (EOS). Therefore, in many applications, a power LDMOS urgently needs to have good ESD and/or latch-up (LU) capabilities [17]–[27].

However, an HV n-channel LDMOS (nLDMOS) is usually served as an ESD protection element, but it has some major disadvantages due to higher trigger voltage (V_{t1}) and lower holding voltage (V_h). Then, a gate-grounded nMOSFET (GGnMOS) device with a multi-finger layout will be occurred the non-uniformity turned-on issue, thus leading to extremely low ESD robustness per unit channel width particularly in the HV nLDMOS devices due to high V_{t1}

value [28]. Moreover, the low holding voltage (V_h) of a component is easily prone to LU burnout. How to solve these difficult reliability problems?

A super-junction (SJ) structure in HV LDMOS devices can effectively improve the relationship between the breakdown voltage and the on-resistance [29]–[38]. In addition, this concept can be used to enhance the ESD capability of HV MOSFETs, but the enhancement is still slightly insufficient. By contrast, power SCRs are commonly used in HV applications because their V_{t1} values are slightly lower than those of nMOSFETs fabricated using the same process [39] and they provide excellent ESD robustness per unit channel width [24], [40]–[47]. However, SCRs have some disadvantages. Compared with the operating voltage V_{DD}, the V_h value is extremely low. Consequently, we have some new ideas to integrate and merge these two HV components. That is to say, if an SJ structure is added into the drain terminal of an HV nLDMOS and linked with an embedded SCR in the drain side again, how will the ESD and LU reliabilities be affected? Therefore, in this study, various P^+ implants were inserted into the drain end of an nLDMOS-SJ (nLDMOS with a super-junction structure) device to form an nLDMOS-SJ sample worked together with an embedded parasitic SCR device. Then, this study investigated the influences of drain-end engineering on the ESD and LU manifestations of this new power compound device. Finally, a comprehensive index for weighing the reliability of ESD and LU, the figure of merit (FOM) of these power samples of the ESD, LU, and cell area considerations are defined and evaluated as

$$FOM = \frac{I_{t2} \times V_h}{cell\ area}. \quad (1)$$

II. DEVICE STRUCTURES OF POWER NLDMOS DUTS

A. THE PURE NLDMOS REFERENCE DEVICE

Testing components of 60-V HV pure nLDMOS and the following devices were fabricated using a TSMC 0.25-μm 60-V Bipolar-CMOS-DMOS (BCD) process. The channel length (L) of these devices under test (DUTs), channel width of each finger (W_f), and total channel width (W_{tot}) (constant) were 2, 100, and 600 μm, respectively; finger numbers M = 6. Here, the pure nLDMOS was regarded as a reference or benchmark DUT. Figs. 1 and 2 respectively show the schematic layout diagram and three-dimensional (3D) cross-sectional view (along the line AA' of Fig. 1) of this pure nLDMOS transistor. The HVPB, SH_P, H60PW, H60NW, and shallow-trench isolation (STI) layers are the necessary well structures for a 60-V device. Furthermore, spacing of the H60NW edge to the left drain-side thin-oxide definition (OD) is denoted by L_d, and the OD zone is denoted by the thin-oxide definition area. In addition, a butted contact structure for the source-to-bulk electrode connection was used in this study. A silicide layer was formed at drain and source ends. As shown in Fig. 2, when an nLDMOS device forms a gate-to-ground connection, it can conduct the transient ESD current through the parasitic BJT (Q1) under this MOSFET; R_{bulk} and R_{drift} are the parasitic resistances of the source-to-bulk and drift regions, respectively.

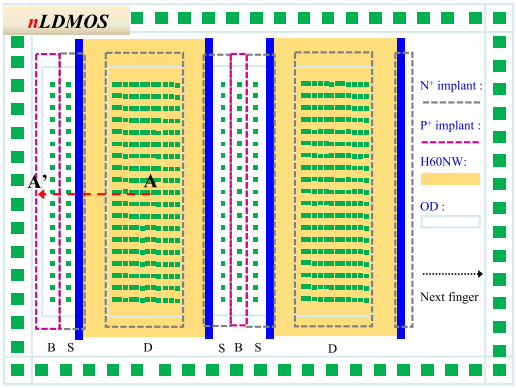

FIGURE 1. Layout-view diagram of the HV pure nLDMOS (Ref. DUT).

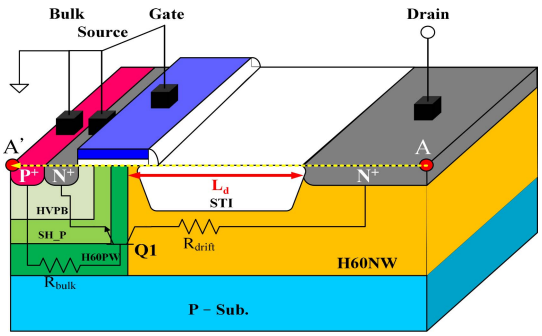

FIGURE 2. 3D Cross-sectional view of the HV pure nLDMOS (Ref. DUT).

B. AN NLDMOS WITH SUPER-JUNCTION (SJ) STRUCTURES

Figs. 3 and 4 show that an nLDMOS was constructed in a parallel SJ structure below the shallow-trench-isolation (STI) region at the drain end (denoted as nLDMOS-SJ). It is found that it is a complex architecture. Beneath the drain-side STI region, some H60PW layers were inserted into the H60NW layer and permuted to form a similar SJ structure. A 4-μm STI gap was present between the parallel SJ endings and the drain-side with high doses ($> 10^{19}$ cm^{-3}) of OD. When the H60PW and H60NW widths for the nLDMOS-SJ devices varied, the pillar widths of these two layers were always kept equal ($W_n = W_p = W$), and there were four classifications of 6-, 9-, 18-, and 27-μm widths. The heights of the SJ pillar (H60NW and H60PW layers) were denoted by h.

C. AN NLDMOS-SJ WITH EMBEDDED SCR STRUCTURES

Figs. 5–8 show the schematic layout diagrams and 3D cross-sectional views of an nLDMOS-SJ with a drain-side *p-n-p-* and *n-p-n*-arranged SCR. These doped-zone arrangements are named from the left side to the right side of the drain electrode. In this study, the total drain-side areas of the nLDMOS, nLDMOS-SJ, and nLDMOS-SJ-SCR devices were

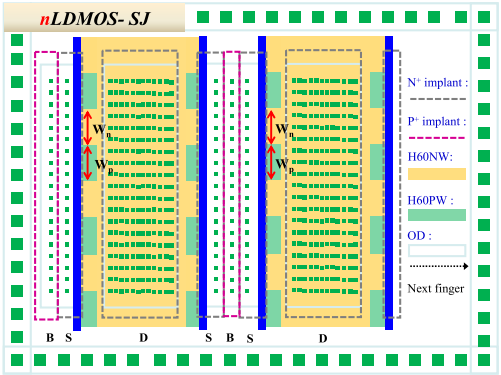

FIGURE 3. Layout-view diagram of an HV nLDMOS-SJ device.

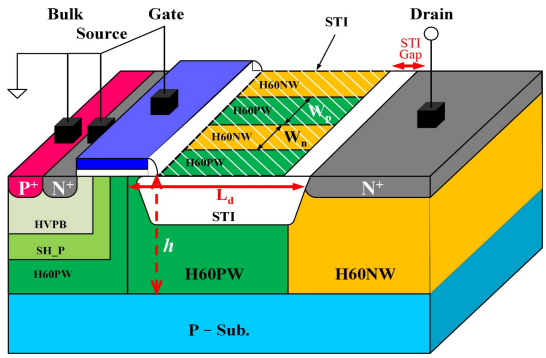

FIGURE 4. 3D Cross-sectional view of an HV nLDMOS-SJ device.

set to be equal. For a simplified and symmetrical device, the N^+/P^+ area ratio in the drain region was set to a unit value for the *p-n-p-* and *n-p-n*-arranged stripe SCR DUTs. According to this cross-sectional view, the nLDMOS with SJs (as in the previous section) was divided into three zones in the drain-end OD area. Next, the P^+ doses were then implanted into the first and third regions (central region) to form two (one) parasitic SCR devices, which was called the nLDMOS-SJ-SCR *p-n-p-* (*n-p-n-*) arranged structures. Furthermore, these embedded SCR current paths are denoted as SCR1 and SCR2 (SCR3) for the nLDMOS-SJ-SCR *p-n-p-* (*n-p-n-*) arranged types, respectively. Therefore, from Section II-A∼II-C, there are thirteen kinds of experimental group shown in Table 1. Eventually, we will determine the extent to which these layout designs at the drain end affect device reliability.

III. EQUIVALENT-CIRCUIT MODELS OF NLDMOS-SJ AND NLDMOS-SJ-SCRS

Adding an SJ structure into the nLDMOS will change the distribution of the depletion region in the drift region. This SJ structure can suppress the maximum peak electric field in the horizontal direction of the device. Of course, it can also change the electrical behavior of this new component. Therefore, from the device structure of Fig. 4, Fig. 9 shows an equivalent circuit of an nLDMOS with a super junction (SJ) structure, where the R'_{drift} variable

TABLE 1. Devices list of different testing sample types.

Sample Type	Structure	W of SJ (μm)	Embedded SCR
0	nLDMOS (Ref. DUT)	–	–
1, 2, 3, 4	nLDMOS-SJ	6, 9, 18, 27	–
5, 6, 7, 8	nLDMOS-SJ	6, 9, 18, 27	*p-n-p*
9, 10, 11, 12	nLDMOS-SJ	6, 9, 18, 27	*n-p-n*

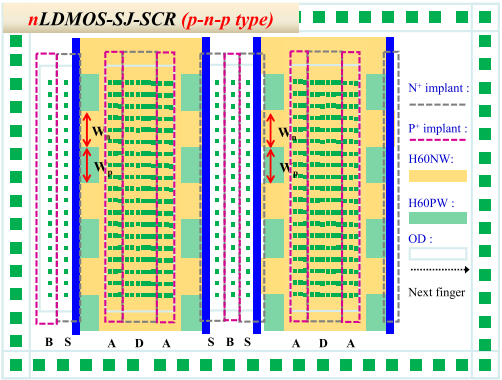

FIGURE 5. Layout-view diagram of an nLDMOS-SJ-SCR (*p-n-p*-arranged).

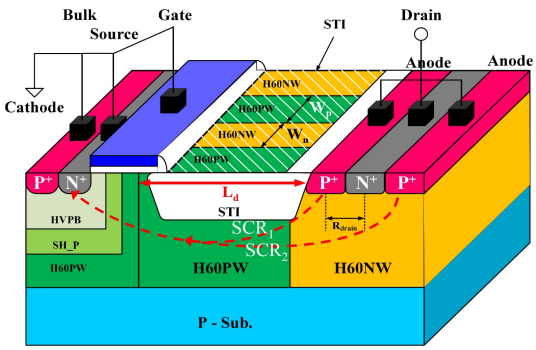

FIGURE 6. 3D Cross-sectional view of an nLDMOS-SJ-SCR (*p-n-p*-arranged).

resistance is a parasitic resistance in the drift region including the SJ modulation effect. Furthermore, it is assumed that the ON-resistance (R_{on}) of an nLDMOS can be approximately determined by the resistance of the lightly-doped drift region. Then, according to [29], the ON-resistance of the nLDMOS-SJ device can therefore be expressed as

$$R_{on} \cong R'_{drift} = K \cdot L_d^2 \frac{W}{h} \tag{2}$$

where K is a proportional constant, W and h are the width and height of SJ pillars, respectively.

For simplifying, the conduction weighting of two embedded SCRs in Fig. 6 (nLDMOS-SJ-SCR (*p-n-p*)) can be taken as dominated by the short path SCR_1. Based on the device structures, the equivalent circuits of nLDMOS-SJ-SCRs with *p-n-p-* and *n-p-n*-arranged structures are shown in Figs. 10(a) and 10(b), respectively. The main discrepancy between these two circuits is the location of the P^+implants of an SCR

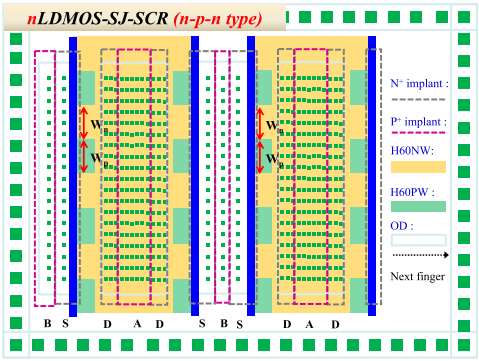

FIGURE 7. Layout-view diagram of an nLDMOS-SJ-SCR (*n-p-n*-arranged).

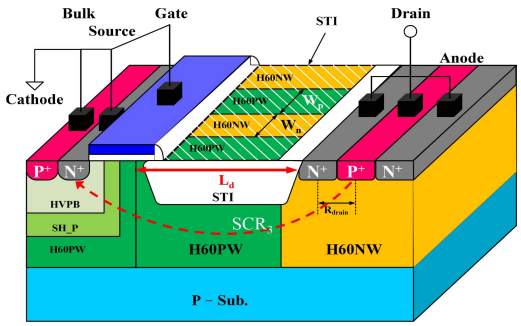

FIGURE 8. 3D Cross-sectional view of an nLDMOS-SJ-SCR (*n-p-n*-arranged).

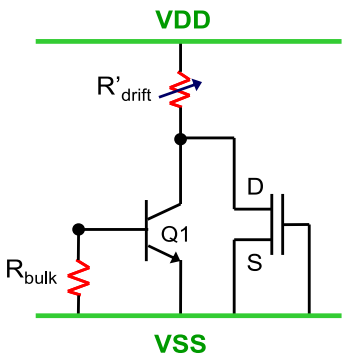

FIGURE 9. The equivalent circuit of an HV nLDMOS-SJ device.

anode. Due to the light doping in the drift region (the SJ structure effect included) and the considerable drain-side lateral spacing, the parasitic resistances of the drift region (R'_{drift}) (this impedance value is related to the SJ structure and changes accordingly) and the SCR-to-nLDMOS at the drain end (R_{drain}) are sufficiently high. Therefore, none of them can be neglected. Moreover, when the position of the P^+ anode region of the embedded SCR is adjusted, the equivalent circuits of the nLDMOS–SJ-SCR *p-n-p* and nLDMOS–SJ-SCR *n-p-n* arranged types change (Figs. 10(a) and 10(b)). Here, the red dashed lines indicate the more prone triggered conduction-on current path. The different P^+ anode changes will result in the two types to reveal dissimilar snapback characteristics.

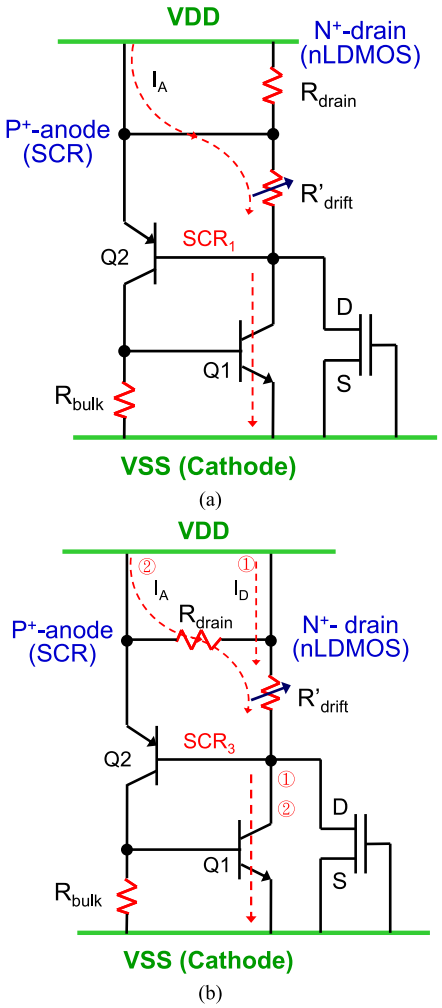

FIGURE 10. Equivalent circuits of the (a) nLDMOS-SJ-SCR (*p-n-p*-arranged type), and (b) nLDMOS-SJ-SCR (*n-p-n*-arranged type).

From Fig. 10(a), in the conduction-on holding situation of nLDMOS-SJ-SCR (*p-n-p*-arranged type), the Q1 and Q2 BJTs of the embedded SCR_1 are in a saturated condition. The voltage drop between anode-to-cathode electrodes (SCR_1 path) can be regarded as the $(V_h)_{p-n-p}$ (holding voltage of the *p-n-p*-arranged type). Then, the $(V_h)_{p-n-p}$ can be denoted as:

$$(V_h)_{p-n-p} \cong (V_{EB})_{Q2} + (V_{CE,sat})_{Q1} = I_A \times R'_{drift} + (V_{CE,sat})_{Q1}, \quad (3)$$

where I_A is the anode current (shown by the red dashed line) flowed through the right-hand branch during a triggered conduction-on condition.

For the nLDMOS-SJ-SCR *n-p-n*-arranged type, since the conduction path of the LDMOS is in front of the parasitic SCR (as shown in the path-① on the right side of Fig. 10(b)), the parasitic Q1 BJT of the nLDMOS will be turned on first. Eventually, the embedded SCR_3 will be turned on successively, and the conduction current will pass through the right-branch path of the SCR_3 (as indicated in the

path-②). Therefore, the $(V_h)_{n-p-n}$ of the nLDMOS-SJ-SCR (*n-p-n*-arranged type) can be described as:

$$(V_h)_{n-p-n} \cong (I_A \times R_{drain}) + (I_A + I_D) \times R'_{drift} + (V_{CE,sat})_{Q1}, \quad (4)$$

where I_D is the initial drain current of an nLDMOS flowed through the R'_{drift} branch (shown in Fig. 10(b)) during a triggered conduction-on condition.

IV. EXPERIMENTAL TESTING SYSTEM

A transmission-line-pulse (TLP) system with the human-body-model (HBM) like characteristic will be used to evaluate the snapback key parameters of these nLDMOS, nLDMOS-SJ and nLDMOS-SJ-SCR DUTs. This TLP tester is operated and fulfilled a convenient measurement by the LabVIEW interface, which controlled the electronic facilities of subsystem such as an ESD pulse generator, a multi-channel voltage supplier and a high-frequency digital oscilloscope. A TLP tester can provide a continuous step-high square pulse (100-ns pulse width) to a sample, and quickly rising/falling time (< 10-ns) of the continuous square wave can also follow the transient noise of an ESD incident. And, during the TLP leakage test after each TLP zapping, the reversed leakage-biased voltage (V_{LB}) was set to be 5 V.

V. EXPERIMENTAL DATA, DISCUSSIONS AND VERIFICATIONS

A. AN NLDMOS WITH SUPER-JUNCTION (SJ) STRUCTURES

By using a TLP tester, the leakage and snapback current–voltage (I–V) curves of power nLDMOS and nLDMOS-SJ samples with various W types are presented in Fig. 11. In addition, the V_{t1}, V_h, and I_{t2} data behaviors are listed and shown in Table 2 and Fig. 12. The I_{t2} value is not favorable (only 1.632 A) for the nLDMOS reference device. Because of the influence of series SJs of an nLDMOS in the drain side (resulting in the R'_{drift} impedance change shown in Fig. 9), it was found that the nLDMOS-SJs have higher I_{t2}, V_h, and FOM values. The layout of SJs in the drain side has positive effects on ESD and LU capabilities. Compared with the pure nLDMOS DUT used as a reference, the nLDMOS-SJ DUT with $W_n = W_p = W = 9\mu$m has the highest I_{t2} value. The I_{t2} (V_h) values of such an arrangement are favorable for the ESD and LU immunities (enhanced reaching 46.3% (13.3%)) compared to the reference DUT.

B. AN NLDMOS-SJ WITH EMBEDDED SCR STRUCTURES

The leakage and snapback I–V curves of power nLDMOS-SJ DUTs with different *p-n-p-* and *n-p-n*-arranged SCRs in the drain side are presented in Figs. 13(a) and 13(b). In addition, the V_{t1}, V_h, and I_{t2} testing data are indicated in Table 3. Compared with the *n-p-n*-arranged SCR in this structure, the parasitic SCR of *p-n-p*-arranged type had a lower V_{t1} value, which was due to a shortest conduction path.

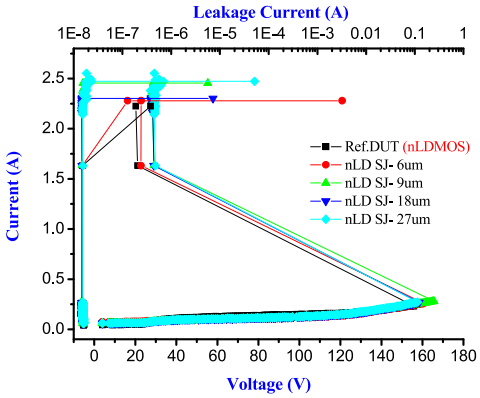

FIGURE 11. Leakage and snapback I-V curves of nLDMOS-SJ DUTs.

TABLE 2. Snapback key parameters of nLDMOS and nLDMOS-SJ DUTs.

nLDMOS + SJ	V_{t1} (V)	V_h (V)	I_{t2}(A)	FOM (μA×V /μm²)
Ref_nLDMOS	156.961	21.071	1.632	2471.25
SJ W= 6 μm	160.241	21.907	1.632	2569.29
SJ W= 9 μm	162.355	23.864	2.387	4093.62
SJ W= 18 μm	158.578	29.281	2.296	4831.36
SJ W= 27 μm	157.62	29.76	2.346	4980.07

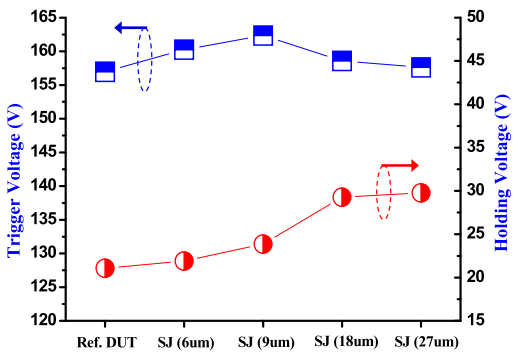

FIGURE 12. V_{t1} & V_h values charts of nLDMOS-SJ DUTs.

Because of the influences of *p-n-p-* and *n-p-n*-arranged SCR structures of nLDMOS-SJ in the drain side, the nLDMOS-SJ-SCR *p-n-p-* (*n-p-n-*) type DUTs have higher (lower) I_{t2} values than the corresponding nLDMOS-SJ samples. The highest FOM value of the *p-n-p* type SCR is favorable for ESD and LU reliabilities, which upgraded reaching 13.72% compared to the nLDMOS-SJ ($W_n = W_p = W = 27\mu$m) DUT. Conversely, the highest FOM value of the *n-p-n* type SCR is disadvantageous for the ESD and LU immunities (downgraded reaching 18%) compared to the nLDMOS-SJ ($W_n = W_p = W = 27\mu$m) sample.

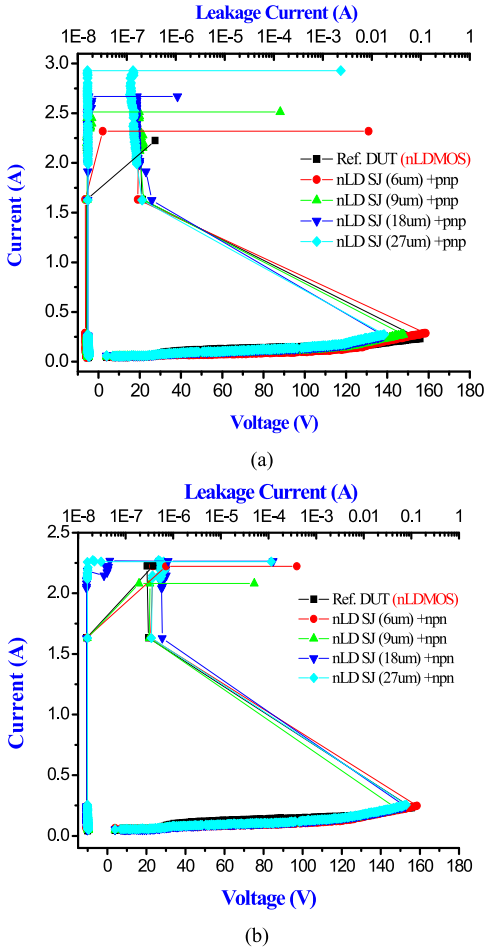

FIGURE 13. Leakage and snapback I-V curves of nLDMOS-SJ-SCR DUTs with the (a) *p-n-p-* and (b) *n-p-n*-arranged manner.

TABLE 3. Snapback key parameters of nLDMOS and nLDMOS-SJ-SCR DUTs.

nLDMOS + SJ + SCR		V_{t1} (V)	V_h (V)	I_{t2} (A)	FOM ($\mu A \times V / \mu m^2$)
Ref_nLDMOS		156.961	21.071	1.632	2471.25
p-n-p type	SJ W= 6 μm	153.336	18.954	1.632	2222.96
	SJ W= 9 μm	147.903	21.799	2.471	3870.97
	SJ W= 18 μm	138.208	23.869	2.847	4883.51
	SJ W= 27 μm	137.711	24.369	3.234	5663.54
n-p-n type	SJ W= 6 μm	153.894	20.877	1.631	2446.99
	SJ W= 9 μm	152.769	21.377	1.631	2505.6
	SJ W= 18 μm	152.043	24.980	2.228	3999.61
	SJ W= 27 μm	151.689	25.391	2.238	4083.67

C. VERIFICATIONS BY EQUIVALENT-CIRCUIT MODELS OF NLDMOS-SJS AND NLDMOS-SJ-SCRS

Since the holding voltage (V_h) of a transistor device is proportional to the ON-resistance (R_{on}) of the device, it can be clearly found from Equation (2) that with the addition of SJ structures in the drain side, the V_h values of nLDMOS-SJs and nLDMOS-SJ-SCR devices do have a certain proportional relationship with the SJ width (W). This is consistent with the experimental data in Tables 2 and 3. However, for the nLDMOS-SJ sample with SJ $W = 6\mu m$, the width may be too small, so the corresponding V_h value does not increase significantly in Table 2. More importantly, after adding this SJ structure to nLDMOS devices, both the $V_h$and I_{t2} values will increase, which is helpful to strengthen the ESD and LU (& FOM) reliability capabilities of nLDMOS devices.

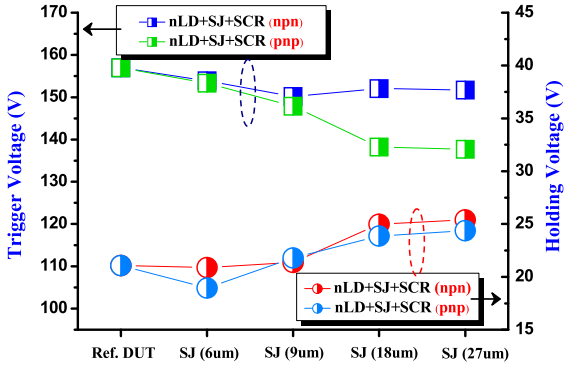

FIGURE 14. V_{t1} & V_h values charts of Ref. DUT, nLDMOS-SJ and nLDMOS-SJ-SCR DUTs.

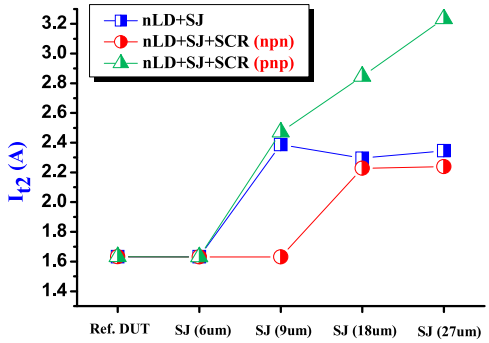

FIGURE 15. I_{t2} values charts of Ref. DUT, nLDMOS-SJ and nLDMOS-SJ-SCR DUTs.

In order to let the nLDMOS-SJ-SCRs behaviors of the V_{t1}, V_h, and I_{t2} data more clearer, the measured data in Table 3 are re-plotted again as shown in Figs. 14 and 15. Compared with Tables 2-3 and Figs. 14-15, as a result of lower trigger voltage and conduction-on resistance of SCR contribution in the nLDMOS-SJ-SCR compound devices, the snapback parameters of V_{t1} or V_h value for the *p-n-p-* or *n-p-n*-type of an nLDMOS-SJ-SCR compound device will be lower than that of the corresponding nLDMOS-SJ sample. The decrease of holding voltage (V_h) will weaken the ability of power components or circuits to prevent LU. In addition, due to the series-resistance R_{drain} influence, a trigger current for the *p-n-p-* (*n-p-n-*) type flowed through the SCR_1 (SCR_3) anode conduction-on current path, as shown in Fig. 10(a) (10(b)). The V_{t1} value of the nLDMOS-SJ-SCR *n-p-n* type is higher than that of the corresponding *p-n-p* type. Similarly, from

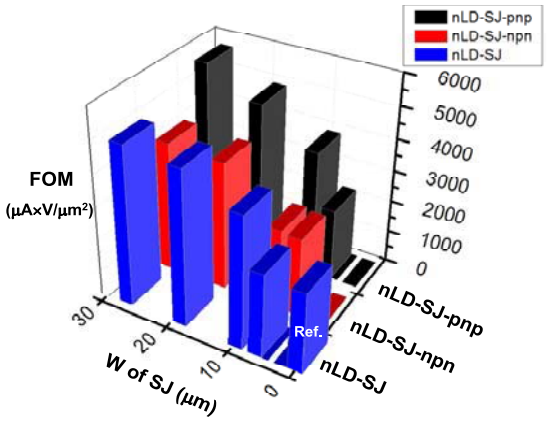

FIGURE 16. 3D diagram of FOM impacts as the W varied in Ref. DUT, nLDMOS-SJ and nLDMOS-SJ-SCRs DUTs.

Equations (3) and (4), the V_h value of the *n-p-n* type is greater than that of the *p-n-p* type in the nLDMOS-SJ embedded SCR structures.

At the same time, without going into detailed, the I_{t2} values (ESD ability) of the nLDMOS-SJ-SCR *p-n-p*-arranged type are higher than those of the corresponding samples of the nLDMOS-SJ-SCR *n-p-n*-arranged type for smaller series resistance of the SCR. In other words, in the ESD strengthening consideration, a best arrangement of embedded SCR in the nLDMOS drain-side is the *p-n-p*-arranged type. But from the standpoint of LU reliability, the *n-p-n*-arranged type is better. Finally, in terms of ESD and LU reliability trade-offs, that is the FOM consideration shown in Fig. 16, the disadvantage of the *p-n-p*-arranged type in LU can be compensated by adding SJ in the drift region. Obviously, in the nLDMOS-SJ-SCR devices, whether it is a *p-n-p-* or an *n-p-n*-arranged type, the best FOM device should have the best I_{t2} and V_h performances. From Equations (1)-(4) and Table 3, it is clear that an nLDMOS-SJ-SCR *p-n-p*-arranged device with SJ structure and $W = 27\mu$m is the most reliable ESD/LU best choice (it has the highest I_{t2} and V_h values). Therefore, it can be concluded that the nLDMOS-SJ-SCR could be a good drain architecture for the ESD/LU robustness, especially for the *p-n-p*-arranged type as compared with the pure nLDMOS (Ref. DUT).

VI. CONCLUSION

This study combines two effective techniques and with different layout architectures in the drain side to improve the ESD and LU reliabilities of HV nLDMOS transistors. One of the techniques is to use the SJ structure in the drain side of an nLDMOS, which can be effectively used to strengthen the I_{t2} and V_h values of the device. Therefore, the ESD and LU capabilities of the nLDMOS-SJ device are increased. Furthermore, compared with the corresponding nLDMOS-SJ samples, if the drain side of the nLDMOS-SJ-SCR compound devices are embedded with a *p-n-p-* (*n-p-n-*) arranged type SCR, the I_{t2} data will be upgraded (degraded). Subsequently, their corresponding ESD capabilities were enhanced (decreased). However, in both of these scenarios, V_{t1} and V_h values are reduced compared with the corresponding nLDMOS-SJ samples. Therefore, it can be concluded that a drain side with a parallel SJ structure is favorable for ESD and LU reliabilities. However, the drain side *p-n-p-* (*n-p-n-*) arranged type SCR is favorable (unfavorable) for the ESD current conduction. In summary, for the considerations of ESD and LU reliability (i.e., FOM), the parallel SJ integrated with an SCR *p-n-p*-arranged type at the drain end of the power nLDMOS is an optimal strategy.

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