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GaN Nanotube FET With Embedded Gate for High Performance, Low Power Applications

KE HAN (Member, IEEE), JIAWEI LI, ZHONGLIANG DENG (Senior Member, IEEE), YANNAN ZHANG, AND SHANGLIN LONG

School of Electronic Engineering, Beijing University of Posts and Telecommunications, Beijing 100876, China

CORRESPONDING AUTHOR: K. HAN (e-mail: hanke@bupt.edu.cn)

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ABSTRACT On the road of CMOS device continuously scaling, there are lots of challenges regarding the device structure and material engineering. GaN channel has recently been used in MOSFETs and achieved excellent performance. In this paper, we study a novel embedded gate GaN nanotube field effect transistor of 5 nm gate length with I_{ON}/I_{OFF} as high as 10^6, and subthreshold swing (SS) as small as 64 mV/dec using Sentaurus TCAD simulation. The device can effectively improve subthreshold characteristics due to the GaN channel and embedded gate design. Compared with Si nanotube FET and GaN nanowire FET, GaN embedded nanotube FET exhibits low SS and high I_{ON}/I_{OFF} at the same channel thickness. GaN embedded nanotube FET has also been determined to superior temperature adaptability and performs better in terms of threshold voltage and subthreshold characteristics compared to Si nanotube FET at the same temperature. In addition, we investigated the impact of different lengths and thicknesses of the embedded gate on the subthreshold characteristics. As the length and thickness of the embedded gate are increased, SS and I_{ON}/I_{OFF} are improved. This excellent electrical performance demonstrates the possibility of GaN as a channel material in MOSFETs and embedded gate as an effective design to improve subthreshold characteristics, opening a new way for continued device scaling.

INDEX TERMS GaN, embedded gate, nanotube FET, subthreshold characteristic.

I. INTRODUCTION

As the size of MOSFETs is approaching the limit of scaling, other possibilities for improving device performance have been widely explored in recent years. At the same time, short channel effects and parasitic components caused by scaling can result in performance degradation. Researchers have proposed many device structures with better performance at the same size, such as FinFET, dual gate, GAA [1]–[3]. GAA is considered to be the most promising candidate due to its excellent short channel control capabilities [4]. Despite the excellent results achieved in gate control and other aspects, the GAA structure still has some shortcomings that need to be improved. First, as the channel thickness increases, device performance will seriously decrease. For example, when the channel thickness increases above 6 nm, the SS of the GAA structure and I_{ON}/I_{OFF} will degrade significantly [5]. Secondly, as the channel length is scaled to 5nm and below, the control of the gate to the channel decreases, and the subthreshold characteristics of the GAA structure are also affected. In order to solve the above problems, we propose a novel GaN nanotube with the embedded gate called GaN embedded nanotube FET. GaN embedded nanotube FET replaces the substrate of GAA with the inner gate as the second gate and provides effective charge control [6]. GaN as a channel material has a wide electronic band gap, which can significantly reduce inter-band tunneling and gate induced drain leakage, thus providing excellent subthreshold characteristics for GaN embedded nanotube FET [7], [8]. In addition, the electric field across the channel region becomes stronger as the embedded gate structure, leading to the enhancement of the gate control [9]. Therefore, GaN embedded nanotube FET exhibits exceptional electrical

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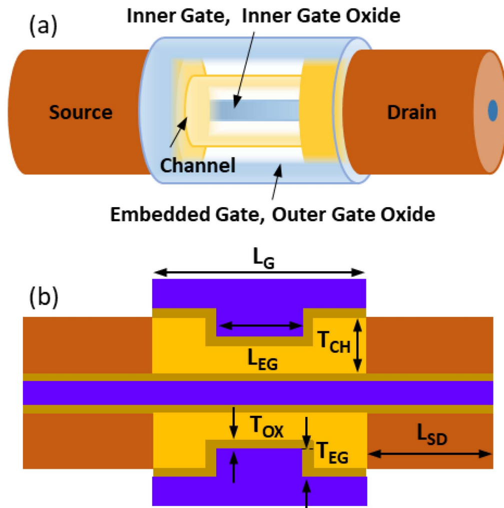

FIGURE 1. (a) 3-D structure Schematic of GaN nanotube FET with embedded gate. (b) 2-D vertical cross-section diagram of the device.

performance, of which subthreshold characteristics are better than Si nanotube FET.

In this work, we present the performance of GaN embedded nanotube FET with different channel thicknesses and temperatures compared to other structures and the impact of the embedded gate length and thickness on GaN embedded nanotube FET, and demonstrate that the device has excellent device performance and superior scaling capacity.

II. DEVICE STRUCTRUE AND SIMULATION APPROACH

All the experiments are performed using the numerical device simulation tools Sentaurus TCAD with Drift-Diffusion, Density-Gradient, Philips Unified Mobility and Hurkx Trap Assisted Tunneling models [10], [11]. Considering the effect of quantum effects on the nanometer scale, we used the quantum potential model in the simulation. Besides, we use band gap narrowing model to simulate the source and drain are highly doped [12]. Fig. 1 shows the 3-D schematic of the GaN embedded nanotube FET and the corresponding 2-D cross-section diagram. The device is comprised of the source, channel, drain, outer embedded gate, inner gate, and gate oxide. The inner gate is located at the center of the structure, and surrounded by the inner gate oxide layer. HfO_2 as the gate oxide layer material provides for high dielectric constant and large band gap width, which can effectively solve the problem of poor reliability caused by the reduction of gate oxide thickness [13], [14]. The source, channel, and drain is formed surrounding the gate oxide layer. GaN is used as the channel material because of which having higher electron mobility and wider band-gap than Si. The channel is surrounded by the outer gate oxide layer and embedded gate. The comparison of the embedded gate and traditional gate structure is shown in Fig. 2. Different from traditional gate, part of the outer gate and gate oxide layer of GaN embedded nanotube FET is embedded in the channel to enhance the electric field in the region and improve the gate control capability of the device. Metal is used as the gate material

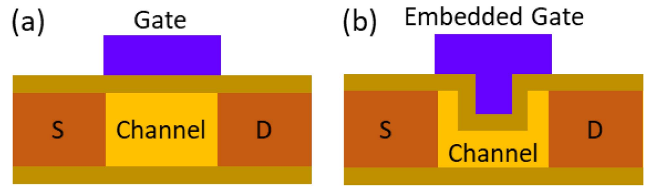

FIGURE 2. Schematic diagram of (a) traditional outer gate structure and (b) embedded outer gate structure.

TABLE 1. GaN embedded nanotube FET structural parameter used in simulation.

Symbol	Quantity	Value
L_G	Gate Length	5 nm
T_{CH}	Channel Thickness	1.8 $\rightarrow$ 2.4 nm
T_{EG}	Embedded Gate Thickness	0.15 nm
T_{OX}	Oxide Thickness	0.7 nm
L_{SD}	Source/Drain Length	10 nm
N_{SD}	Doping in S/D region	1×10^{20} cm^{-3}
N_{CH}	Channel Doping	1×10^{15} cm^{-3}

because it has the property of a work function that varies with fabrication process [15]. The important device parameters for the experimental are listed in Table 1. Si nanotube FET has the same dimensions and is simulated at the drain voltage of 1V to compare device performance with GaN embedded nanotube FET at different channel thicknesses. GaN embedded nanotube FET can be fabricated according to the process flow for conventional GaN nanowire FET in [16], [17], using an embedded gate instead of the outer gate and introducing an inter gate. Therefore, compared with GaN nanowire FET proposed in [16], [17], the manufacture of GaN embedded nanotube FET will not too difficult. In addition, we also show the suggested fabrication process flow in Fig. 3 for replacing the conventional nanowire structure with an embedded gate nanotube structure on the process flow suggested in [18].

III. SIMULATION AND RESULT

Fig. 4 shows the impact of the channel thickness on SS and I_{ON}/I_{OFF} of Si nanotube FET and GaN embedded nanotube FET. I_{DS}-V_{GS} transfer characteristics of Si nanotube FET and GaN embedded nanotube FET with $T_{CH} = 1.8$ nm is as shown in Fig. 4(a). For the same channel thickness, we can find that I_{ON} of the Si nanotube FET is inferior than GaN embedded nanotube FET and I_{ON} gradually decreases as the channel thickness increases. Fig. 4(b) shows that as the channel thickness increases, SS increases. Meanwhile, higher electron mobility enables better gate control for GaN. Therefore, SS of the GaN embedded nanotube FET is always lower than that of the Si nanotube FET, and SS decays more slowly as the channel thickness increases. As shown in Fig. 4(c), we can find that I_{ON}/I_{OFF} decreases as channel thickness increases, and I_{ON}/I_{OFF} of GaN embedded nanotube FET is higher than that of Si nanotube FET.

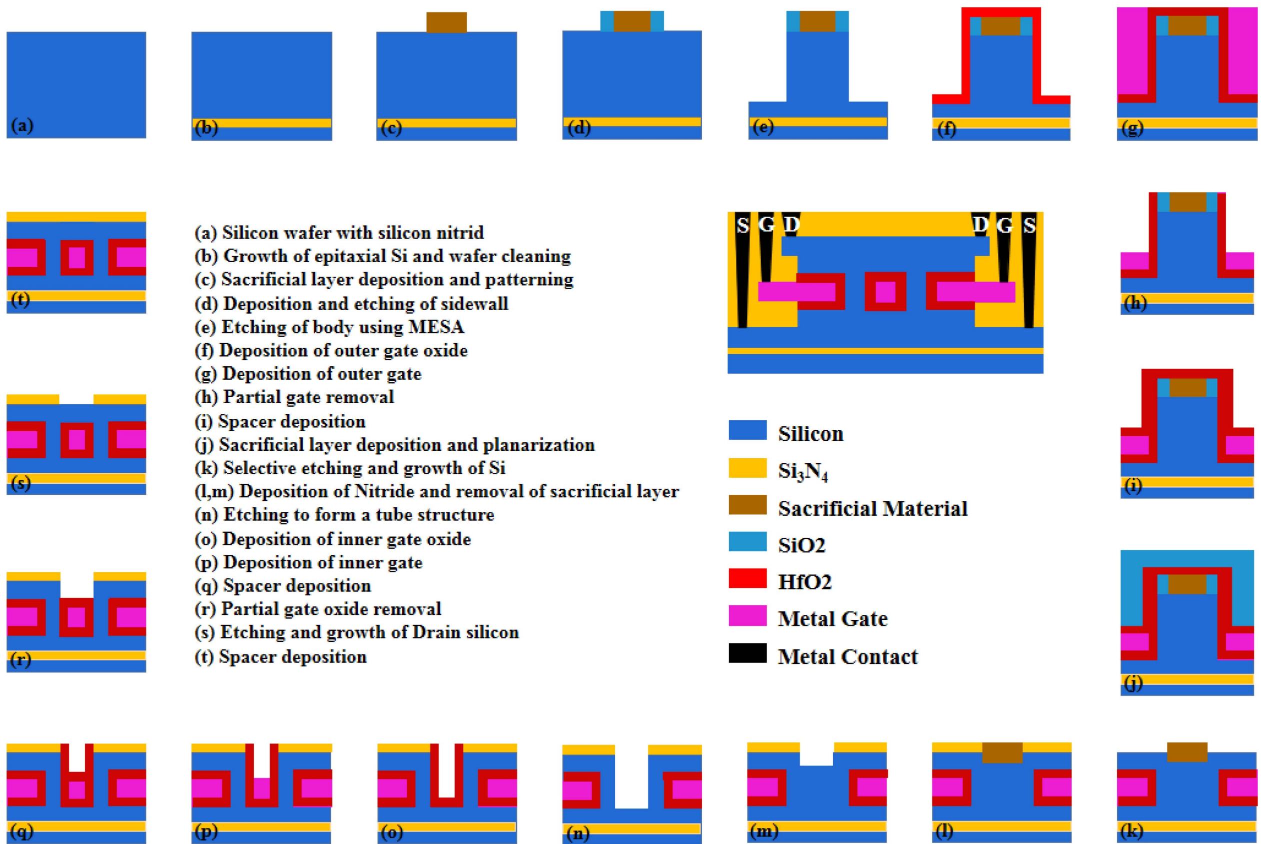

FIGURE 3. Suggested fabrication process flow for embedded nanotube FET.

Fig. 4(d) compared I_{OFF} of Si nanotube FET and GaN embedded nanotube FET at different channel thicknesses. I_{OFF} of the GaN embedded nanotube FET is significantly lower compared to the Si nanotube FET. These results indicate that GaN embedded nanotube FET exhibits more excellent performance in terms of subthreshold characteristics compared to Si nanotube FET for the same channel thickness.

By comparing GaN embedded nanotube FET and GaN nanowire FET with the same channel thickness, we find that the embedded gate demonstrates significant enhancement in gate control, thereby improving the electrical performance of the device compared with traditional gate structure. We compared GaN embedded nanotube FET and GaN nanowire FET at $T_{CH} = 1.6$ nm. The SS is 63.8 mV/dec and 67.2 mV/dec and I_{ON}/I_{OFF} is 4.5×10^6 and 2.2×10^6 for the GaN embedded nanotube FET and GaN nanowire FET, respectively (see Table 2) [8].

Fig. 5 shows the impact of the temperature on the subthreshold characteristics of the Si nanotube FET and GaN embedded nanotube FET. Fig. 5(a) and (b) show that GaN embedded nanotube FET exhibits superior SS and I_{ON}/I_{OFF} than Si nanotube FET at the same temperature. I_{OFF} of the GaN embedded nanotube FET is significantly lower than Si nanotube FET in Fig. 5(c). As the decrease in electron mobility with temperature increases,

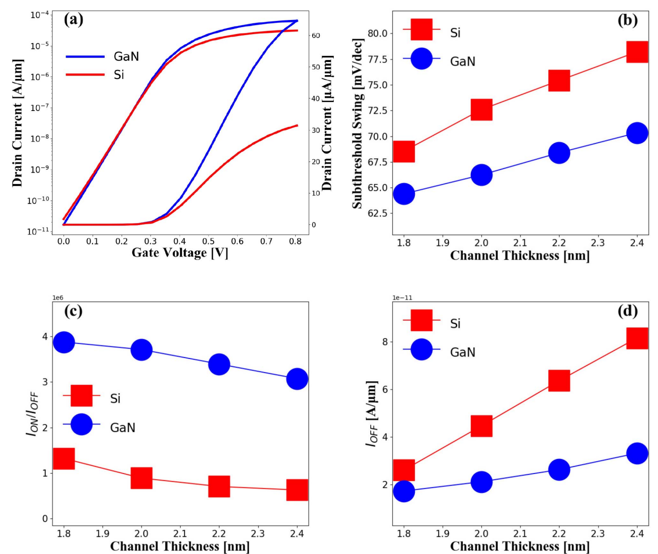

FIGURE 4. (a) I_{DS}-V_{GS} transfer characteristics of Si nanotube FET and GaN embedded nanotube FET with $T_{CH} = 1.8$ nm. (b) SS of the GaN embedded nanotube FET and Si nanotube FET at different channel thicknesses. Comparison of (c) I_{ON}/I_{OFF} and (d) I_{OFF} of Si nanotube FET and GaN embedded nanotube FET with different channel thicknesses.

the subthreshold characteristics deteriorate. On the other hand, GaN has a wide band gap allowing for high temperature operation [19]. GaN embedded nanotube FET is less

TABLE 2. Performance comparison of GaN embedded nanotube and GaN nanowire [8] at the same channel thickness.

Performance metrics	GaN nanowire	GaN embedded nanotube
SS(mV/dec)	67.2	63.8
I_{ON}/I_{OFF}	2.2×10^6	4.5×10^6

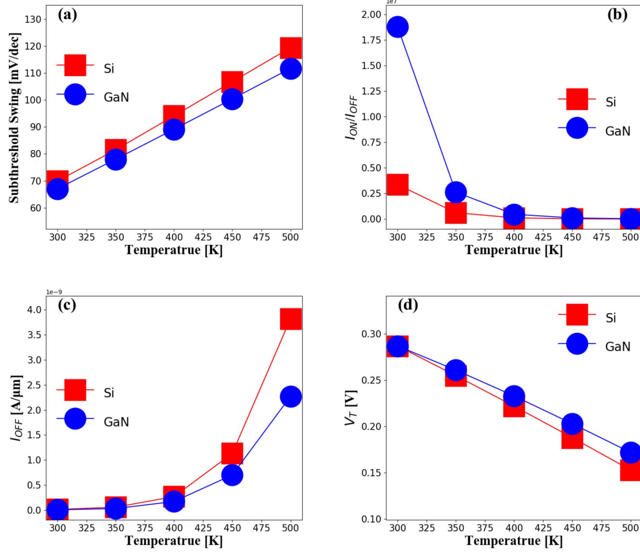

FIGURE 5. (a) SS comparison for Si nanotube FET and GaN embedded nanotube FET at different temperatures. Comparison of (b) I_{ON}/I_{OFF} and (c) I_{OFF} of Si nanotube FET and GaN embedded nanotube FET with different temperatures. (d) Threshold voltages of the GaN embedded nanotube FET and Si nanotube FET at different temperatures.

affected by temperature than Si nanotube FET. Fig. 5(d) shows that threshold voltage (V_T) decreases as the temperature increases, and V_T roll-off of GaN embedded nanotube FET is lower than Si nanotube FET.

To further investigate the impact of embedded gate on the subthreshold characteristics, we simulated GaN embedded nanotube FET with the embedded gate of different lengths and thicknesses at $L_G = 10$ nm and $T_{CH} = 5$ nm. The dimensions of the device are expanded to make it easier to adjust the size of the embedded gate. Fig. 6 shows the I_{DS}-V_{GS} transfer characteristics of GaN embedded nanotube FET with different embedded gate lengths at $T_{EG} = 1.5$ nm. Compared with the traditional gate structure ($L_{EG} = 0$ nm), the subthreshold characteristics of the embedded gate structure has been significantly improved, and as the embedded gate length increases, the contact area between the gate and the channel becomes larger, SS and I_{ON}/I_{OFF} having also been further improved. For GaN embedded nanotube FET, the length of the embedded gate can increase the contact area between the gate and the channel, thereby enhancing the control of the channel by the gate. Therefore, increasing the length of the embedded gate can improving the subthreshold characteristics. Fig. 7(a) shows that SS decreases as the embedded gate length increases. The

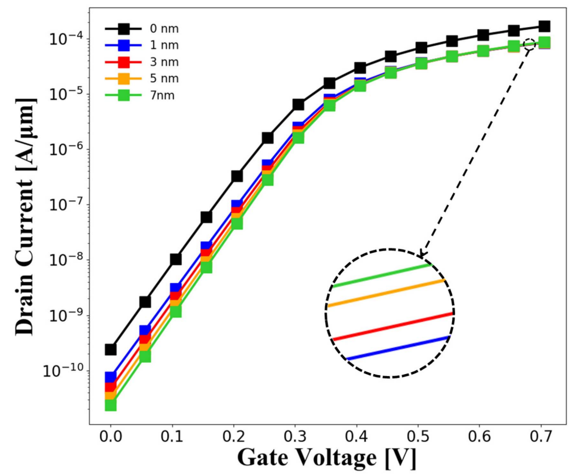

FIGURE 6. I_{DS}-V_{GS} transfer characteristics of GaN embedded nanotube FET with different embedded gate lengths.

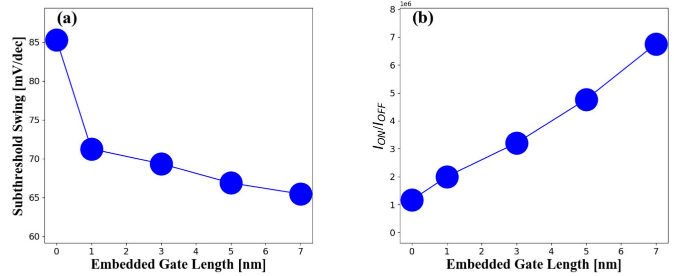

FIGURE 7. Impact of embedded gate thickness (L_{EG}) on subthreshold characteristics of the GaN embedded nanotube FET. (a) Subthreshold swing. (b) I_{ON}/I_{OFF}.

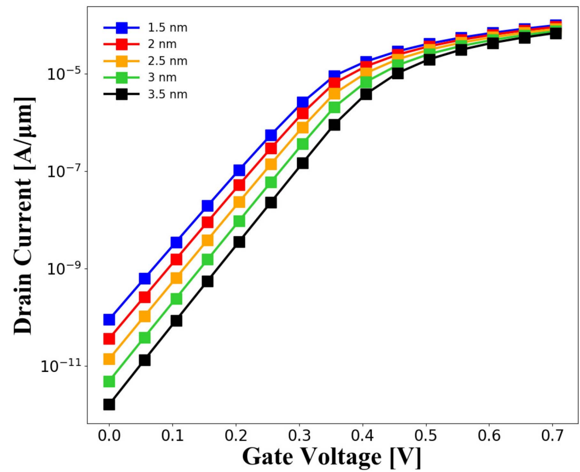

FIGURE 8. I_{DS}-V_{GS} transfer characteristics of GaN embedded nanotube FET with different embedded gate thicknesses.

SS of GaN embedded nanotube FET at $L_{EG} = 0$ nm is about 85.3 mV/dec. When the length of the embedded gate increases to 7 nm, SS shows a minimum value of 65.4 mV/dec. As shown in Fig. 7(b), I_{ON}/I_{OFF} are 1.2×10^6 and 6.7×10^6 at the embedded gate lengths of 0 nm and 7 nm, respectively.

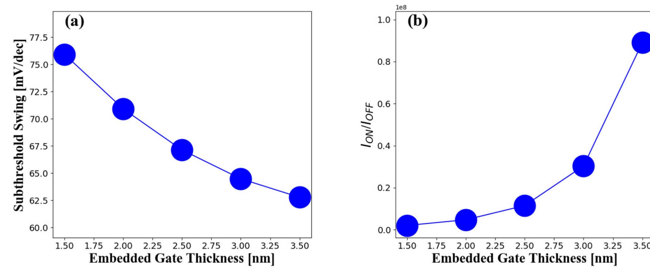

FIGURE 9. Impact of embedded gate thickness (T_{EG}) on subthreshold characteristics of the GaN embedded nanotube FET. (a) Subthreshold swing. (b) I_{ON}/I_{OFF}.

Fig. 8 shows the I_{DS}-V_{GS} transfer characteristics of GaN embedded nanotube FET with different embedded gate thicknesses at $L_{EG} = 5$ nm. Fig. 9(a) shows that SS decreases as the embedded gate thickness increases. As the embedded gate thickness increases, the cross-sectional area of the channel becomes narrower and the electric field across the channel region becomes stronger, thereby SS decreases and I_{ON}/I_{OFF} increases. The embedded gate thickness increases from 1.5 nm to 3.5 nm, and SS decreases from 75.9 mV/dec to 62.8 mV/dec. The impact of different embedded gate thicknesses on I_{ON}/I_{OFF} of the GaN embedded nanotube FET is shown in Fig. 9(b). Obviously, thin embedded gate thickness renders low I_{ON}/I_{OFF}.

IV. CONCLUSION

In this work, we proposed a novel GaN nanotube with embedded gate and simulated the subthreshold characteristics of GaN embedded nanotube FET with different channel thicknesses and temperatures compared to Si nanotube FET using Sentaurus TCAD simulation. GaN embedded nanotube FET provides excellent immunity to short channel effects and temperature adaptability with the GaN channel and embedded gate design. In addition, the impact of the length and thickness of the embedded gate on SS and I_{ON}/I_{OFF} of GaN embedded nanotube FET are investigated. The results show that longer and thicker embedded gate can improve the subthreshold characteristics of the device. Therefore, GaN embedded nanotube FET can be regarded as one of the promising candidates to extend CMOS scaling roadmap in sub-5 nm node.

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