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# Edge-Etched $Al_2O_3$ Dielectric as Charge Storage Region in a Coupled MIS Tunnel Diode Sensor

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**ABSTRACT** The effects of an $Al_2O_3$ dielectric patterned by wet etching in a metal-insulator-semiconductor (MIS) tunnel diode are studied by I-V, C-V and charge storage characteristics in this paper. The behaviors are obviously different from the device without an etched edge. It is suggested that traps are formed at the edge because of the etching process. A circuit model is proposed to explain the effect of the existence of additional traps. With the etched edge as charge storage region, current ratio of programmed and erased states of the tunnel diode sensor is expanded for 165 times and the retention characteristic is much improved. Meanwhile, charge storage characteristic varies with the thickness of the $Al_2O_3$ dielectric. Multilevel demonstration is carried out by specified programming process which is not feasible on coupled MIS previously. In addition, relation between the sensing current and stress conditions is examined. A maximum on/off ratio of $10^5$ is achieved. The study of the etched edge is believed to be beneficial for future development in memory cell constructed by MIS TD.

**INDEX TERMS** Metal–insulator–semiconductor (MIS), tunnel diode, edge-etched dielectric, current window enlargement, retention time improvement.

## I. INTRODUCTION

Several applications such as solar cells, temperature sensors and memory devices [1]–[4] are carried out by metal-oxide-semiconductor (MIS) tunnel diodes because their oxide-tunneling currents are highly sensitive to surrounding signals. Charge-coupled MIS tunnel diode consists of separated storage and remote sensing design is proposed in [5] to mitigate read disturbance which is common in existing technologies like FLASH memory. Fig. 1 shows the schematic of the charge-coupled MIS tunnel diode. The drain part is an MIS(p) tunnel diode (TD) with ultrathin oxide. The tunneling current of a reversely biased MIS TD is dominated by the massive hole tunneling current which is due to the large fringing effect in the device edge. It should be noted that the large fringing field causes the hole current flows at the edge of device and the bulk generation current is only the small part of total current [3], [6]. The hole current can be modulated by minority carriers nearby which control the effective Schottky barrier height of holes [7], [8].

The tunneling hole current at positive bias can be expressed as the following equations [2]:

$$I_h \propto exp\left(\frac{-q\phi_h^*}{kT}\right) \tag{1}$$

where $q\phi_h^*$ can be expressed as [8], [9]

$$q\phi_h^* = q\chi_s - q\Phi_m + E_g - qV_{ox} \tag{2}$$
$$\phi_h^* = \phi_{h0} - \Delta\phi_h \tag{3}$$
$$\Delta\phi_h = B|J_{n,diff}|d_{ox} = BqF_e d_{ox} \tag{4}$$

$\phi_h^*$ is the effective Schottky barrier height (SBH) of majority carriers, $q\Phi_m$ and $q\chi_s$ are the work function of gate metal and the electron affinity of semiconductor, respectively, $E_g$ is the bandgap of semiconductor, $V_{ox}$ is the oxide voltage drop, $\phi_{h0}$ is the Schottky barrier height of holes without considering the effect of lateral diffusion current, B is a constant, $J_{n,diff}$ is the lateral diffusion current of minority carriers and $\Delta\phi_h$ is the lowering of SBH related to $J_{n,diff}$. $F_e$ is the lateral flux of minority carriers from the outer TD. $Q_e$ in

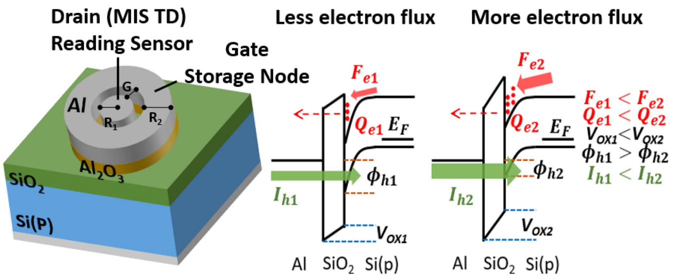

**FIGURE 1.** Schematic of the charge-coupled MIS tunnel diode. Inner circle is defined as drain while the outer ring is defined as gate. The band diagrams of drain on vertical direction as the voltage biased at saturation region under two different quantities of coupled minority carriers are also shown. Effective Schottky barrier height modulation effects are demonstrated. $R_1$ is 85 um, $R_2$ is 500 um, and the gap G is 15 um.

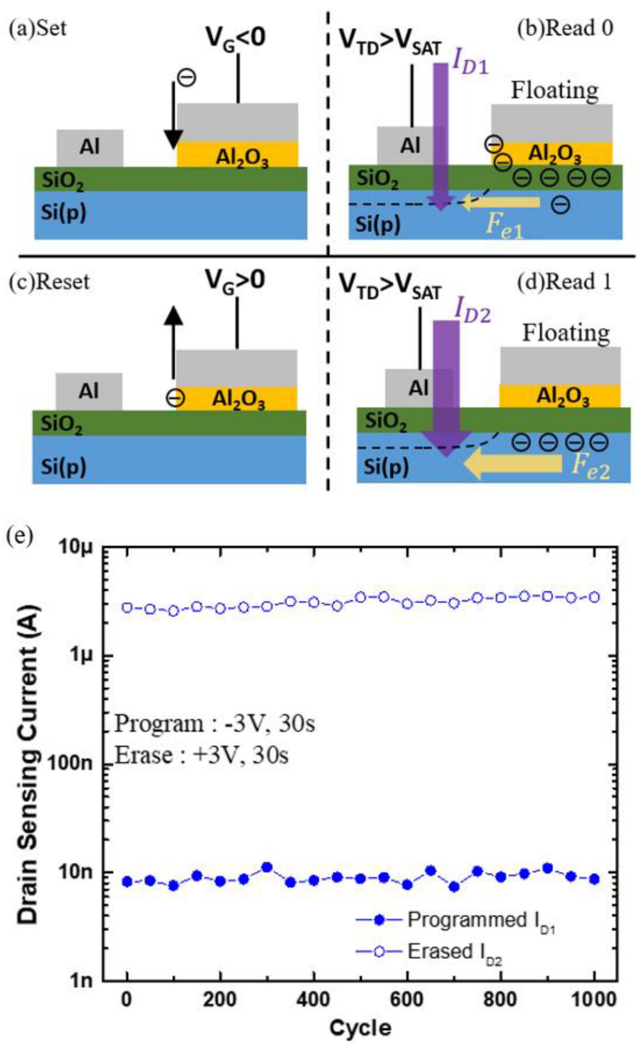

**FIGURE 2.** Memory operation procedure. (a) Trapping electrons in gate edge is defined as program. (b) Minor current is sensed at drain edge. (c) Removing electrons previously trapped in gate edge is defined as erase. (d) Larger current is sensed. The dotted line in (b) and (d) indicates the boundary of depletion region which results in electric sensing field at drain. (e) The endurance characteristic of the proposed MIS TD coupled with single-layer edge-etched $Al_2O_3$.

Fig. 1 is the minority carrier concentration affected by $F_e$. Equations (2), (3) and (4) can be explained by the band diagram shown in Fig. 1. With more supply of minority carriers, the larger $V_{ox}$ is, the lower Schottky barrier height of the holes, resulting in massive hole current injecting from the metal into the substrate. The lateral diffusion current $J_{n,diff}$ is positively related to the inversion charges under the gate which can be controlled by the charges stored in the gate dielectric. The electrons provided by the lateral diffusion current will not diffuse into the bulk region due to the edge fringing field [10].

However, the dielectric of sensing structure in [5] is constructed by $Al_2O_3/HfO_3/SiO_2$ (AHO) which declines the tunneling probability and suppresses the sensing current. Dielectric constructed only by silicon oxide at drain is preferred to lower the sensing voltage due to energy consideration.

In this work, $Al_2O_3$ is chosen as the surrounded gate dielectric to improve the memory performance of a charge-coupled MIS tunnel diode. $Al_2O_3$ has the merits of similar bandgap and band alignment with $SiO_2$ and a dielectric constant of about 9. A layer of $Al_2O_3$ is deposited and etched on the silicon oxide of gate.

In the $Al_2O_3/SiO_3$ stacked dielectric, it is believed that defects are generated in the interface after High-K dielectric layer formation [11]. Charges can be captured by the defects existed in the $Al_2O_3/SiO_2$ by voltage stress and give rise to memory phenomenon [11]. Defects such as Al vacancies ($V_{Al}$), oxygen vacancies ($V_O$), Al interstitials ($Al_i$), and oxygen interstitials ($O_i$) in the $Al_2O_3$ dielectrics are located at or near the interface [12], [13]. Another type of point defect also occurs in amorphous $Al_2O_3$, namely dangling bonds. The defect is a possible cause of traps, leakage, and fixed charges. Besides, a high density of these traps also introduces a pathway for leakage current [14]. The $Al_2O_3$ can be negatively charged by electron injection which causes the states of $Al_i$ or $V_O$ in the band gap to be occupied by electrons [15]. Hole trapping phenomenon is also observed in $Al_2O_3$ as a source of positive charging [16], [17].

It is found that extra traps are formed at the edge of $Al_2O_3$ dielectric due to the etching process. Charges captured by the traps after voltage stress results in memory phenomenon. The sensing device is based on $Al/SiO_2$/p-Si structure. The memory operation procedure is illustrated in Fig. 2.

After a negative voltage defined as program is stressed on gate, electrons are trapped in the dielectric edge (Fig. 2(a)). Gate is opened and sensing voltage is applied on drain later. It should be noted that the sensing voltage must be large enough for drain MIS TD to enter its saturation region, so its current can be modulated by the minority carrier supply. Because of the trapped electrons, the band bending beneath gate edge is smaller at floating and less electrons are induced. This results in the reduction of $F_e$. As a consequence, the $q\phi_h^*$ in equation (1) becomes larger and a minor current is sensed at drain (Fig. 2(b)). On the other hand, a positive voltage defined as erase is stressed on gate to remove the electrons which were previously trapped (Fig. 2(c)). At the MIS TD read period, $F_e$ is larger compared to the programmed state and $q\phi_h^*$ is relatively small. Therefore, a larger current is sensed in this case (Fig. 2(d)). The experimental results are shown in Fig. 2(e). Distinct current levels can be read at the drain MIS TD if different quantities of charges are stored in gate dielectric edge.

It is found that the edge-etched $Al_2O_3$ is capable of enlarging the current window and enhance the retention characteristic in this work. Furthermore, the thickness of $Al_2O_3$ dielectric is a factor affecting the memory performance and is discussed.

## II. EXPERIMENTAL

The process flow is shown in Fig. 3 and described in the following. A boron-doped 1–10 Ω·cm (100) silicon wafer was used as the substrate. After standard Radio Corporation of America clean, an ultrathin $SiO_2$ layer (<40 Å) was grown on the wafer by anodic oxidation (ANO) in deionized water at room temperature. Then, rapid thermal process in $N_2$ ambient at 950 °C for 15 s was implemented for postoxidation annealing. 200 Å of Aluminum film was subsequently deposited by thermal evaporation. The Al films were then oxidized in 68wt% $HNO_3$ aqueous solutions at room temperature for 15 minutes to acquire $Al_2O_3$ dielectric. The deposition and oxidation (DO) process was repeated for two or three times for $Al_2O_3$ layer of different thickness. Each layer of $Al_2O_3$ is about 150 Å. Two groups of sample were fabricated then.

Group A were MISs with differently fabricated $Al_2O_3$ dielectric and were used to study the effects of edge-etched $Al_2O_3$ (Fig. 4). Group B were charge-coupled MIS TDs with various thickness of etched $Al_2O_3$ layer at gate. For group A, an Al film with a thickness of 200 nm was deposited as electrode by thermal evaporation and was patterned by lift off or wet etching. Wet etching was carried out by liquid mixture of nitric and phosphoric acid while the former oxidized the Al and the later etched the $Al_2O_3$. The device fabricated by lift off retained $Al_2O_3$ outside the Al electrode and was named planar MIS. Correspondingly, device fabricated by wet etching retained $Al_2O_3$ only under the electrode since the etchant also removed the $Al_2O_3$. For group B, $Al_2O_3$ first defined by lithography and wet etching remained only at gate area. Al film of 200 nm was deposited and defined by lithography and wet etching as gate and drain electrode later (Fig. 1). Finally, after removing the back native oxide with buffered oxide etchant, Al film of 200 nm was evaporated at the back of the substrate as back electrode for both groups. MOS and charge-coupled MOS without the $Al_2O_3$ layer was also fabricated as control group. The electrical characteristics are measured by Agilent B1500A.

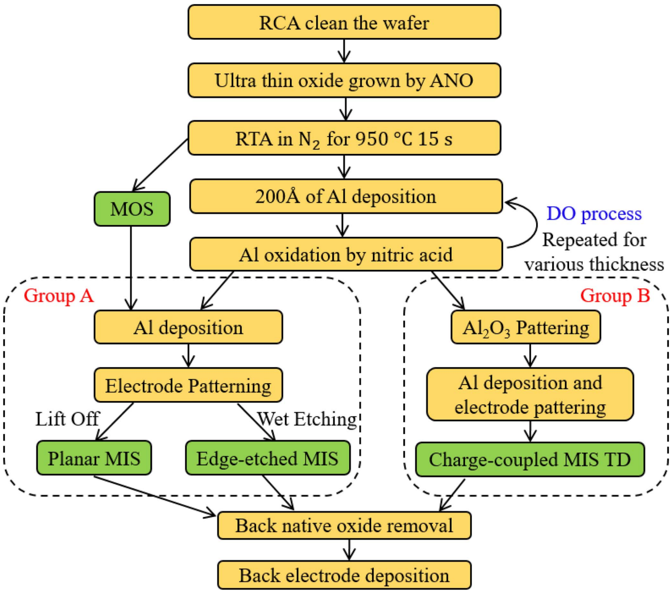

**FIGURE 3. The experimental process flow chart.**

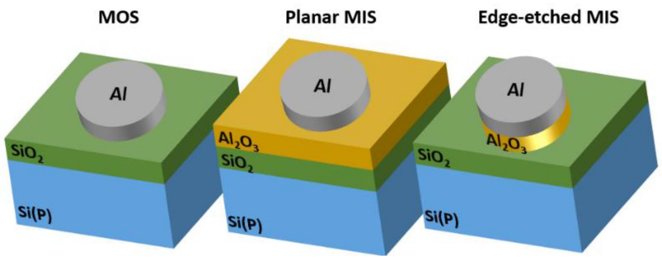

**FIGURE 4. Schematic of three distinct structures in group A. MOS acts as the control group. Planar MIS was carried out by lift off while the edge-etched MIS was accomplished by wet etching. The radius of the electrode is 85 um.**

## III. RESULTS AND DISCUSSION

Fig. 5 shows the current-voltage and capacitance-voltage characteristics of three distinct devices depicted in Fig. 4. It is observed in Fig. 5(a) that the MOS owns the largest current under negative (forward) bias because of its thinnest dielectric. Direct tunneling dominates at this region and the current decreases as the dielectric becomes thicker. Planar MIS possesses the least current due to the additional $Al_2O_3$ because the thick dielectric reduces the direct tunneling probability. However, the edge-etched MIS (EE MIS) owns a medium current level which is bizarre if only direct tunneling mechanism is considered. It is suggested that traps are formed at the edge from the wet etching process. The traps intensify the trap assisted tunneling phenomenon and form a leakage path raising the current at the device edge. At positive (reverse) bias, effective SBH modulation mechanism must be considered. When the voltage is biased from 0 V to 1 V (bias is small), SBH modulation effect is not sufficient and the tunneling probability still affects. Negative correlation appears between the magnitude of tunneling current and oxide thickness. The MOS device saturates first because the thin dielectric cannot stop the inversion charges from tunneling. As the bias rises and makes each device enter the saturation region, SBH modulation mechanism becomes dominant. Current of planar MIS still increases and becomes

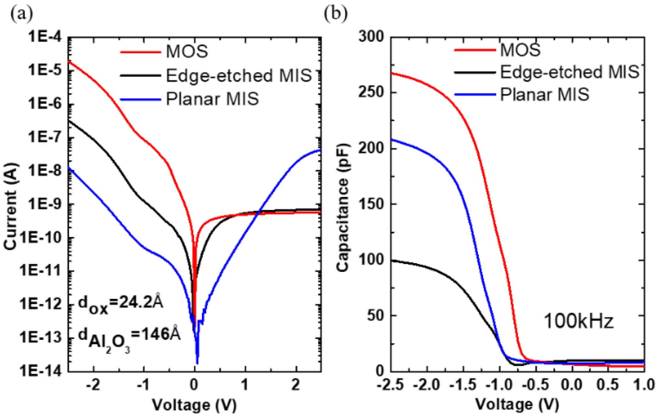

**FIGURE 5.** (a) The current-voltage characteristics and (b) the capacitance-voltage characteristics at 100 kHz of MOS and MIS with various dielectric structures.

the largest one among the three. This is because the inversion charges can accumulate at the $SiO_2$/Si interface and result in a lowest $\phi_h^*$. Although the EE MIS owns a thick dielectric as well, the inversion charges can still tunnel through the edge traps so the saturation current does not increase prominently.

The flat-band voltage is about $-0.85$ V for Al/$SiO_2$/Si(p) system and corresponds to Fig. 5(b). The planar MIS shows a negative flat-band shift due to extra positive fixed charges from $Al_2O_3$ oxidation. The capacitance of planar MIS at accumulation ($-2.5$ V) slightly drops compared to the MOS because of the larger EOT. However, capacitance of EE MIS drops abnormally at accumulation region which means that factor besides EOT must be considered.

To study the etched edge in detail, the C-V curves of planar and EE MIS are measured at 1kHz, 10kHz and 100kHz (Fig. 6). In addition to the drop of capacitance value, an evident frequency dispersion of capacitance is also observed. A circuit model of EE MIS is proposed to explain the effects of edge traps. $C_{HK}$ and $C_{OX}$ are capacitances of dielectric layers. $G_{HK}$ and $G_{OX}$ are the leakage paths which are intrinsic in dielectrics. $G_S$ is the series conductance originated from substrate and contact. $G_{edge}$ (effective) is used to indicate the extra leakage path from edge traps. The admittance of the modeling circuit is

$$Y = \frac{1}{\frac{1}{j\omega C_{ox}+G_{ox}} + \frac{1}{j\omega C_{HK}+G_{HK}+[G_{edge}(effective)]} + \frac{1}{G_s}} \quad (5)$$

and the measured capacitance is

$$C_M = Im(Y)/\omega \quad (6)$$

which equals to the imaginary part of admittance divided by angular frequency. Parameters for simulation are given in Table 1. $C_{OX}$ is extracted from MOS in Fig. 5(b) at $-2.5$V since the oxide thickness is the same in three structures. $C_{HK}$ is calculated from $Al_2O_3$ film of 150 Å with a dielectric constant of 9. $G_S$, $G_{OX}$ and $G_{HK}$ are first chosen to fit the measured capacitance of planar MIS. Capacitance

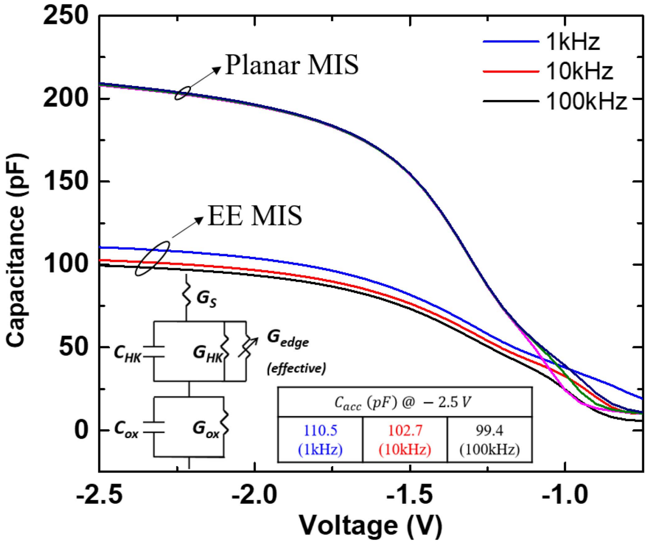

**FIGURE 6.** Measured C-V curves of planar and EE MIS at three frequencies. The inset shows the proposed circuit model. The table lists the capacitances of EE MIS under accumulation at $-2.5$ V for three frequencies.

**TABLE 1.** Parameters for simulation and the results.

| $C_{OX}$(pF) | $C_{HK}$(pF) | $G_S$(S) | $G_{OX}$(S) | $G_{HK}$(S) |
|---|---|---|---|---|
| 258.6 | 1434 | 0.044 | 0.31 | 0.06 |
| Frequency | | 1kHz | 10kHz | 100kHz |
| $G_{edge}$(S) | | 0.0374 | 0.043 | 0.045 |
| Planar MIS $C_M$(pF) @ -2.5 V | | 209.9 | 209.9 | 209.9 |
| EE MIS $C_M$(pF) @ -2.5 V | | 110.56 | 102.1 | 99.3 |

values of planar MIS at three frequencies are almost the same in both experiment and simulation. Frequency dispersion of capacitance is evident in EE MIS due to the nonzero $G_{edge}$. The etched edge constructs parallel capacitances and conductances for charge storage and leakage paths which result in frequency-dependent $G_{edge}$. At high frequency, capacitances can be regarded as short circuit and correspond to assumed larger $G_{edge}$. The simulation results accord to facts of dropped capacitance and frequency dispersion behavior.

To evaluate the charge trapping characteristic of edge-etched MIS, C-V curves of three $Al_2O_3$ thicknesses are measured at different states and are shown in Fig. 7. The $Al_2O_3$ thickness varies due to single, double or triple cycle of Al DO process. Samples with different $Al_2O_3$ thickness exhibits inconsistent directions of $V_{FB}$ shift after negative stress. The detailed charge injection mechanism is illustrated in Fig. 8. The location of the trap must distribute along the edge in realistic and are effectively depicted at the $Al_2O_3$/$SiO_2$ interface in the figure. The triple-layer device performs a negative $V_{FB}$ shift after negative stress indicating the trapped charges are mainly holes injected from substrate. The injection of electrons from metal is little because of thick $Al_2O_3$ layer. A positive stress can later remove the trapped holes. The quantities of injection electrons rise in a thinner

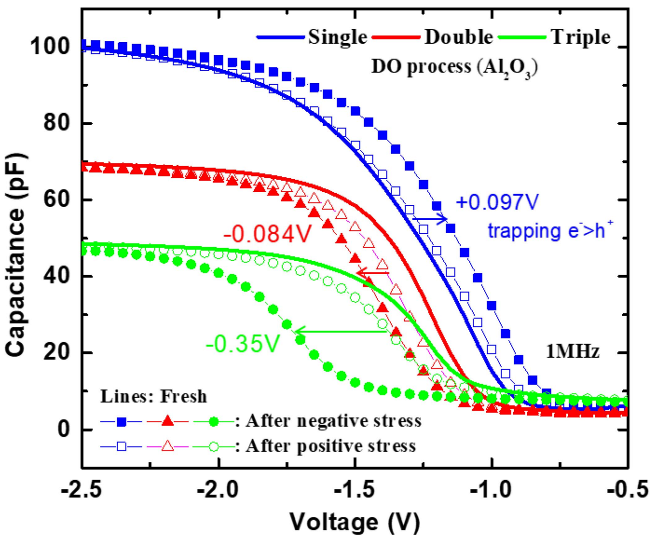

**FIGURE 7.** C-V curves of EE MIS with $Al_2O_3$ prepared by single, double and triple DO process. The fresh capacitance and the values after negative and positive stress measured at 1MHz are shown. The numbers labeled indicate the flat-band voltage shift after negative stress related to positive stress. The negative stress is −3.5 V, 100 s while positive stress is +2V, 100 s.

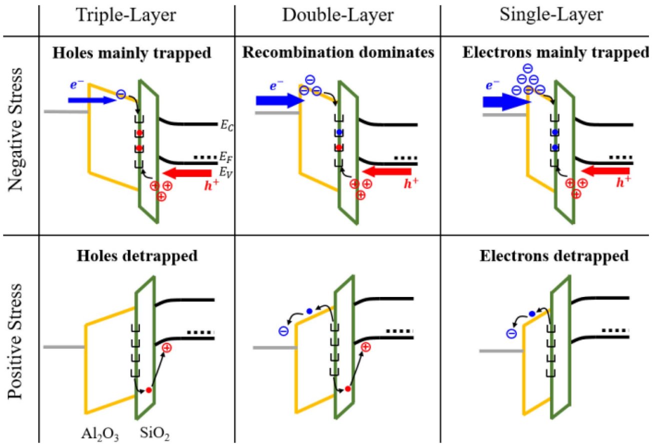

**FIGURE 8.** The schematic diagrams of the injection mechanisms in EE-MIS with different $Al_2O_3$ dielectric thickness. The quantities of electron injection from electrode increase as the thickness of $Al_2O_3$ dielectric is decreased.

$Al_2O_3$ so the recombination of electrons from metal and holes from substrate results in minor $V_{FB}$ shift in double-layer device. On the contrary, positive $V_{FB}$ shift appears in single-layer sample after negative stress because the electron injection from electrode dominates. A positive stress can later detrap the stored electrons.

The edge-etched $Al_2O_3$ structure is then applied as the gate dielectric of a charge-coupled MIS TD. Before the measurement, a positive voltage stress (PVS) induced breakdown [9] was performed on the drain MIS (Fig. 9). After PVS, the current shows earlier saturation behavior which means that the tunnel diode can sense the variation of inversion charges at smaller reversed bias. It is an advantage to memory application by MIS TD because of the lowered power consumption.

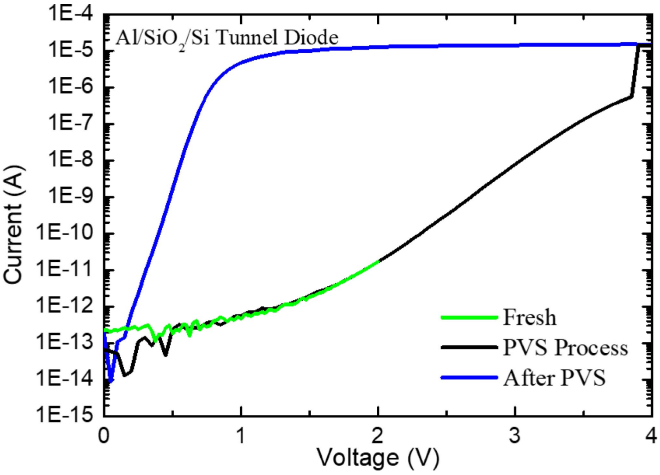

**FIGURE 9.** I-V curves at reversed bias of the drain MIS(p) TD before and after PVS. Current saturates earlier after the PVS process.

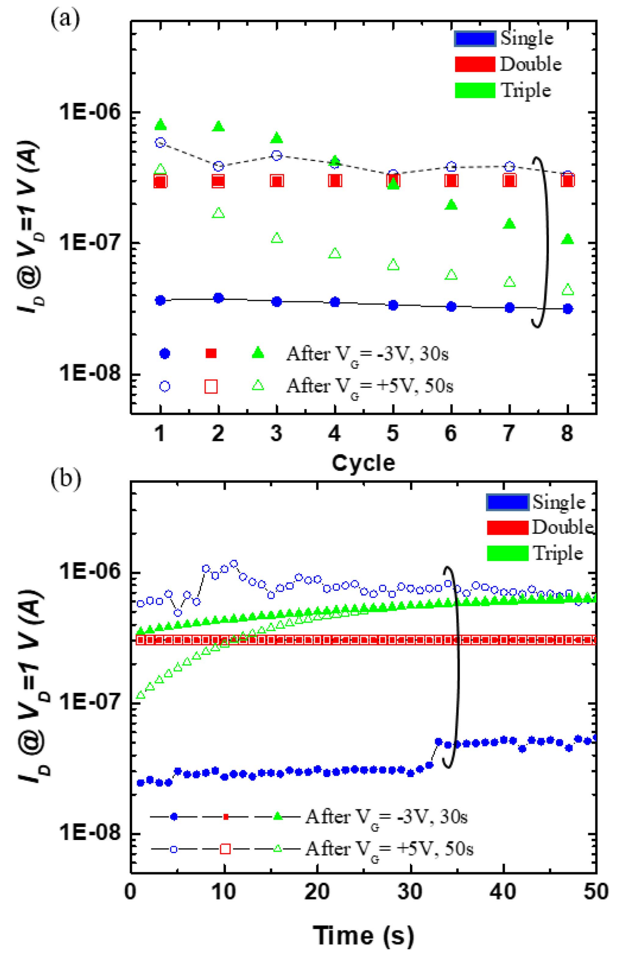

**FIGURE 10.** (a) Endurance and (b) retention characteristics of coupled MIS TDs with single, double and triple layer of edge-etched $Al_2O_3$ gate. The voltage stress of set and reset are −3 V, 30s and +5 V, 50s. The $SiO_2$ thickness is 31.2 Å and the read voltage is 1 V.

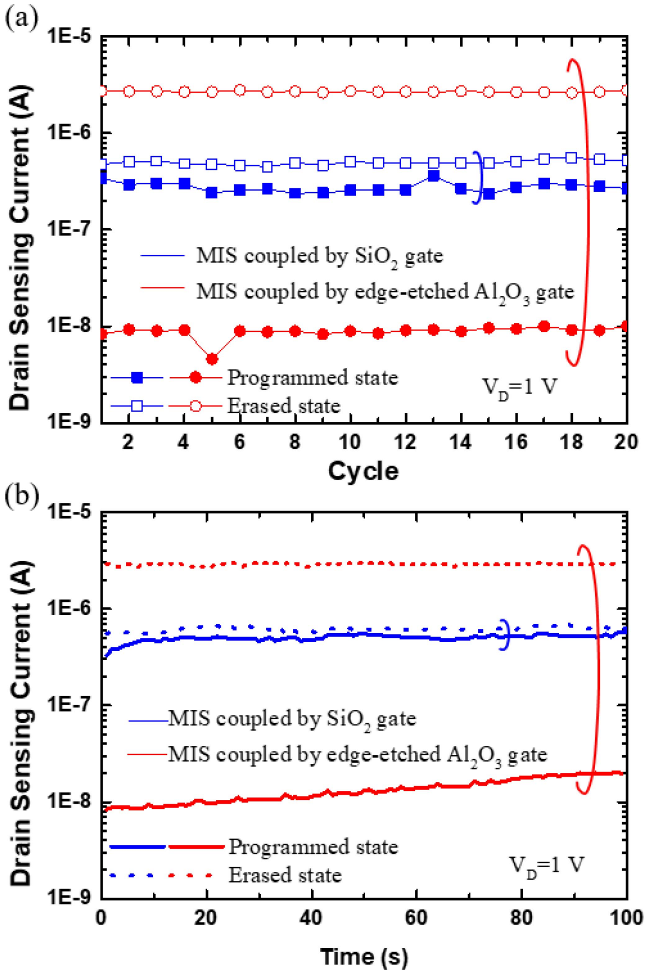

**FIGURE 11.** **(a) Endurance and (b) retention characteristics of coupled MIS TDs with $SiO_2$ and single-layer edge-etched $Al_2O_3$ gate. The program voltage stress is −3 V, 30s while the erase voltage stress is +3V, 30s.**

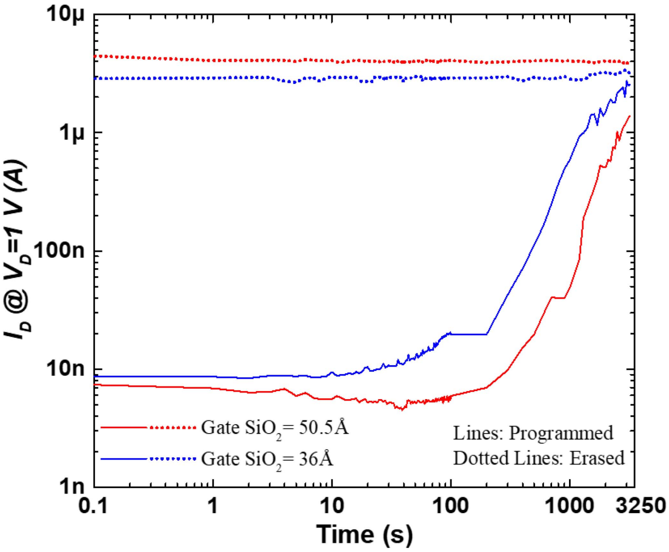

**FIGURE 12.** **The retention characteristics of coupled MIS TDs with different $SiO_2$ thickness at gate region. The $SiO_2$ thickness is 36 Å at both drains.**

Fig. 10 shows the endurance and retention characteristics of MIS coupled with different $Al_2O_3$ thickness. The single-layer device senses minor current while the triple-layer device read a larger current after negative stress. It is the consequence of distinct types of stored charges. Electrons from metal and holes from substrate dominates the memory behavior in single-layer and triple-layer devices respectively which is consistent with Fig. 7. If holes are trapped, more minority carriers are induced under gate area and the supply of lateral electron flux to drain edge is increased. Larger current is sensed due to reduction in $q\phi_h^*$. Current window is barely observed in double-layer device because the magnitude of hole and electron injection in dielectric are comparable and recombination makes little effective charges trapped. Triple-layer device owns an unstable current window because the positive voltage applied is so large that electrons from the substrate are trapped in the dielectric while removing the holes previously stored. Some electrons remain trapped in the next cycle and cause the entire current window to drift. Single-layer device also performs better retention characteristic. Trapped charges are mainly from substrate and probably trapped in $SiO_2$ than $Al_2O_3$ in triple-layer device. The electric field is stronger in $SiO_2$ than $Al_2O_3$ because of the smaller dielectric constant. Hence, the stronger electric field in $SiO_2$ results in rapid charge loss and a worse retention performance. Besides, the lateral field at read operation can disturb the stored charges. Even though the current window of triple-layer device may be stable by adjusting the stress parameters, the retention characteristic is still considered inferior. Based on the above factors, MIS coupled with single-layer edge-etched $Al_2O_3$ dielectric was chosen to implement the following experiment.

Fig. 11 shows the endurance and retention characteristics of MIS TDs coupled by a gate with and without edge-etched $Al_2O_3$. The $SiO_2$ thickness is 36 Å in both cases. It is observed that the current window of edge-etched device is enlarged for 165 times. As a negative stress is added as program process, traps at the edge which can be regarded as storage node capture the electrons and store them. The stored electrons lead to an electric field repelling inversion charges at the consequent read process.

A larger $q\phi_h^*$ is induced and lower current is sensed at drain after programmed. On the other hand, only intrinsic traps exist in the silicon dioxide of planar device and are relatively less than a device coupled with edge-etched $Al_2O_3$. Therefore, Schottky barrier height modulation mechanism is less obvious and minor current window is measured. Since the Al/dielectric/Si system possesses a negative $V_{FB}$, stored charges gradually detrap due to the positive electric field as the gate is zero biased. However, the electric field in $Al_2O_3$ dielectric is weaker because of larger dielectric constant compared to $SiO_2$. Electrons stored in the edge-etched sample is less disturbed after program. This can be recognized from the improved retention performance shown in Fig. 11(b). Current window of MIS coupled by edge-etched

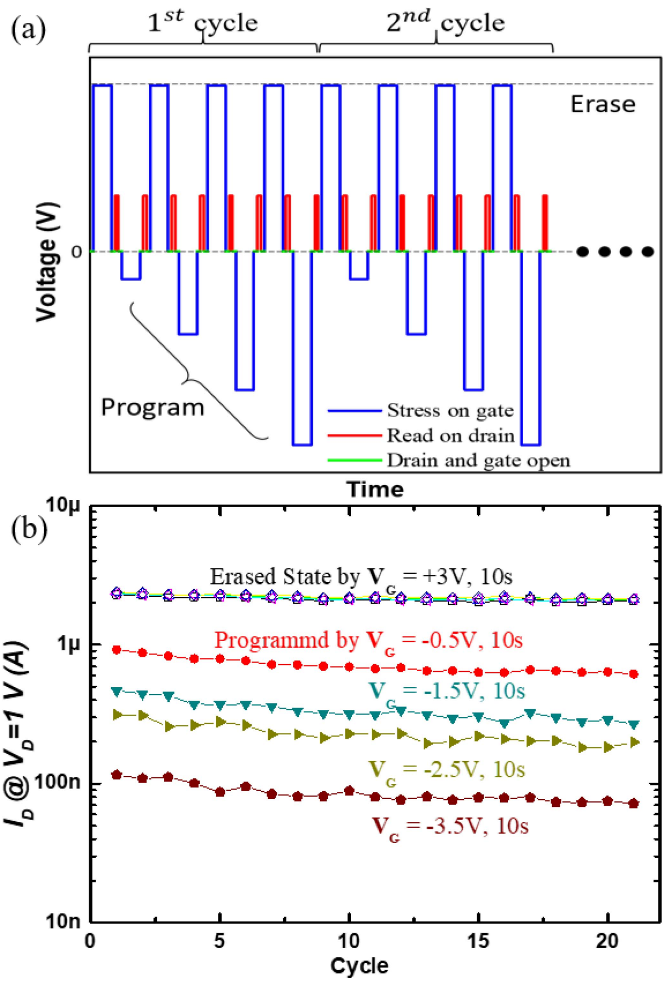

**FIGURE 13.** **(a) Operation principle to perform multilevel characteristic. (b) The measured multilevel characteristic. The $SiO_2$ thickness is 33.6 Å and drain senses the current at 1 V.**

gate remains obvious at 100 seconds after programmed while that of the control group barely exists.

A longer retention characteristic of MIS TD coupled with $Al_2O_3$ is shown in Fig. 12. Memory window gradually decays with time. The phenomenon is reasonable since the charge storage region is not electrically isolated. A thicker $SiO_2$ of 50.5 Å at gate exhibits retention improvement by reducing the electric field at floating. It is suggested that method such as replacing $Al_2O_3$ with a material with higher dielectric constant can also improve the retention in future work.

Due to the enlarged current window, the quantities of stored charges can be manipulated by various stress parameters and exhibit multilevel characteristic. The multilevel demonstration is a way to increase memory density and is not feasible in a charge-coupled MIS TD with only $SiO_2$ because the fewer traps tempt to be fully occupied if a negative stress is added. Fig. 13(a) illustrates the method to obtain multilevel characteristic. The blue line indicates that a voltage is stressed on gate. A constant positive voltage is first served as erase process to remove all the electrons previously trapped. Then, different negative stresses are given to inject distinct numbers of electrons in the dielectric edge. The program process differs in the magnitude of stress. Drain reads the current instantly after the state is modulated which is expressed by red line. The green line indicates a short period as Agilent B1500A switches its measurement channel between gate and drain. Five distinct states are observed in Fig. 13(b). The erased state shown is actually composed by four perfectly overlapping curves. It illustrates that the device can return to the same initial state even being differently programmed.

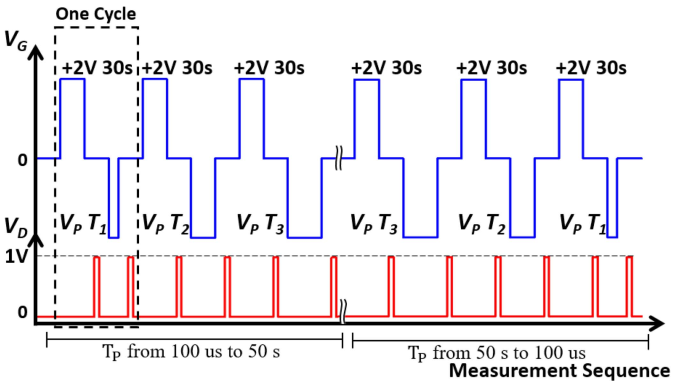

**FIGURE 14.** **Procedure to obtain tunable conductance in coupled MIS. The erase voltage is always +2 V, 30s. The program process differs in the magnitude and duration of stress.**

Although five-state characteristic is achieved above, the operation specification in Fig. 13(b) is not the only choice. By tuning the magnitude and duration of programming process, analog behavior is achieved. Fig. 14 illustrates the concept to test the analog behavior of coupled MIS TD. +2V, 30s is served as erase voltage in each cycle to retrieve initial state before the conductance is tuned. The erase voltage must be well chosen to ensure a stable current window. Otherwise, the whole current level will gradually decline because electrons are not totally removed before the next program cycle. Program voltage is denoted as $V_P$. Program duration is denoted as $T_P$ and varies from 100 $\mu$s to 50 s in this experiment. The analog characteristic is carried out from 100 $\mu$s to 50 s forward and then backward to examine the repeatability of the operation.

Fig. 15(a) shows the sensing current as the procedure illustrated in Fig. 14 was carried out. $V_P$ was tested with $-1$ V, $-2$ V and $-3$ V. Current larger than 1$\mu$S is defined as erased state. The relation between the sensing current and the duration of voltage stress is shown in Fig. 15(b). A negative stress with a larger magnitude can modify the current to a lower state in a relatively short duration. However, the current cannot be suppressed ultimately. Current remains 20 pA once the duration exceeds 40 s with $V_P$ equals to $-3$ V. This is because the number of traps at gate edge is limited. Current is fixed at a value when the traps are totally occupied. Each state labeled in Fig. 15(b) is defined

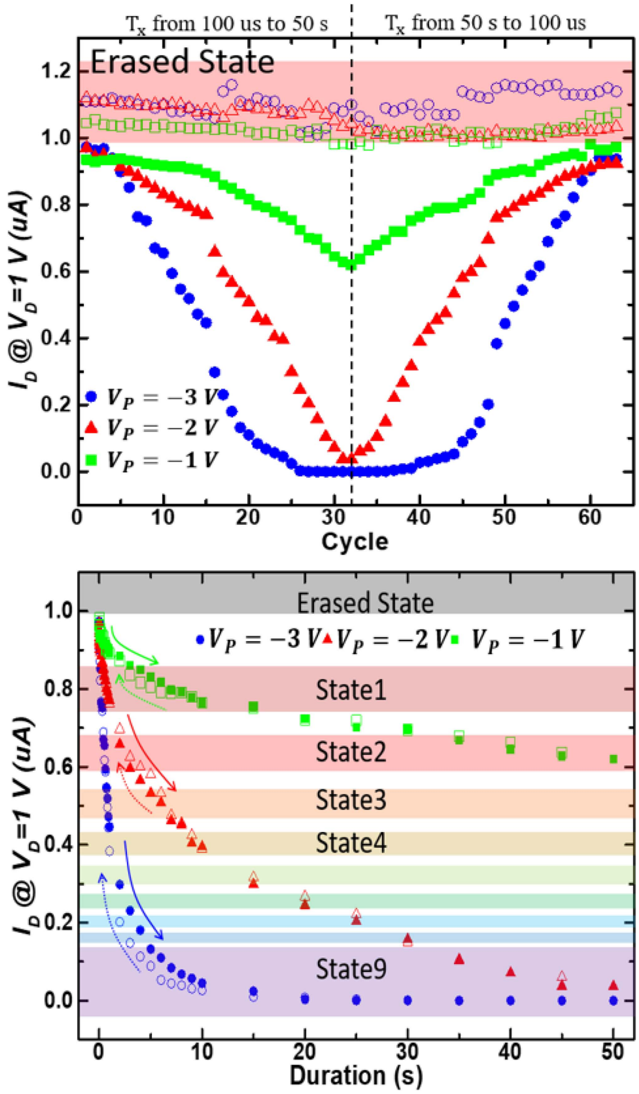

**FIGURE 15. (a) Conductance tuning characteristic by procedure shown in Fig. 14. The hollow symbols represent the erased states while the solid represent the programmed states. (b) Relation between the tunable conductance and the duration of voltage stress. The solid lines indicate conductance measured when $T_P$ changes from 100 $\mu$s to 50 s forward and the dot lines indicate the measurement done backward. Conductance was measured at $V_D$ = 1 V.**

by multiplying the current value of former state by 0.8 with a ±10% range. Values below 0.15 $\mu$A is all defined as state 9 because the range of each state is too small to be labeled. The analog-like behavior proposed a possible application of coupled MIS TD as synaptic device in artificial neural network (ANN). As a voltage signal is received at gate, various current values be sensed and transmitted at drain. The on/off ratio is $10^5$ which is larger than most of the resistive synaptic device candidates [18].

In the future work, a scaled down device must be constructed to promote the operation speed and is preferable in practical application. The narrower distance between drain and gate can shorten the duration of program and erase by enhancing the gradient of minority concentration. The supply of electron flux to the edge of drain is therefore more sensitive to the stimulation on gate. It is also required to improve the retention if the device is aiming for nonvolatile application. Although further refinements are required for the present device, the demonstration of multilevel and analog characteristics is believed to be beneficial for development in memory cells with tunnel diodes.

## IV. CONCLUSION

In this paper, edge-etched $Al_2O_3$ dielectric is applied as gate dielectric in charge-coupled MIS TD memory. The effects are first investigated by various MIS structures. Traps formed at the device edge from the etching process result in different current and capacitance characteristics compared to a planar device. Extra conductance is proposed in circuit model to explain the drop and frequency dispersion of capacitance. Thickness of $Al_2O_3$ layer is also an important factor to charge storage characteristic. The coupled MIS TD with thinner $Al_2O_3$ dielectric possesses stable current window and better retention characteristic in our experiment. With an additional edge-etched $Al_2O_3$ layer, both the current window and retention are improved. Due to the enlarged current window, multilevel charge storage is demonstrated. Furthermore, the analog-like feature which is necessary for synaptic application is achieved by various programming parameters. The relation between programmed current and the stress parameters is studied.

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