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Superjunction LDMOS With Dual Gate for Low On-Resistance and High Transconductance

ZHEN CAO (Member, IEEE), AND LICHENG JIAO (Fellow, IEEE)

Key Laboratory of Intelligent Perception and Image Understanding of Ministry of Education, International Research Center for Intelligent Perception and Computation, Joint International Research Laboratory of Intelligent Perception and Computation, School of Artificial Intelligence, Xidian University, Xi'an 710071, China

CORRESPONDING AUTHOR: Z. CAO (e-mail: icaozhen@163.com)

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ABSTRACT In this paper, a novel bulk silicon lateral superjunction double diffused MOSFET (SJ-LDMOS) with dual gate (DG) is proposed and its mechanism is investigated by numerical TCAD simulations. The proposed structure features the combination of a trench gate and a planar gate, forming two current conduction paths. One current conduction takes place along the highly doped *N*-pillar. The other is through the *N*-buffer layer ensuring uniform current distributions, which solves the problem of low conduction in the *N*-buffer layer of the SJ-LDMOS structures. The dual conduction paths improve the current uniformity through the entire SJ layer and the *N*-buffer layer, which effectively reduces the resistance of the device. Simulation results indicate that the proposed device is predicted to achieve a high breakdown voltage (*BV*) of 643 V and an extremely low specific *ON*-resistance ($R_{ON,sp}$) of 28.53 mΩ·cm^2, which is by 46.7 % lower than that of the previously *N*-buffer SJ-LDMOS structures with the same drift length. Besides, the transconductance of DG SJ-LDMOS is increased by 54.5 % and the figure of merit (FOM) on $BV^2/R_{ON,sp}$ of DG SJ-LDMOS is increased by 85.5 %.

INDEX TERMS Superjunction MOSFET, *N*-buffer, trench gate, breakdown voltage, *ON*-resistance.

I. INTRODUCTION

Superjunction (SJ) technology is with the ability to achieve a remarkable low specific *ON*-resistance ($R_{ON,sp}$) at a given breakdown voltage (*BV*) while keeping almost all of the advantages of the power MOSFET, which has been realized in the 500–900 V power SJ MOSFET [1]–[4]. The bulk silicon lateral superjunction double diffused MOSFET (SJ-LDMOS) with good heat dissipation and the low-cost substrate has been developed in high voltage power integrated circuits. The early development of bulk silicon SJ-LDMOS devices were primarily to eliminate the substrate-assisted depletion (SAD) effect of the device [5]–[8]. Some authors use additional *N*-type impurities to compensate for the SAD [6], [8]. Then some reported structures based on the *N*-buffer SJ-LDMOS are all focusing on the optimization of the lateral and bulk electric field distributions of the device to further improve the *BV*, using the technology of resistive field plates [9]–[10], stepped doping buffer layers [11]–[12], *N*-type buried layers [13]–[14], deep drain diffusion [15], high-*K* dielectric trench [16], etc. However, the $R_{ON,sp}$ of the *N*-buffer SJ-LDMOS structures is still limited at high voltage ratings (~600V).This is because of the JFET effect of *N*/*P* pillars. When the pillar width of SJ-LDMOS decreases, the pillar width becomes comparable to the built-in depletion regions between *N*- and *P*-pillars, which narrows the current path in the pillars [17]. The electronic current mainly flows at the surface of the *N*-pillars. Moreover, the conductivity of the *N*-buffer layer is poor, especially, the *N*-buffer layer in the area under the *P*-pillar due to the built-in depletions between the *N*-buffer layer and the *P*-pillars. Thus, the conduction of the *N*-buffer layer is not fully utilized, which limits the *ON*-resistance of the device. In order to further reduce the resistance of the LDMOS, several types of trench LDMOS have been reported to improve the performance of the conventional LDMOS [18]–[24], however, these structures are mainly adopted for the low voltage applications.

To address the requirement for high voltage lateral MOSFETs with low $R_{ON,sp}$. In this paper, a novel SJ-LDMOS with dual gate (DG) is proposed, which combines the advantages of the trench gate and the planar gate. The

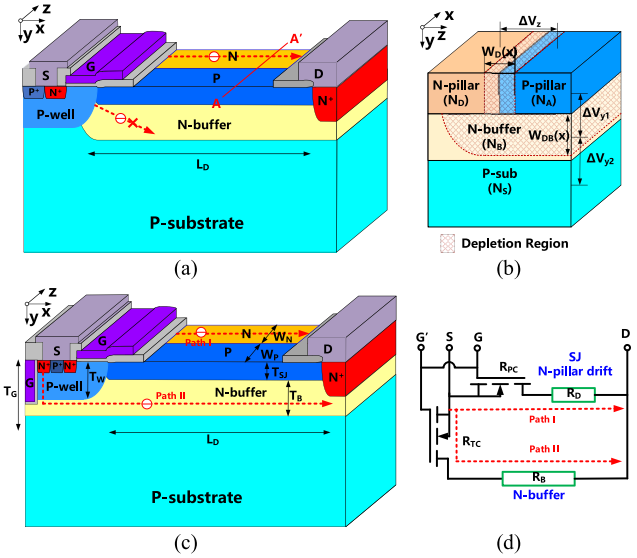

FIGURE 1. **Three-dimensional schematic structures. (a) Conventional *N*-buffer SJ-LDMOS. (b) Sectional view along AA'. (c) Proposed DG SJ-LDMOS. (d) Simplified equivalent circuit of the dual current conduction paths.**

dual current conduction paths are achieved, taking place along both the *N*-pillar and the *N*-buffer layer. The *N*-buffer layer not only effectively eliminates the substrate-assisted depletion effect, but also fully participates in current conduction. The dual conduction paths improve current uniformity through the entire SJ layer and the *N*-buffer layer, which effectively reduces the resistance of the device. Simulation results indicate that the $R_{ON,sp}$ of DG SJ-LDMOS is considerably reduced, which is 46.7 % lower than that of the previously *N*-buffer SJ-LDMOS structures. The transconductance of DG SJ-LDMOS is increased by 54.5 % and the figure of merit (FOM) on $BV^2/R_{ON,sp}$ of DG SJ-LDMOS reaches 14.49 MW/cm^2, increased by 85.5 %. The structure and theory for the proposal will be described in the following.

II. DEVICE STRUCTURE AND WORKING PRINCIPLE

The three-dimensional schematic structures of the proposed DG SJ-LDMOS and the conventional *N*-buffer SJ-LDMOS are shown in Fig. 1 (c) and (a). The main feature of DG SJ-LDMOS is the combination of a planar gate and a trench gate structure. This novel design inherits the advantages of both concepts while requiring only a minimum of additional process. The process flow is the same as the conventional *N*-buffer SJ-LDMOS apart from the implantation of a trench gate structure incorporated into the source side of the SJ-LDMOS complementing the standard p-well body contact. The width and depth of the gate trench are W_G and T_G. The thickness of the gate oxide of the trench gate and the planar gate are both T_{OX}. The parameters of the proposed DG SJ-LDMOS, the conventional *N*-buffer SJ-LDMOS and the conventional RESURF LDMOS with dual gate structure (DG LDMOS) used in the three-dimensional device simulation are specified in TABLE 1.

TABLE 1. **Parameters of optimized device structures.**

Symbol	Description	DG SJ-LDMOS	N-buffer SJ-LDMOS	DG LDMOS
W_N, W_P	*N*, *P* drift width (μm)	1.0	1.0	--
T_W	*P* well depth (μm)	3.0	3.0	3.0
T_{SJ}	SJ layer thickness (μm)	2.0	2.0	--
T_B	Buffer layer thickness (μm)	2.0	2.0	2.0~4.0
L_{GP}, L_{DP}	Gate, Drain FP length (μm)	3.0, 2.0	3.0, 2.0	3.0, 2.0
T_{OX}	Gate oxide thickness (μm)	0.05	0.05	0.05
T_{FOX}	Field oxide thickness (μm)	0.8	0.8	0.8
L_{PC}	Plane channel length (μm)	2.0	2.0	2.0
L_{TC}	Trench channel length (μm)	2.5	--	2.5
T_G	Plane, trench gate depth(μm)	1.0~5.0	--	1.0~5.0
W_{GT}	Gate trench width (μm)	2.0	--	2.0
L_D	Drift length (μm)	20~80	20~80	20~80
N_S	Substrate doping (cm^{-3})	1~2×10^{14}	1~2×10^{14}	1~2×10^{14}
N_D, N_A	*N*, *P* drift doping (cm^{-3})	5×10^{16}	5×10^{16}	--
N_B	Buffer layer doping (cm^{-3})	2~4×10^{15}	2~4×10^{15}	3~12×10^{15}

For the conventional SJ-LDMOS structures, the specific resistance of the SJ drift region $R_{D-SJ,sp}$ is the dominant component at high voltage ratings above 200 V, which is given by

$$R_{D\text{-}SJ,sp} = \frac{\rho_D L_D}{S_{NA}} L_D (W_N + W_P) = \frac{L_D^2}{q\mu N_D T_{SJ}} \left(\frac{W_N + W_P}{W_N - W_D(x)/2} \right) \quad (1)$$

where $S_{NA} = T_{SJ}\ (W_N - W_D(x)/2)$ is the equivalent cross-sectional area of the electron current flowing in the *N*-pillar. Fig. 1 (b) shows the sectional view along *AA*' of the conventional *N*-buffer SJ-LDMOS. $W_D(x)$ is the depletion region width between the *N*- and *P*-pillar ($N_A = N_D$), which is supported by the voltage difference ΔV_Z that is equal to the sum of the built-in potential V_{bi} and the on-state voltage $V_{on}(x)$ drop of the SJ drift region [25]. $W_D(x)$ and $V_{on}(x)$ gradually increase from the channel to the drain. In these case

$$W_D(x) = \sqrt{\frac{2\varepsilon_{Si}(V_{bi} + V_{on}(x))}{q} \left[\frac{N_A + N_D}{N_D N_A} \right]} \quad (2)$$

Therefore, the $R_{D\text{-}SJ,sp}$ is limited by the existence of the $W_D(x)$ due to the JFET effect, especially when the W_N becomes comparable to the $W_D(x)$. Similarly, the current conduction path in the *N*-buffer layer is poor, which is depleted both by the *P*-pillar with the voltage difference of ΔV_{y1} and by the *P*-substrate with the voltage difference of ΔV_{y2}, with the depletion region width of $W_{DB}(x)$.

With the additional trench gate of DG SJ-LDMOS, these problems mentioned above can be effectively improved. Firstly, due to the trench gate, electron current is fully conducted in the *N*-pillar, which will reduce the $V_{on}(x)$ and the $W_D(x)$. Secondly, the dual current conduction paths are achieved, taking place along both the *N*-pillar (path I) and the *N*-buffer layer (path II) as shown in Fig. 1 (d), which effectively reduces the resistance of the device. The total resistance of the drift region ($R_{D\text{-}total}$) and the channel

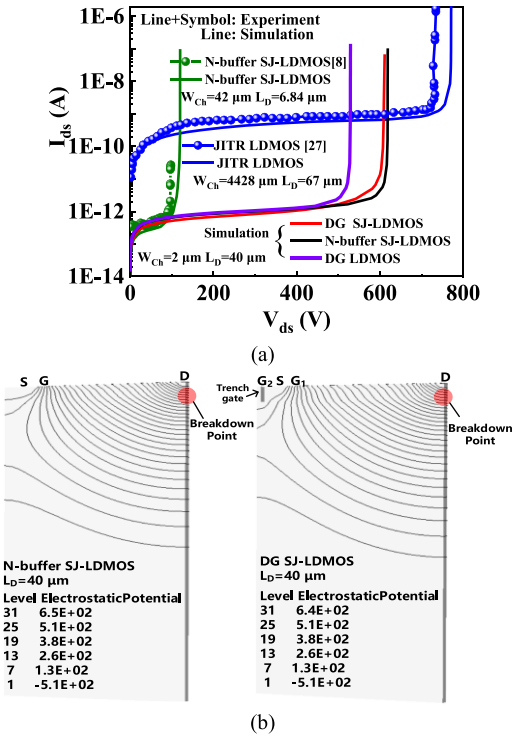

FIGURE 2. **(a) Experimental and simulation breakdown characteristics for the conventional *N*-buffer SJ-LDMOS, DG SJ-LDMOS, DG LDMOS and JITR LDMOS. (b) The equipotential distribution at the onset of breakdown for DG SJ-LDMOS and the conventional *N*-buffer SJ-LDMOS.**

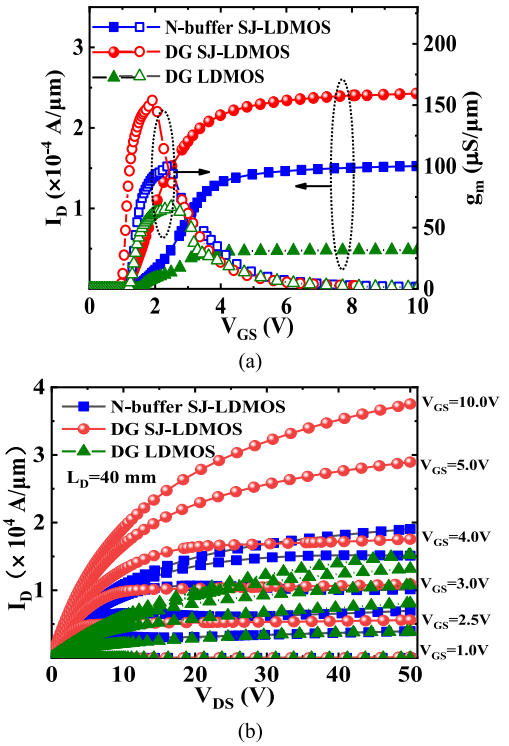

FIGURE 3. **Comparisons of (a) Transfer and transconductance characteristics (b) Output characteristics (V_{GS} @ 1.0, 2.5, 3.0, 4.0, 5.0, 10.0 V) for DG SJ-LDMOS, the conventional *N*-buffer SJ-LDMOS and DG LDMOS.**

($R_{\text{Ch-total}}$) of DG SJ-LDMOS is effectively reduced, which is given by

$$R_{\text{D-total}} + R_{\text{Ch-total}} = (R_{\text{D}} + R_{\text{PC}}) \| (R_{\text{B}} + R_{\text{TC}}) \qquad (3)$$

where R_{D} and R_{B} are the resistance of the *N*-pillar and *N*-buffer layer respectively, R_{PC} the resistance of the planar channel and R_{TC} the resistance of the trench channel.

III. RESULTS AND DISCUSSION

In this paper, to illustrate the credibility of the simulation, the TCAD simulation [26] is calibrated to experimental breakdown characteristics ($I_{\text{ds}} - V_{\text{ds}}$) data extracted from *N*-Buffer SJ-LDMOS [8] and Triple RESURF (Reduced SURface Field) LDMOS [27] with a certain channel width (W_{Ch}) shown in Fig. 2 (a). With one set of self-consistent parameters, the TCAD simulation results and the experimental data are all well matched. Fig. 2 (a) shows the off-state breakdown characteristics of the proposed DG SJ-LDMOS, the conventional *N*-buffer SJ-LDMOS and the DG LDMOS under the optimized conditions. Compared to the DG LDMOS (522 V), both the conventional *N*-buffer SJ-LDMOS (647 V) and DG SJ-LDMOS (643 V) have obtained the high *BV* due to the SJ drift. These devices are with the same low leakage current. Fig. 2 (b) shows the equipotential distribution at the onset of breakdown for DG SJ-LDMOS and the conventional *N*-buffer SJ-LDMOS. The breakdown points of these two devices are located where the equipotential lines dense under the drain, which is affected by the curvature effect of the N^+ drain diffusion. It can be seen that the trench gate is located near the low voltage source of DG SJ-LDMOS, and there is no equipotential line dense around it, so the trench gate has little effect on the breakdown voltage of the device.

The transfer and transconductance characteristics of DG SJ-LDMOS, the conventional *N*-buffer SJ-LDMOS, and DG LDMOS are shown in Fig. 3 (a). The threshold voltage of DG SJ-LDMOS, the conventional *N*-buffer SJ-LDMOS, and DG LDMOS is found to be 1.7 V, 2.0 V and 1.8V, respectively. For DG SJ-LDMOS, a higher peak transconductance (g_{m}) is obtained due to the simultaneous formation of the two current conduction paths. The g_{m} of DG SJ-LDMOS (153 μS/μm) is higher than that (99 μS/μm) of the conventional *N*-buffer SJ-LDMOS and that (67 μS/μm) of DG LDMOS with the improvement of 54.5 % and 128.4 %, respectively. The comparison of output characteristics for the three devices is shown in Fig 3 (b). DG SJ-LDMOS demonstrates better output performance than the conventional *N*-buffer SJ-LDMOS and DG LDMOS, under the conditions of different gate voltages (V_{GS} @ 1.0, 2.5, 3.0, 4.0, 5.0, 10.0 V). DG SJ-LDMOS has a higher slope in the linear region, indicating a lower $R_{\text{ON,sp}}$ (28.53 mΩcm^2) than that (53.57 mΩcm^2) of the conventional *N*-buffer SJ-LDMOS and that (124.84 mΩcm^2) of DG LDMOS with the decrease of 46.7 % and 77.2 %, respectively.

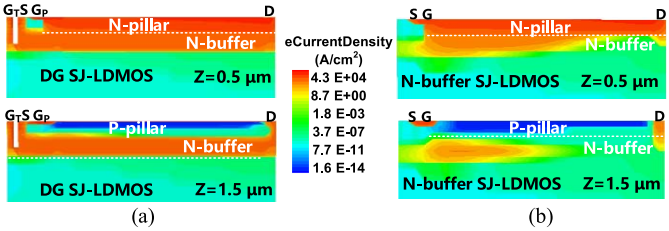

FIGURE 4. Electron current density of the conventional *N*-buffer SJ-LDMOS and DG SJ-LDMOS in the *ON*-state (V_{GS} = 10 V, V_{DS} = 10 V). (a) DG SJ-LDMOS and (b) Con. SJ-LDMOS @ Z = 0.5 μm (Middle position of the *N*-pillar) and @ Z = 1.5 μm (Middle position of the *P*-pillar).

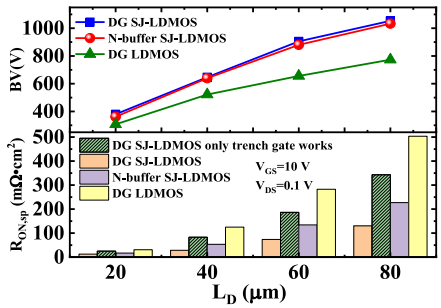

FIGURE 5. *BV* and $R_{ON,sp}$ versus L_D for DG SJ-LDMOS, the conventional *N*-buffer SJ-LDMOS and DG LDMOS.

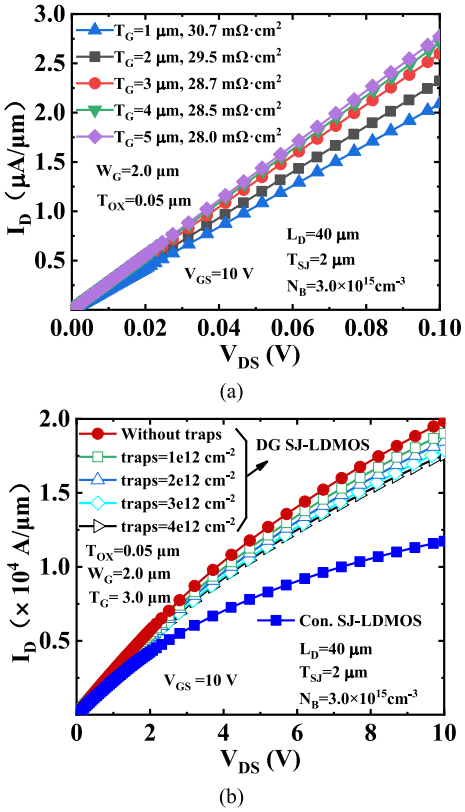

FIGURE 6. Simulated output characteristics at different (a) T_G and (b) different surface trap density at the Oxide/Silicon interface around the trench gate.

Fig. 4 (a) and (b) show the comparisons of the electron current density plots in the middle of the *P*-and *N*-pillar with the corresponding *N*-buffer layer below of the two devices. It can be seen that the electron current density of the *N*-buffer layer of DG SJ-LDMOS is higher than that of the conventional *N*-buffer SJ-LDMOS. For the conventional *N*-buffer SJ-LDMOS, the *N*-buffer layer in the area below the *P*-pillar is almost non-conductive. However, for DG SJ-LDMOS, the *N*-buffer layer is completely conductive due to the trench gate.

Fig. 5 shows the comparisons of the *BV* and $R_{ON,sp}$ for the three devices with the different L_D (20, 40, 60, 80 μm). It can be seen that DG SJ-LDMOS has obtained a lower on-resistance at different L_D. In addition, the $R_{ON,sp}$ generated by the path II of DG SJ-LDMOS (only the trench gate turns on) is still lower than that of DG LDMOS due to the highly doped *N*-pillar drift, which is an important part of the overall $R_{ON,sp}$ reduction for DG SJ-LDMOS. The figure of merit (FOM) on $BV^2/R_{ON,sp}$ of DG SJ-LDMOS is 14.49 MW/cm^2, higher than that (7.81 MW/cm^2) of the conventional *N*-buffer SJ-LDMOS and that (2.18 MW/cm^2) of DG LDMOS, with the improvement of 85.5 % and 564.7 % with the same L_D of 40 μm.

Fig. 6 (a) shows the influence of T_G on $R_{ON,sp}$ of DG SJ-LDMOS. The $R_{ON,sp}$ decreases as T_G increases and tends to saturate when T_G is 3.0 μm because the vertical channel length of the trench L_{TC} is 2.5 μm. Although further increasing T_G will form a vertical gate field plate at the bottom of the trench gate, leading to carrier accumulation and reduce resistance, it will also increase the gate capacitance of the device. Fig. 6 (b) shows the output characteristics at different surface trap density at the Oxide/Silicon interface around the trench gate. In reality, the mobility on the trench sidewalls could be different from the planar one due to the traps at the etched interface. It can be seen from the simulation results that as the density of traps increases, the conduction characteristics of DG SJ-LDMOS slightly decrease, but the overall conduction is still significantly higher than that of conventional *N*-buffer SJ-LDMOS. For the high voltage (>200) LDMOS devices, the on-resistance in the drift region plays a major role.

Fig. 7 (a) shows the influence of N_B on $R_{ON,sp}$ and *BV* of DG SJ-LDMOS. Since the *N*-buffer layer needs to fully compensate for the substrate-assisted depletion effect, there is an optimal N_B to obtain the maximum *BV* and correspondingly low $R_{ON,sp}$. Fig. 7 (b) shows the influence of N_A/N_D on $R_{ON,sp}$ and *BV* of DG SJ-LDMOS. With the increase of N_A/N_D, the $R_{ON,sp}$ of DG SJ-LDMOS gradually decreases and the maximum *BV* can be obtained under the condition of satisfying the charge balance. Fig. 7 (c) shows the influence of T_{SJ} on $R_{ON,sp}$ and *BV* of DG SJ-LDMOS. Since the conditions of RESURF and charge balance need to be satisfied between the SJ layer and the *N*-buffer layer, the optimal *BV* and $R_{ON,sp}$ are obtained under certain N_B conditions. Fig. 7 (d) shows the influence of T_B on $R_{ON,sp}$ and *BV* of

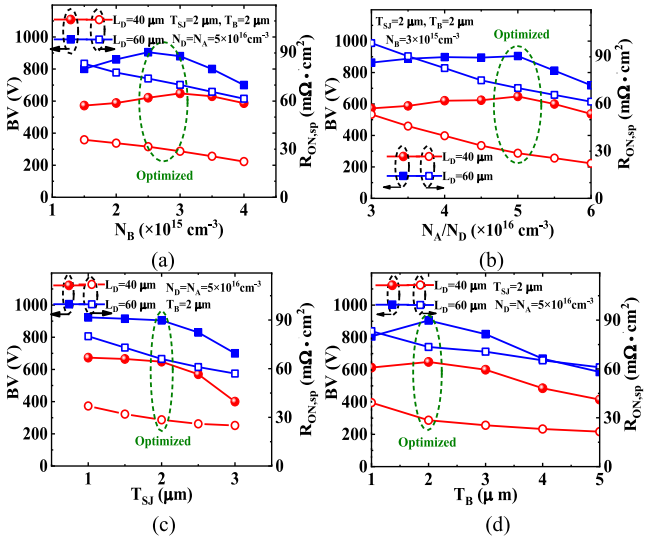

FIGURE 7. (a) $R_{ON,sp}$ and BV versus N_B at different L_D. (b) $R_{ON,sp}$ and BV versus N_A/N_D at different L_D. (c) $R_{ON,sp}$ and BV versus T_{SJ} at different L_D. (d) $R_{ON,sp}$ and BV versus T_B at different L_D for DG SJ-LDMOS.

DG SJ-LDMOS. A certain T_B can make DG SJ-LDMOS meet the conditions of RESURF and charge balance at the same time, so that the device can obtain a high BV. As T_B increases, although the $R_{ON,sp}$ of the device decreases, the voltage of the device also decreases.

Fig. 8 (a) compares the gate charge (Q_G) characteristics of DG SJ-LDMOS, DG LDMOS, and the N-buffer SJ-LDMOS. The components (gate–source charge (Q_{GS}) and gate–drain charge Q_{GD}) of the gate charge for DG SJ-LDMOS (Q_{GS} = 26.3 nC·cm^{-2}, Q_{GD} = 53.5 nC·cm^{-2}) and DG LDMOS (Q_{GS} = 26.1 nC·cm^{-2}, Q_{GD} = 51.2 nC·cm^{-2}) is larger than that (Q_{GS} = 18 nC·cm^{-2}, Q_{GD} = 43.7 nC·cm^{-2}) of the N-buffer SJ-LDMOS due to the additional capacitance of the trench gate. The gate plateau voltage for the proposed DG SJ-LDMOS is smaller due to its lower threshold voltage and larger transconductance. The switching characteristics of these three structures are given in Fig. 8 (b). The time spent on charging the additional capacitance of the trench gate increases the turn on and off time of DG SJ-LDMOS and DG LDMOS structures, which is larger than that of the conventional N-buffer SJ-LDMOS. The dynamic characteristic of the proposed DG SJ-LDMOS is more inclined to apply to the low and medium frequencies (10∼200 kHz) in the power field. Although the DG structure will increase a certain switching loss, it can significantly reduce the on-state power loss.

Temperature distributions in the N-buffer SJ-LDMOS and DG SJ-LDMOS are shown in Fig. 9. The thermodynamic transport model is required for simulations with high current levels, where considerable self-heating may occur. It can be seen from the results that although the high current causes the temperature of the two devices to increase, the two devices can still work normally.

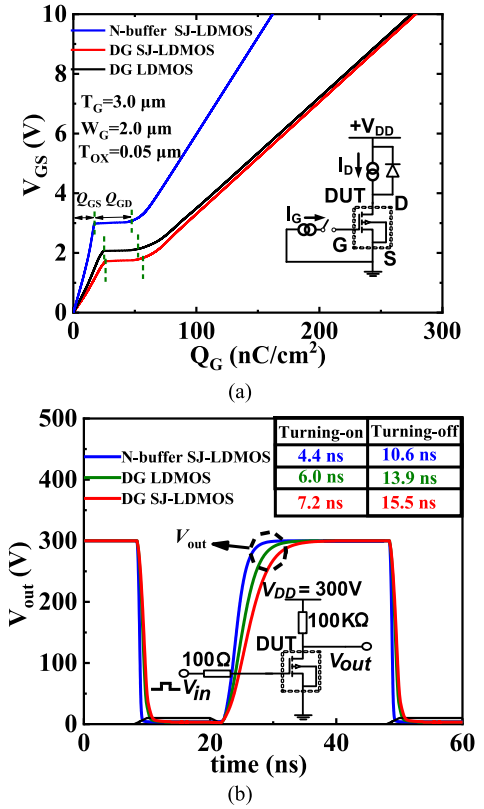

FIGURE 8. (a) Gate charge and (b) Switching waves of DG SJ-LDMOS, DG LDMOS, and the N-buffer SJ-LDMOS.

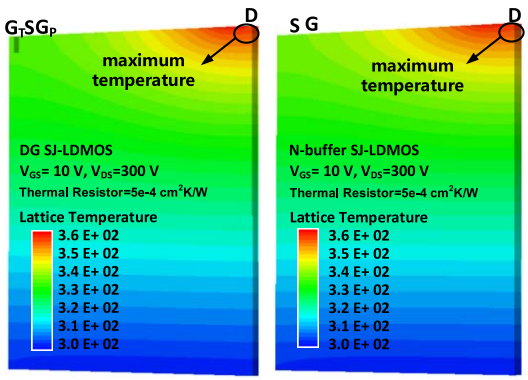

FIGURE 9. Temperature distributions in the N-buffer SJ-LDMOS and DG SJ-LDMOS.

Fig. 10 shows the $R_{on,sp}$ versus BV for DG SJ-LDMOS, DG LDMOS, the N-buffer SJ-LDMOS, and other existing SJ-LDMOS structures [4], [6], [14]–[16]. It is shown that DG SJ-LDMOS is with better performance in the BV region (400∼1200V) much closer to the lateral SJ Silicon limit [28].

Fig. 11 shows the key fabrication steps of the proposed DG SJ-LDMOS, which is basically the same as the process of the conventional N-buffer SJ-LDMOS, except that of a sidewall trench gate structure is formed. This device starts from a P-type (100) substrate and forms an N-type buffer layer with a certain concentration by the epitaxial process as shown

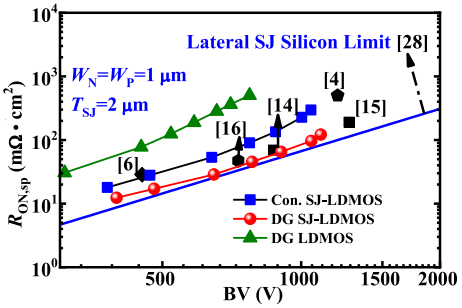

FIGURE 10. $R_{ON,sp}$ against *BV* of DG SJ-LDMOS, DG LDMOS, the *N*-buffer SJ-LDMOS and previously structures with the lateral SJ Silicon limit line.

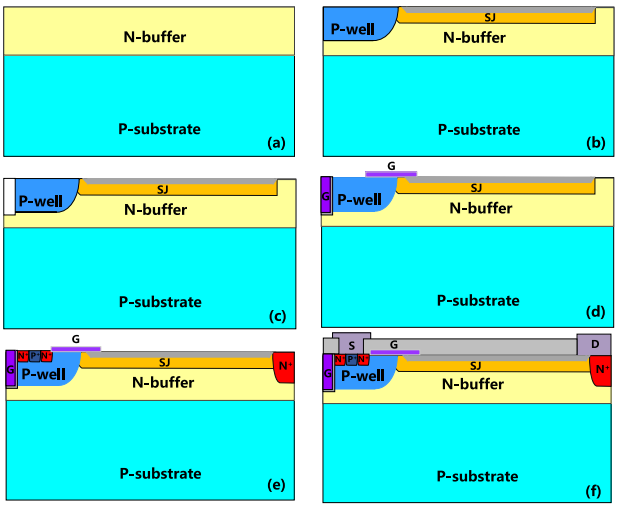

FIGURE 11. Simplified key fabrication steps of DG SJ-LDMOS. (a) The *P*-type substrate with *N*-type epitaxial layer. (b)After active region formation, the *P*-base and SJ layer are formed in the *N*-buffer layer. Then the field oxide is formed by STI. (c) A gate trench is formed. (d) Deposit and etch polysilicon after gate oxide layer thermally grown. (e) The source and drain are formed by N^+ and P^+ ions implantation. (f) Deposit and etch metal to form source and drain electrodes.

in Fig. 11 (a). After active region formation, the *P*-type base region is formed by *P*-type ion implantation, and the SJ layer is then formed by *N* and *P*-type ion implantation, respectively. Then the field oxide layer is formed by the shallow trench isolation (STI) as shown in Fig. 11 (b). The sidewall trench gate is formed by a trench etching process as shown in Fig. 11 (c). A thin gate oxide layer formation grows by thermal oxidation. Polysilicon is then deposited and etched to form the plane and trench gate electrode as shown in Fig. 11 (d). The N^+ and P^+ in the source and drain region are formed by high dosage ion implantation. as shown in Fig. 11 (e). Finally, deposit and etch metal to form source and drain electrodes as shown in Fig. 11 (f).

IV. CONCLUSION

In this paper, we propose a novel bulk Silicon SJ-LDMOS with the dual gate structure, which features the combination of a planar gate and a trench gate structure forming a dual current conduction path to reduce the overall *ON*-resistance. Device simulations show that the proposed DG SJ-LDMOS can deliver a remarkably lower $R_{ON,sp}$ than the conventional *N*-buffer SJ-LDMOS with the same drift length. The slightly longer switching time produced by the gate trench is tolerable. DG SJ-LDMOS provides noticeable benefits over the conventional *N*-buffer SJ-LDMOS structures with a limited amount of additional process steps.

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ZHEN CAO (Member, IEEE) received the B.S. degree from the Qingdao University of Science and Technology in 2013, and the M.S. and Ph.D. degrees from Xidian University, Xi'an, China, in 2016 and 2019, respectively, where he is currently a Postdoctoral Researcher with the School of Artificial Intelligence. Her current research interests include novel power devices, low-power devices, and neuromorphic smart devices.

LICHENG JIAO (Fellow, IEEE) received the B.S. degree from Shanghai Jiao Tong University, Shanghai, China, in 1982, and the M.S. and Ph.D. degrees from Xi'an Jiaotong University, Xi'an, China, in 1984 and 1990, respectively.

Since 1992, he has been a Professor with the School of Artificial Intelligence, Xidian University, Xi'an, where he is currently the Director of the Key Laboratory of Intelligent Perception and Image Understanding of the Ministry of Education of China. His research interests include image processing, natural computation, machine learning, and intelligent information processing. He is also the Chairman of the Awards and Recognition Committee, the Vice Board Chairperson of the Chinese Association of Artificial Intelligence, a Councilor of the Chinese Institute of Electronics, a Committee Member of the Chinese Committee of Neural Networks, and an Expert of the Academic Degrees Committee of the State Council. He is a member of the IEEE Xi'an Section Execution Committee.