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Different JFET Designs on Conduction and Short-Circuit Capability for 3.3 kV Planar-Gate Silicon Carbide MOSFETs

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ABSTRACT Both large current capability and strong short-circuit (SC) ruggedness are necessary for 3.3 kV SiC MOSFETs to improve system efficiency and reduce costs in industrial and traction applications. In this paper, the effects of Junction Field Effect Transistor (JFET) region width and JFET doping (JD) on conduction and SC capability of the 3.3 kV planar-gate SiC MOSFETs are systematically investigated by experiments and simulations. When the JFET width (W_{JFET}) of device without JD is smaller, the positive temperature coefficient of the special on-resistance ($R_{on,SP}$) is larger. The JD is effective to improve the $R_{on,SP}$, but excessive electric field in gate oxide induced by JD should be paid more attention. The optimization of W_{JFET} can be used to improve both $R_{on,SP}$ and short circuit withstanding time (SCWT) at the same time. The drain-source current (I_{ds}) and SCWT of the optimized devices are 50 A and more than 20 μs, respectively, which is state-of-the-art for 3.3 kV SiC MOSFETs.

INDEX TERMS SiC MOSFET, JFET width, JFET doping, short circuit.

I. INTRODUCTION

Compared with silicon power devices, silicon carbide (SiC) power devices possess lower power loss, higher operation temperature, higher switching frequency, and better heat dissipation owing to its superior material properties, such as wider bandgap, higher critical electric field strength, and higher thermal conductivity [1]–[3]. Hereby SiC power devices are expected to be next-generation alternatives to silicon power devices in power conversion systems.

With the rapid development of SiC material and device technology, SiC power devices with voltage rating under 1700 V have been commercially available and show excellent performances such as low on-resistance and low switching loss. Development of 3.3 kV SiC Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) in half-bridge power modules are of great interest for industrial and traction applications to improve system efficiency and reduce cost of power conversion systems compared to the state-of-the-art silicon IGBT based technology [4]. Up to now, 3.3 kV SiC MOSFETs are under developments by several research groups [4]–[10]. The reported maximum conduction current is 30 A [9] and the maximum short circuit withstanding time (SCWT) is 10 μs [10]. However, in most cases of industrial converters, the SCWT of switches is required around 10 μs in order to survive accidental event, especially in motor drive applications [10], [11]. Meanwhile, both high conduction current and expected device reliability are essential in traction inverter applications. For SiC MOSFETs with a voltage rating under 1700 V, the on-resistance is strongly dependent on the channel resistance, while the JFET resistance play a significant role when voltage rating is above 3.3 kV. Hence, the optimization of the JFET region is necessary in 3.3 kV SiC MOSFETs.

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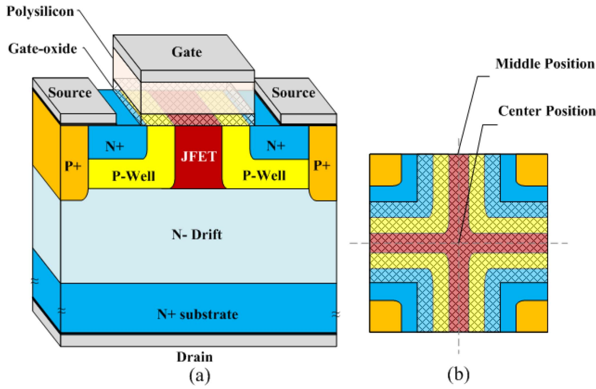
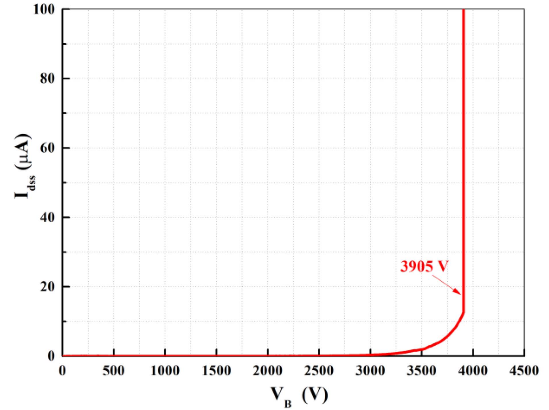


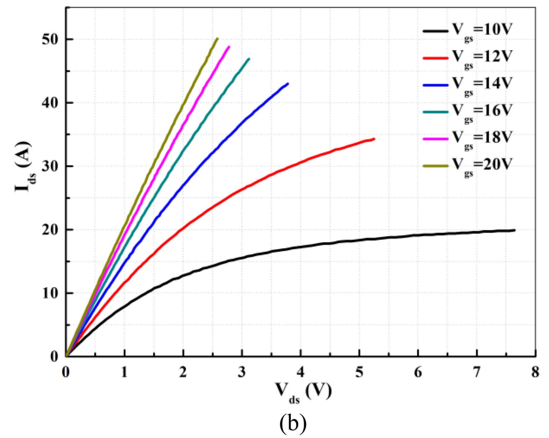
FIGURE 1. Cross section of the fabricated 3.3 kV planar-gate SiC MOSFET. (a) 3D schematic cross section, and (b) top view of the cell structure.

In this paper, the effects of JFET width (W_{JFET}) and JFET doping (JD) on the specific on-resistance ($R_{on,SP}$) and electric field of gate oxide (E_{ox}) of 3.3 kV SiC MOSFETs are systematically investigated by experiments and simulations. Furthermore, the effects of W_{JFET} on SC capability and the corresponding electro-thermal behaviors are studied in detail.

II. DEVICE FABRICATION AND SIMULATION BACKGROUND

In this work, 4-inch SiC wafers consisting of a 350-μm-thick N-type 4H-SiC substrate and 32-μm-thick N-type epitaxial layer with doping concentration of 2.1×10^{15} cm^{-3} are used to fabricate 3.3 kV SiC MOSFETs. The P-Well region is formed by high energy aluminum (Al) implantation, and the implant depth is 0.85 μm from the surface with highest doping concentration of 2×10^{18} cm^{-3}. The N+ source region is then formed by heavy dose nitrogen (N) implantation. P+ source region and the floating guard rings are formed by heavy dose Al implantation at the same time. The JD region is formed by multiple high-energy N implantation, and the implant depth is 0.8 μm from surface with doping concentration of 1×10^{17} cm^{-3}. The termination area is composed of 36 guard rings with 340 μm width. The space between two adjacent guard rings increases linearly with the initial space of 0.8 μm, and the common difference is 0.1 μm. The implants are activated in argon under 1750°C for 30 min. A 800 nm silicon dioxide (SiO_2) is deposited as field oxide and the active area is defined by wet etch. A 50 nm gate oxide is thermally grown in dry oxygen at 1300°C, and then post annealed in 10% nitric oxide diluted in nitrogen. Then, 500 nm thick polysilicon is deposited as gate and 800 nm SiO_2 is deposited as an inter-metallic dielectric medium and via holes are opened. After that, 50 nm 2.6% Al in nickel is deposited on the source and drain, then annealed at 980°C for 2 min by rapid thermal annealing process. A multi-layer metal of titanium (Ti) (20 nm)-Al (4000 nm)-Ti (20 nm) is deposited as a gate metal and is used to interconnect whole cells in the die. The 3D schematic cross-section and top view of the fabricated 3.3 kV planar-gate SiC MOSFET are shown in Fig. 1 (a) and (b), respectively. It consists of a square cell layout with channel length of 1 μm and JFET width (W_{JFET}) of 2.5-4.5 μm.





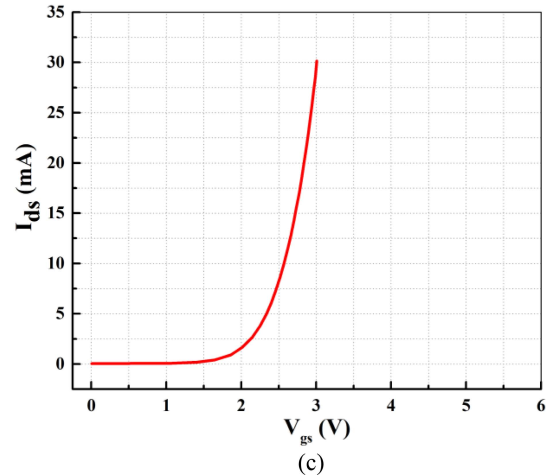


FIGURE 2. Static characteristics for 3.3 kV SiC MOSFET with W_{JFET} of 3.5 μm, without JD and active area of 0.557 cm^2. (a) Blocking current-voltage (I-V) curve at 25°C, (b) Output I-V curves at 25°C, (c) Transfer curves at 25°C.

In order to further investigate physics of the fabricated SiC MOSFETs, a detailed MOSFET structure is constructed accordingly through Sentaurus TCAD software. For static characteristics, the following models are used, including Shockley-Read-Hall and Auger recombination model, avalanche generation, band-gap narrowing, impact

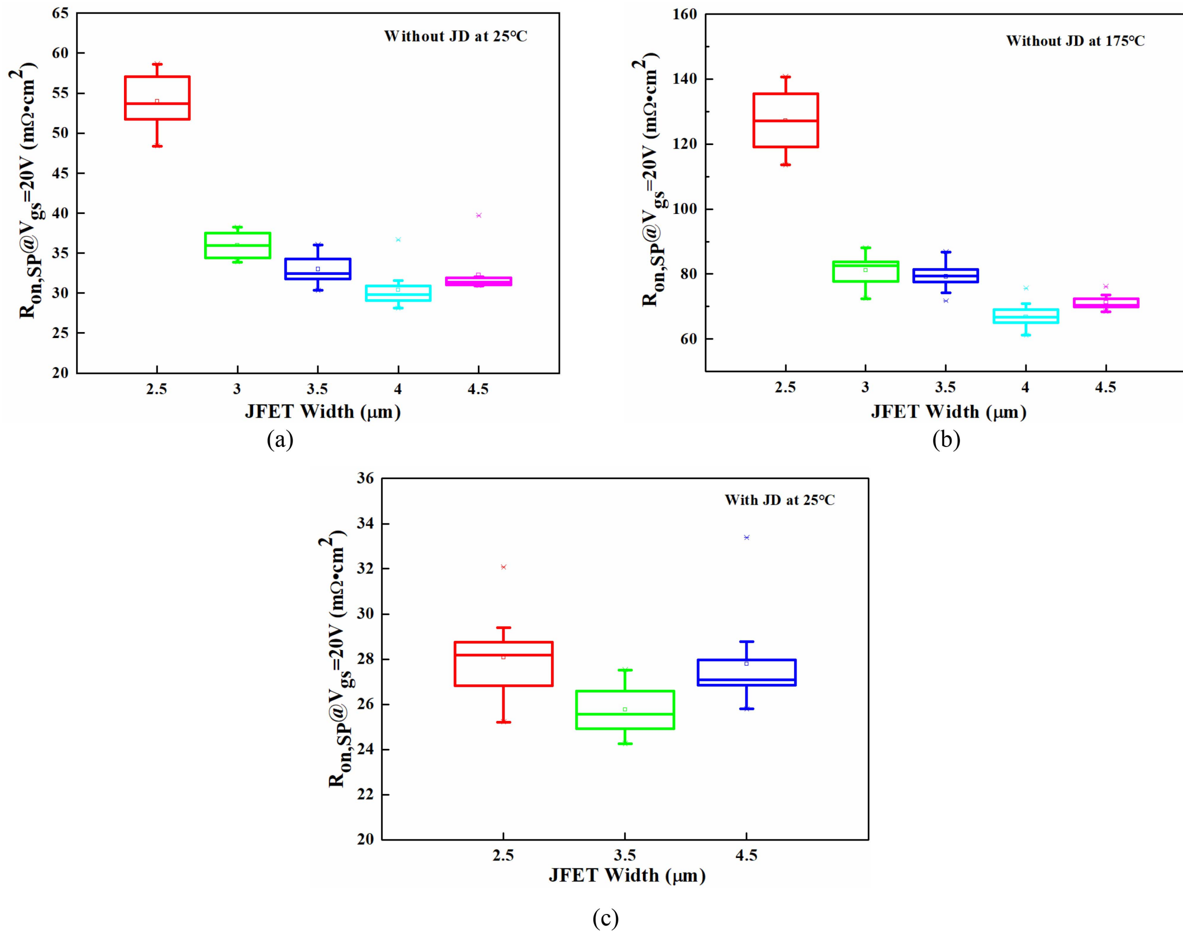


FIGURE 3. $R_{on,SP}$ of 3.3 kV SiC MOSFET with different JFET designs. (a) $R_{on,SP}$ Vs W_{JFET} (without JD) at 25°C, (b) $R_{on,SP}$ Vs W_{JFET} (without JD) at 175°C, (c) $R_{on,SP}$ Vs W_{JFET} (with JD) at 25°C.

ionization, incomplete ionization model, and traps and fixed charges model [12]. For SC characteristics, the thermodynamic model, full anisotropy and temperature dependence of thermal material properties are added.

III. RESULTS AND DISCUSSION

A. STATIC ELECTRICAL CHARACTERIZATIONS

The fabricated 3.3 kV SiC MOSFETs with W_{JFET} of 3.5 μm and without JD show the best trade-off among blocking voltage (V_B), drain-source current (I_{ds}) and SCWT. The corresponding static electrical characteristics are shown in Fig. 2. The measured V_B is 3905 V @source-drain leakage current (I_{dss}) = 12.6 μA, and the curve features hard breakdown with expected avalanche breakdown characteristic, as shown in Fig. 2 (a). When the gate bias (V_{gs}) is 20 V, the I_{ds} reaches as high as 50 A@drain-source conduction voltage ($V_{ds,on}$) = 2.5 V, as shown in Fig. 2 (b). The $I_{ds} - V_{gs}$ curve is measured at gate-drain short circuit condition, the threshold voltage (V_{th}) is 2.93V, as shown in Fig. 2 (c). The high V_{th} is also of great significance to prohibit fault conduction in traction inverters.

B. EFFECT OF JFET DESIGN ON $R_{ON,SP}$

The $R_{on,SP}$ of 3.3 kV SiC MOSFET is impacted by different JFET designs. As shown in Fig. 3 (a), the $R_{on,SP}$ with W_{JFET} of 2.5 μm and without JD is 54.0 mΩ·cm^2, while the $R_{on,SP}$ with W_{JFET} of 3 μm and without JD reduces to 37.5 mΩ·cm^2. When the W_{JFET} increases from 3 μm to 4 μm (without JD), the $R_{on,SP}$ only reduces to 34.26 mΩ·cm^2. When the W_{JFET} increases from 4 μm to 4.5 μm (without JD), the $R_{on,SP}$ increases from 30.3 mΩ·cm^2 to 32.3 mΩ·cm^2, due to the reduction of the cell density. When the temperature is increased from 25°C to 175°C, the $R_{on,SP}$ with W_{JFET} of 4.5 μm, 3.5 μm and 2.5 μm (without JD) increases by 38.7 mΩ·cm^2, 46.3 mΩ·cm^2 and 72 mΩ·cm^2, respectively, as shown in Fig. 3 (b). It is indicated that the W_{JFET} takes an obvious effect on the positive temperature coefficient of $R_{on,SP}$. When the JD concentration increases from background levels to 1×10^{17} cm^{-3}, there is a significant improvement in $R_{on,SP}$ for W_{JFET} of 2.5 μm. The $R_{on,SP}$ with W_{JFET} of 2.5 μm and with JD decreases from 54.0 mΩ·cm^2 to 28.1 mΩ·cm^2. However, the JD has little influence on the $R_{on,SP}$ with W_{JFET} of 3.5 μm and 4.5 μm, and the $R_{on,SP}$ only decrease to 25.8 mΩ·cm^2 and 27.8 mΩ·cm^2, respectively.

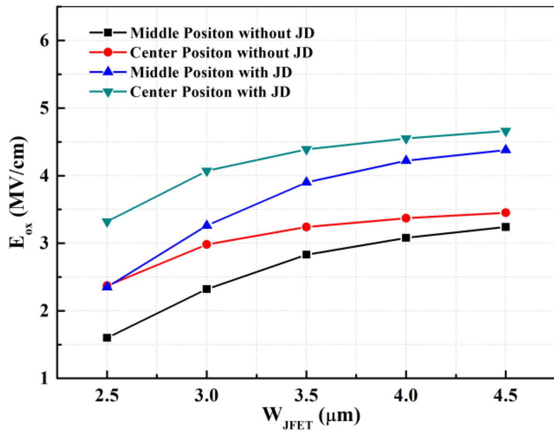


FIGURE 4. $E_{ox,max}$ at middle and center position when the V_B of 3.3 kV for the SiC MOSFET with various JFET design.

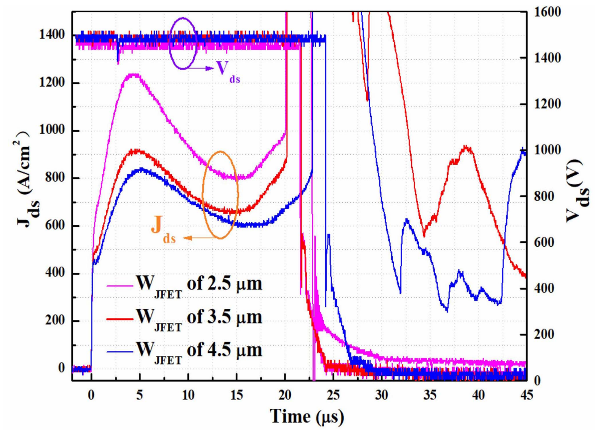


FIGURE 5. Tested SC waveforms of devices with different W_{JFET}.

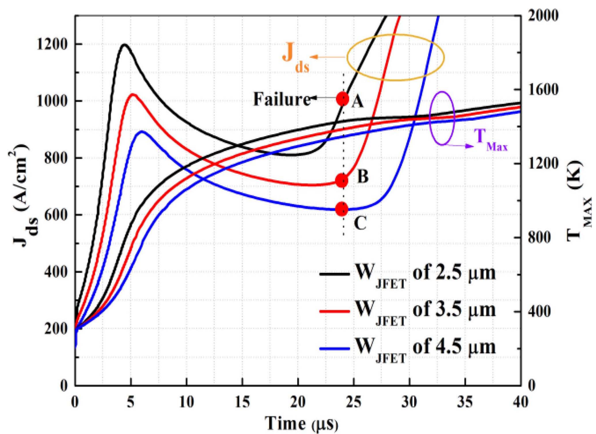


FIGURE 6. Simulated SC waveforms and T_{Max} of SiC MOSFETs with different W_{JFET}.

C. EFFECT OF JFET DESIGN ON $E_{OX,MAX}$

The maximum E_{ox} ($E_{ox,max}$) at middle and center position of the cell is shown in Fig. 4 for different JFET designs. In the simulation of the $E_{ox,max}$ at center position, the W_{JFET} is set to square root of 2 times of initial W_{JFET}. Regardless of presence or absence of JD, the $E_{ox,max}$ increases gradually when the W_{JFET} increases from 2.5 μm to 4.5 μm. For the deivce without JD, the $E_{ox,max}$ at middle position increases from 1.6 MV/cm to 3.4 MV/cm and $R_{on,SP}$ decreases from 54.0 mΩ·cm^2 to 32.3 mΩ·cm^2. Hence the trade-off between $E_{ox,max}$ and $R_{on,SP}$ should be considered when the JFET region is not doped. On the other hand, for the device with JD, the $E_{ox,max}$ at middle position increases from 2.4 MV/cm to 4.4 MV/cm, while there is slight change in $R_{on,SP}$ as shown in Fig. 3 (c). It is indicated that JD is useful to improve trade-off between $E_{ox,max}$ and $R_{on,SP}$. Obviously, JD can lead to an increasing of $E_{ox,max}$, compared with absence of JD. Therefore, the $E_{ox,max}$ should be optimized carefully when JD is used to reduce $R_{on,SP}$ of 3.3 kV planar-gate SiC MOSFET. The $E_{ox,max}$ of center position for either with JD or without JD is always higher than that at middle position. For the device with JD, the W_{JFET} should be less than 3 μm to ensure $E_{ox,max}$ below 4 MV/cm to prohibit the premature breakdown.

D. EFFECT OF W_{JFET} ON SC CAPABILITY

In order to investigate the effect of W_{JFET} on SC characteristics, the SiC MOSFETs without JD and W_{JFET} of 2.5 μm, 3.5 μm as well as 4.5 μm are utilized in this study. In the test condition, the SC pulse width is set to 50 μs. The V_{ds} is 1500 V, and the V_{gs} is 18 V/-5 V. The external gate resistance (R_g) is 10 Ω. There is an obvious difference in the SC waveforms of devices with different W_{JFET} as shown in Fig. 5. The SC peak current density of the devices with W_{JFET} of 2.5 μm, 3.5 μm and 4.5 μm are 1237 A/cm^2, 903 A/cm^2, and 828 A/cm^2, respectively. It decreases with increasing of W_{JFET}, because increasing W_{JFET} causes decreasing of channel density. With W_{JFET} increasing from 2.5 μm to 4.5 μm, the SCWT increases from 20.1 μs to 22.8 μs. The SC energy density (E_{SC}) is achieved by

$$E_{SC} = \int_0^{t_{SC}} V_{ds} J_d dt \tag{1}$$

where t_{SC} is SCWT, V_{ds} is the drain-source voltage, and J_{ds} is the density of drain-source current. The E_{SC} of devices with W_{JFET} of 2.5 μm, 3.5 μm and 4.5 μm are 23.4 J/cm^2, 19 J/cm^2, and 19.7 J/cm^2, respectively.

Furthermore, the simulated SC waveforms of SiC MOSFET with different W_{JFET} are also shown in Fig. 6. The simulated SC current and SCWT have same trend as the tested results, therefore the results can be used to explain the electro-thermal characteristics of SC event. With the increasing of W_{JFET}, the maximum temperature (T_{Max}) of device with W_{JFET} of 2.5 μm increases faster than that of devices with W_{JFET} of 3.5 μm and 4.5 μm. The extracted current density of electrons (J_e) and holes (J_h) from J_{ds} are shown in Fig. 7. The J_{ds} is mainly contributed by the J_e. The J_h starts to be activated at ∼1300 K, and the J_h increases quickly until the device falls into failure. When the W_{JFET} increases from 2.5 μm to 4.5 μm, the activation time of J_h is delayed due to the different increasing rate of T_{Max}.

In order to further figure out electro-thermal behaviors, the distributions of lattice temperature, J_h, J_e, and total current

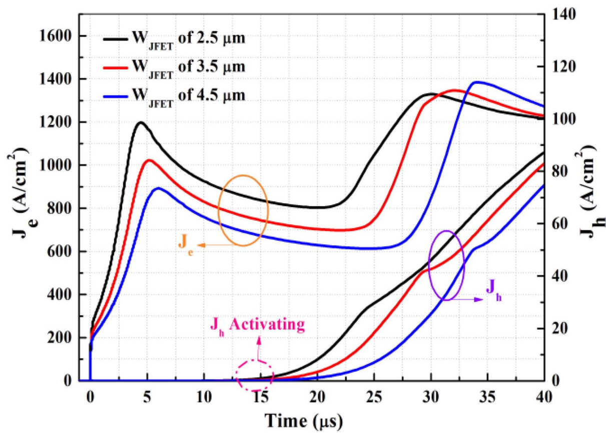


FIGURE 7. Extracted J_e and J_h from J_{ds} during SC event.

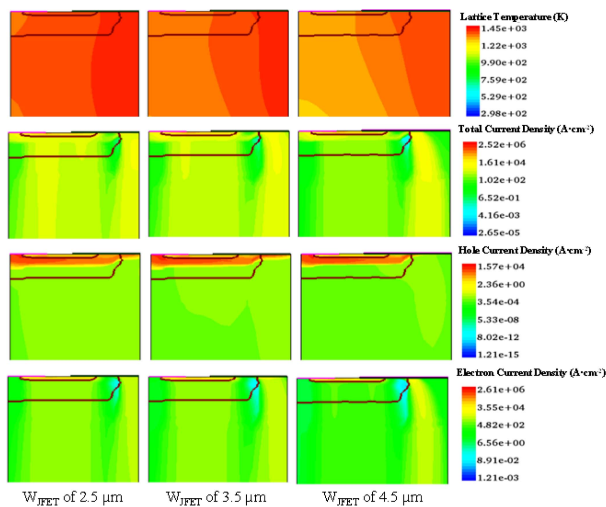


FIGURE 8. Distributions of lattice temperature, J_h, J_e, and total current density when the device with W_{JFET} of 2.5 μm reaches 1000 A/cm^2.

density are extracted from point A, B, and C of Fig. 6, as shown in Fig. 8. The T_{Max} is located at the JFET region, which decreases with the W_{JFET} increasing from 2.5 μm to 4.5 μm. This phenomenon could be explained by that the wider W_{JFET} provides more effective current paths for the SC current to decrease the power dissipation at the JFET region. The lower the T_{Max}, the fewer the number of activated holes. Hence, the J_h decreases gradually with W_{JFET} increasing from 2.5 μm to 4.5 μm. For the device with W_{JFET} of 2.5 μm, total current density between P-Well/N- drift junction is even comparable with the total current density at the JFET region.

IV. CONCLUSION

In this paper, the effects of W_{JFET} and JD on the conduction and SC capability of 3.3 kV planar-gate SiC MOSFETs are systematically investigated in detail. With the W_{JFET} increasing from 2.5 μm to 4 μm, the $R_{on,SP}$ of the devices without JD decreases, and the W_{JFET} plays a significant role in $R_{on,SP}$. When the W_{JFET} goes on increasing, the effects of reduction of cell density start to dominate instead of W_{JFET}. Meanwhile, the W_{JFET} has an obvious effect on the positive temperature coefficient of the $R_{on,sp}$ of devices without JD. With the temperature increasing from 25°C to 175°C, the $R_{on,SP}$ with W_{JFET} of 2.5 μm, 3.5 μm, and 4.5 μm increases by 38.7 mΩ·cm^2, 46.3 mΩ·cm^2, and 72 mΩ·cm^2, respectively. The JD adoption can effectively improve $R_{on,SP}$ while it may cause gate oxide reliability issues induced by increasing of $E_{ox,max}$. When the W_{JFET} is increased from 2.5 μm to 4.5 μm, the SCWT of the devices without JD increases from 20.1 μs to 22.8 μs, and the $R_{on,SP}$ decreases from 54.0 mΩ·cm^2 to 32.3 mΩ·cm^2 at 25°C. Hence, optimization of W_{JFET} can be used to improve both $R_{on,SP}$ and SCWT at the same time. The high conduction capability of 50 A with high avalanche breakdown voltage of 3905 V is realized for the device with W_{JFET} of 3.5 μm and without JD. Meanwhile, its SCWT is more than 20 μs. Up to now, both conduction capability and SCWT are state-of-the-art for 3.3 kV SiC MOSFETs. This paper provides important guidance for design 3.3 kV planar-gate SiC MOSFETs, which can be used to practical industrial and traction applications.

REFERENCES

[1] K. Puschkarsky, T. Grasser, T. Aichinger, W. Gustin, and H. Reisinger, "Review on SiC MOSFETs high-voltage device reliability focusing on threshold voltage instability," *IEEE Trans. Electron Devices*, vol. 66, no. 11, pp. 4604–4616, Nov. 2019, doi: 10.1109/ted.2019.2938262.

[2] Y. Mikamura *et al.*, "Novel designed SiC devices for high power and high efficiency systems," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 382–389, Feb. 2015, doi: 10.1109/ted.2014.2362537.

[3] X. Li *et al.*, "Achieving zero switching loss in silicon carbide MOSFET," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12193–12199, Dec. 2019, doi: 10.1109/TPEL.2019.2906352.

[4] F. Leonid, L. Xueqing, H. Xing, Z. Ke, and S. William, "Development of a high-performance 3,300V silicon carbide MOSFET," *Mater. Sci. Forum*, vol. 924, pp. 770–773, Jun. 2018, doi: 10.4028/www.scientific.net/MSF.924.770.

[5] S. Harada *et al.*, "3.3-kV-class 4H-SiC MeV-implanted UMOSFET with reduced gate oxide field," *IEEE Electron Device Lett.*, vol. 37, no. 3, pp. 314–316, Mar. 2016, doi: 10.1109/led.2016.2520464.

[6] M. Imaizumi and N. Miura, "Characteristics of 600, 1200, and 3300 V planar SiC-MOSFETs for energy conversion applications," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 390–395, Feb. 2015, doi: 10.1109/TED.2014.2358581.

[7] P. Blake, M. Kevin, C. Sauvik, and H. Chris, "3300V SiC DMOSFETs fabricated in high-volume 150 mm CMOS fab," *Mater. Sci. Forum*, vol. 924, pp. 731–734, Jun. 2018, doi: 10.4028/www.scientific.net/MSF.924.731.

[8] T. Tsuji, H. Shiomi, N. Ohse, Y. Onishi, and K. Fukuda, "3300V-class 4H SiC implantation-epitaxial MOSFETs with low specific on-resistance of 11.6mΩ cm^2 and high avalanche withstanding capability," *Mater. Sci. Forum*, vol. 858, pp. 962–965, May 2016, doi: 10.4028/www.scientific.net/MSF.858.962.

[9] L. Cheng *et al.*, "3300 V, 30 A 4H-SiC power DMOSFETs," in *Proc. Int. Semicond. Device Res. Symp. (ISDRS)*, College park, MD, USA, Dec. 2009, pp. 1–2, doi: 10.1109/isdrs.2009.5378284.

[10] X. Huang, L. Fursin, A. Bhalla, W. Simon, and J. C. Dries, "Design and fabrication of 3.3kV SiC MOSFETs for industrial applications," in *Proc. 29th Int. Symp. Power Semicond. Devices IC's (ISPSD)*, Sapporo, Japan 2017, pp. 255–258, doi: 10.23919/ISPSD.2017.7988908.

[11] J. Hernandez, F. Sutil, and P. Vidal, "Protection of a multiterminal DC compact node feeding electric vehicles on electric railway systems, secondary distribution networks, and PV systems," *Turk. J. Elect. Eng. Comput. Sci.*, vol. 24, pp. 3123–3143, Apr. 2016, doi: 10.3906/elk-1406-14.

[12] R. Huang *et al.*, "Design and fabrication of a 3.3 kV 4H-SiC MOSFET," *J. Semicond.*, vol. 36, no. 9, pp. 1–4, Sep. 2015, doi: 10.1088/1674-4926/36/9/094002.