Received 20 April 2020; revised 24 June 2020; accepted 21 July 2020. Date of publication 23 July 2020; date of current version 7 August 2020.
The review of this article was arranged by Editor J.-S. Goo.

Digital Object Identifier 10.1109/JEDS.2020.3011635

Parameter Extraction for the PSPHV LDMOS Transistor Model

KEJUN XIA (Senior Member, IEEE), COLIN C. MCANDREW (Fellow, IEEE), AND RONALD VAN LANGEVELDE (Member, IEEE)

Department of Front End Innovation, NXP Semiconductors N. V., Chandler, AZ 85224, USA

CORRESPONDING AUTHOR: K. XIA (e-mail: kejun.xia@nxp.com)

ABSTRACT This paper details a robust parameter extraction flow for the PSPHV LDMOS transistor model. The procedure uses a global scaling parameter set and accounts for self-heating. We describe how to determine parameters associated with important physical effects specific to PSPHV: non-uniform lateral channel doping; the Kirk effect; internal drain voltage clamping; and the drain expansion effect. The method is verified on devices from different technologies. Verilog-A code for PSPHV is publicly available.

INDEX TERMS MOSFET, LDMOS, parameter extraction, semiconductor device modeling, SPICE.

I. INTRODUCTION

Laterally diffused MOS (LDMOS) transistors are widely used in integrated circuits (ICs) for applications such as switch-mode power supplies, power amplifiers, power management, and motor drivers. Recently, we developed an accurate surface-potential based compact LDMOS transistor model PSPHV [1] to help design and optimize such ICs. PSPHV consists of an enhanced version of the PSP103.6 MOS transistor model [2] for the intrinsic channel, a modified version of the JFETIDG dual-gate JFET model [3] for the drift region, and JUNCAP2 [4], extended to improve modeling at high forward bias, for parasitic junction diodes. These components are integrated into a single Verilog-A code which is publicly available [5].

Compared to existing compact models for LDMOS transistors, such as SPHV [6], BSIM-HV [7], and the CMC standard model HiSIM_HV [8], PSPHV:

- models nonuniform lateral doping (NULD), from out-diffused channels and source-side halo implants
- models gradual channel turn-on
- does not exhibit unphysical spikes in capacitance versus voltage [9]–[12]
- includes a significantly more accurate avalanche current model, that accounts for the Kirk effect [13]
- as an option, can include reverse recovery modeling for the junction diodes.

A model is not useful without a procedure to extract parameters of the model to fit a wide variety of device types. The parameter extraction process for PSPHV is reasonably complex because LDMOS transistors are complex devices, hence PSPHV is a fairly complex model. This paper presents a robust extraction flow for PSPHV, to help modeling engineers use PSPHV for the devices they need to model. In particular, we introduce a self-heating effect (SHE) aware extraction flow. Previously proposed LDMOS model parameter extraction procedures, e.g., [14], determine values for temperature coefficients as a final step. However, output characteristics at the reference temperature T_r cannot be fitted without good values for temperature coefficients, because behavior at high gate bias V_{gs} and drain bias V_{ds} is affected by SHE. Our procedure improves on the prior art because it self-consistently accounts for SHE.

Our procedure includes extraction of capacitance parameters, but the focus is extraction of drain current parameters for full channel width and length scaling. We show the effect of parameters on capabilities unique to PSPHV: drain voltage scaling, the Kirk effect, internal drain voltage clamping, and the drain expansion effect. Our method is verified using devices from different technologies. Extraction of parameters for other parts of the model, such as gate current, parasitic junction diodes, noise, etc. is not detailed here, and follows the procedures defined for PSP [2].

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

In some instances, there may be unexpected device characteristics that cause issues with using a "canned" extraction program on a new device. Our procedure recognizes this fact: below "extract" means either an initial manual tuning, or small optimization, of one or a small number of parameters to fit a limited set of data, and "optimization" means the step is more substantial, and not manual, and involves adjusting multiple parameters to fit multiple data sets, often over geometry and temperature as well as over bias.

II. OVERVIEW AND GLOBAL SWITCHES

PSPHV inherits the local-global hierarchical parameter structure of PSP [15]. Model parameters can be specified at a local level, i.e., for one specific geometry, or at a global level. Here we use global level parameters. All PSPHV parameters are in SI units and here are typeset in `constantWidth` font.

PSPHV can model LDMOS transistors with different drift region structures, see Fig. 1. For devices like those, set `swtgmos` = 1 and `swbgmos` = 0; this defines the type of the top and bottom gates of the drift region as MOS and p-n junction, respectively.

Fig. 2 shows the equivalent circuit for PSPHV (this includes parasitics series resistance not explicitly shown in [1]). The optional second gate-drain overlap capacitance is turned on by specifying a positive value for the instance parameter `lgdov2`, the length of the second gate-drain overlap region, see Fig. 1, (note that the bulk connection of this component is moved from the di to the d node compared to [1]; this improves accuracy).

For LDMOS transistor structures like those of Figs. 1(a) and 1(c), the first gate-drain overlap region, whose length is specified by the instance parameter `lgdov`, covers only a small portion of the overall drift region length. The JFETIDG model, which is used for the drift region, assumes that depletion pinching occurs over the whole length of that region (which is true for the bottom gate of the drift region, the bulk). If parameters for the JFETIDG top gate depletion pinching effect are extracted at low V_{ds} they unphysically predict the drift region will pinchoff at high V_{ds}. For such structures, set `dfto` = 0, to turn off the top gate depletion pinching effect, and instead model drift region resistance modulation by the top gate via the `mumto` mobility modulation parameter.

For LDMOS transistor structures like Fig. 1(b), `lgdov` covers a substantial portion of the drift region and the JFETIDG top gate depletion pinching model can be used. Initial estimates of top gate depletion pinching factor `dfto` and built-in potential `psirto` are

$$d_{fto} = \frac{\sqrt{\epsilon_s/(qN_c)}}{t_m + t_{ox}\epsilon_s/\epsilon_{ox}}, \quad \psi_{rto} = \frac{q\epsilon_s N_c t_{ox}^2}{\epsilon_{ox}^2} - 2V_{FB,ov} \qquad (1)$$

where t_m is the drift region metallurgical thickness and t_{ox} is oxide thickness; ϵ_{ox} and ϵ_s are the permittivities of SiO_2 and Si, respectively, q is the magnitude of the electronic charge, N_c is the doping concentration in the drift region,

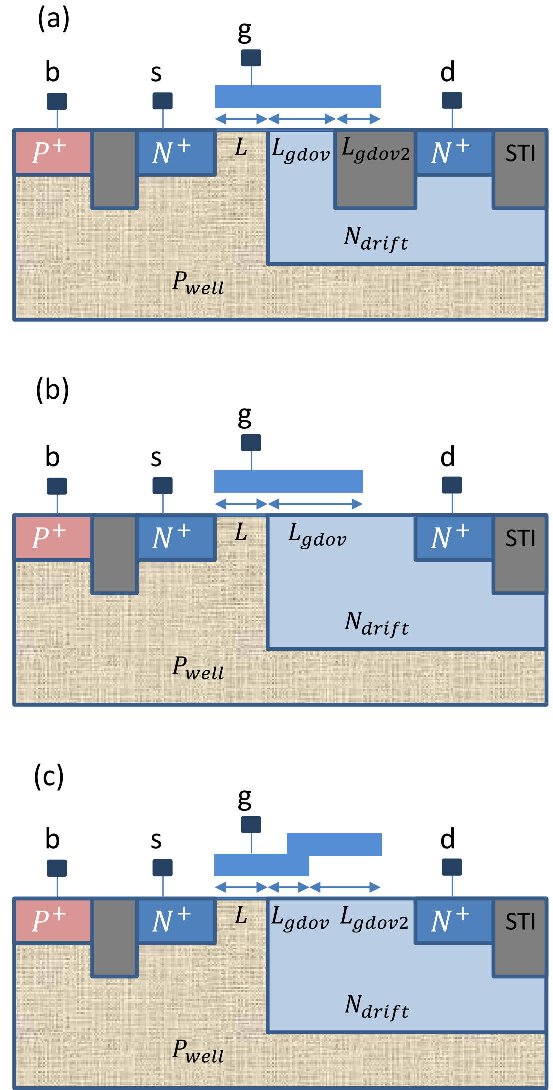


FIGURE 1. Cross-section of n-LDMOS transistors with different drift region designs.

assumed to be constant, and $V_{FB,ov}$ is the flat-band voltage of the overlap region.

Other important global switch settings:

- `swet`: set to 1 to turn on self-heating modeling (in which case either the thermal node must be connected to an external thermal network or the thermal resistance must be positive)
- `swvdscale`: set to 1 to turn on V_{ds} scaling to model NULD (this triggers a separate surface potential solution for charge calculations for the intrinsic MOS transistor, as when `swdelvtac` = 1)
- `swvdimp`: set to 1 to make PSP impact ionization calculations use V(d,s) instead of V(di,s) (this is necessary if V_{di} clamping is activated, when `swvdiclmp` = 1)
- `swdrlin`: set to 1 to have JFETIDG treat the drift region as a linear resistor (for debugging or to speed up simulations, with associated loss of accuracy of course)

JOURNAL OF THE
ELECTRON DEVICES SOCIETY

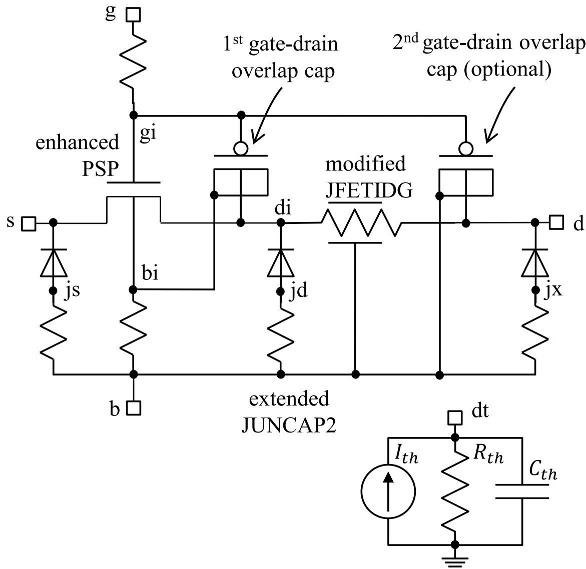


FIGURE 2. Large-signal equivalent circuit for PSPHV.

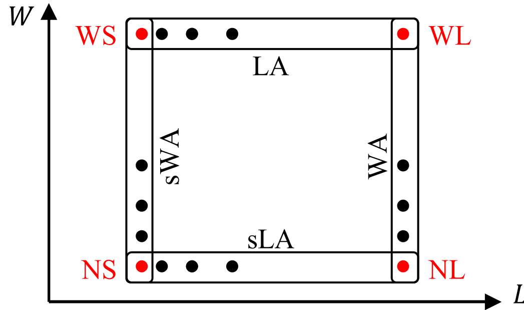


FIGURE 3. Device geometries for extraction.

- for swgeo, swedge, swigate, swimpact, swgidl, swjunc, swjunasym, swnud, and swdelvtac refer to the PSP manual [2]

III. DEVICE GEOMETRIES AND MEASUREMENTS

Figure 3 shows the device geometries that are needed to extract a fully scalable PSPHV model. WL, WS, NL, NS stand for the wide/long, wide/short, narrow/long, narrow/short devices, respectively. Besides the four corner geometries, there are primary and secondary width W and length L arrays. Because short and narrow channel effects vary roughly as $1/L$ and $1/W$, respectively, the length and width arrays should space geometries roughly equally in $1/L$ and $1/W$; this maximizes observability of parameters.

The following data are needed ($x = d, g, s, b$):

- DC data (all geometries and temperatures)
  - *idvg_lin:* $I_d(V_{gs})$ at low V_{ds}, over V_{bs} if the bulk and source are not tied together
  - *idvg_sat:* $I_d(V_{gs})$ and $I_b(V_{gs})$ at three or more high V_{ds} values and $V_{bs} = 0$
  - *idvd data:* $I_d(V_{ds})$ and $I_b(V_{ds})$ for several V_{gs} in strong inversion, $V_{bs} = 0$

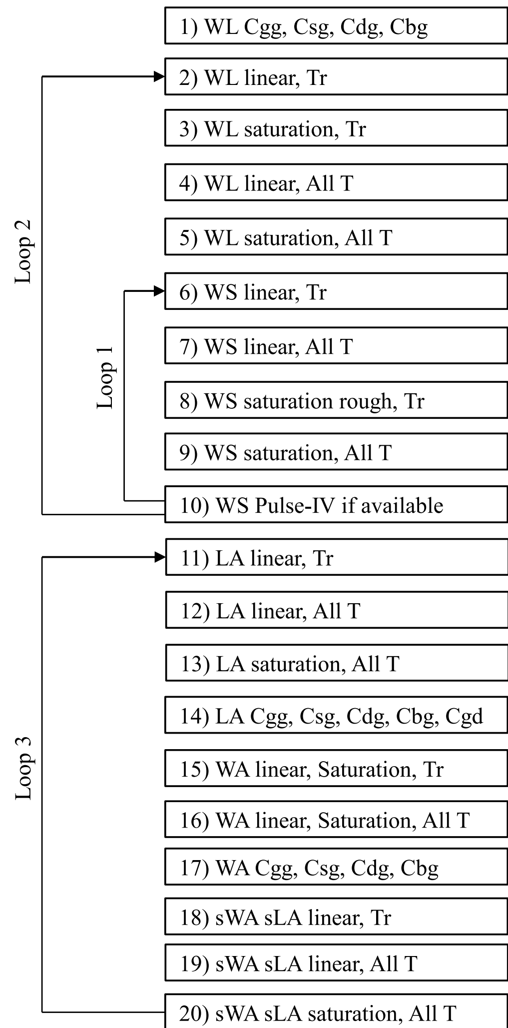


FIGURE 4. Extraction flow.

- CV data for WL, WS, NL, NS devices at T_r
  - *cxg:* $C_{xg}(V_{gs})$ at $V_{ds} = V_{bs} = 0$
  - *cgd:* $C_{gd}(V_{ds})$ at $V_{gs} = V_{bs} = 0$
- (optional) s-parameter data for the WS device at T_r
  - *y22:* $y_{22}(f)$ from 10 kHz to 10 MHz, $V_{gs} = V_{gs,max}/2$, $V_{ds} = V_{ds,max}/2$, $V_{bs} = 0$
  - *cxg_spar:* $C_{xg}(V_{gs})$ from s-parameters, for V_{gs} from $-V_{gs,max}$ to $+V_{gs,max}$, several values of V_{ds} from 0 to $V_{ds,max}/2$, $V_{bs} = 0$, $f = 2$ GHz
- (optional) pulsed IV data for the WS device at T_r
  - *idvd_pulse:* $I_d(V_{ds})$ and $I_b(V_{ds})$ for several V_{gs} in strong inversion, $V_{bs} = 0$

To avoid damaging devices, the highest V_{ds} for idvg_sat and idvd data may be limited to $V_{ds,max}/2$. Structures for capacitance and s-parameter data should have a sufficient number of gates N_g to enable reliable measurement.

IV. EXTRACTION FLOW

Fig. 4 shows the steps in our flow, which are detailed below. Unless otherwise stated, the data are for a 45V n-LDMOS

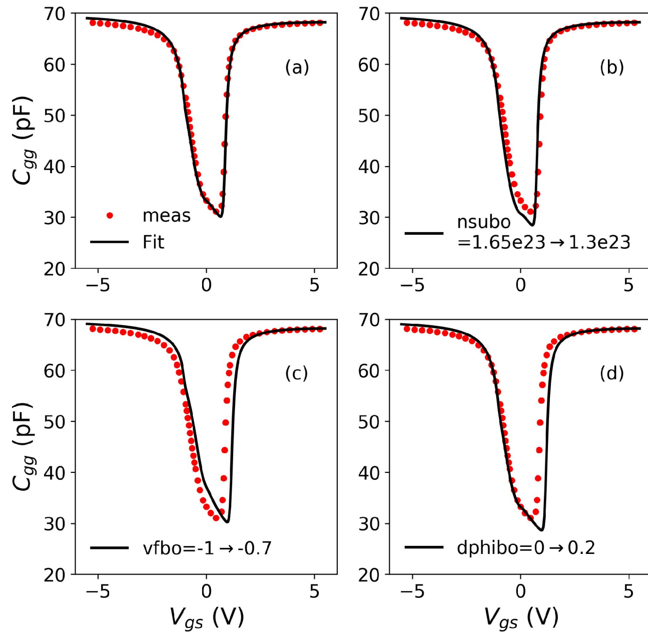


FIGURE 5. C_{gg} **of a WL transistor,** $W/L/N_g = 25\ \mu m/10\ \mu m/112$, $V_{ds} = V_{bs} = 0$ **V.**

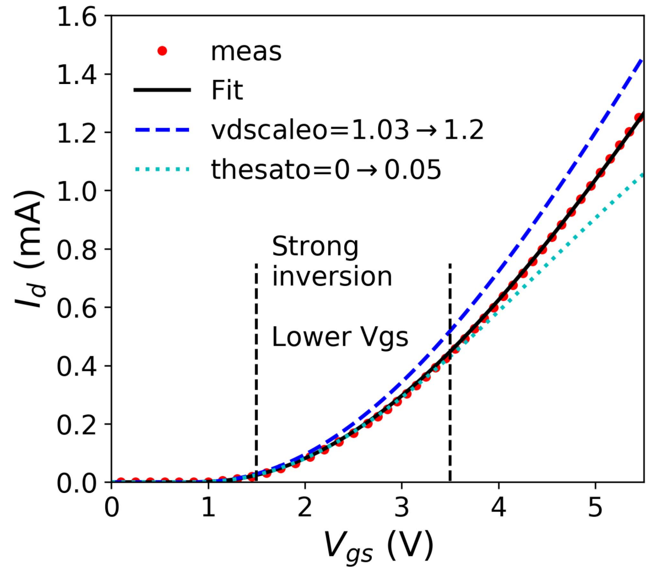


FIGURE 6. $I_d(V_{gs})$ **of a WL transistor,** $W/L/N_g = 25\ \mu m/25\ \mu m/2$, V_{ds}=28 **V and** V_{bs}=0.

transistor in a 90nm BCD technology at $T = T_r = 25$ °C, measured data are plotted as symbols, and PSPHV model results are plotted as lines. If devices have the bulk and source tied, omit parameters and steps that require V_{sb} to V_{bs} and I_b data.

Following the PSP parameter naming convention, `paramo` is the geometry independent part for `param` (WL device); `paraml` models the L dependence (WS device); `paramw` models the W dependence (NL); and `paramlw` models the area dependence (coupled L and W dependence, NS device). Refer to the Appendix for the meaning of each parameter.

Selection and technology parameters:

- set `type` to +1/−1 for n/p-type transistors, respectively
- set `tr` and `trj` to the reference temperature
- if the device has no halo implant, set `lpck` = 0
- set `lgdov` based on the device cross-section and layout
- for devices with a second gate-drain overlap region, set `lgdov2` and `toxovd2o` from technology data

JFETIDG has several ways to define and calculate the sheet resistance of the drift region, see [3, Fig. 4]; we recommend specifying `rsh0`.

Step 1: device: WL, data: cgg, temperature: T_r.

Extract the gate oxide thickness `toxo` by fitting the capacitance data for $V_{gs} = \pm V_{gs,max}$. Set `toxovo` = `toxovdo` = `toxo`. The bulk doping `nsubo` then determines the minimum C_{gg}, see Fig. 5(b). The flat band voltage `vfbo` shifts the whole C_{gg} curve horizontally, as Fig. 5(c) shows, and should be used to fit the data in depletion. The offset of the bulk potential ϕ_B, `dphibo`, only affects C_{gg} in inversion as Fig. 5(d) shows. Fig. 5(a) shows the final fit. If the influence of poly depletion is apparent include `npo`.

Step 2: device: WL, data: idvg_lin, temperature: T_r.

Extract `nsubo`, `dphibo`, and the interface charge factor `cto` to fit the data in weak inversion; if gradual channel turn on is apparent include the gate dependence of interface charge `ctgo`, see [1, Fig. 6]. For the data in strong inversion, extract mobility related parameters `uo`, `mueo`, `themuo` and, at high V_{bs}, the non-universality parameter `xcoro`.

Step 3: device: WL, data: idvg_sat, temperature: T_r.

Extract the velocity saturation parameters `thesato` and `thesatgo` at $V_{bs} = 0$, `thesatbo` at high V_{bs}. If the model underestimates I_d even with `thesato` = 0 use the V_{di} scaling parameter `vdscaleo`. Fig. 6 shows the effect of `vdscaleo` and `thesato`. `vdscaleo` affects strong inversion for all V_{gs}, `thesato` mainly impacts the higher V_{gs} region. Therefore, use `vdscaleo` to fit strong inversion data at lower V_{gs}. This V_{ds} scaling technique [16] is an important feature of PSPHV, not available in PSP, and significantly improves modeling of short channel devices where NULD is significant. A similar technique is also used in the BSIM-BULK model [17].

Extract the smoothing parameter `aro` of the new C^∞ V_{dsat} clamping function in PSPHV [18] by fitting the nonsaturation to saturation transition region.

Extract the avalanche current parameter `a1o`, `a2o`, `a3o` and `a3cvdo` to fit I_b. Fig. 11(b) shows the influence of `a3cvdl`; `a3cvdo` has similar effect.

Step 4: device: WL, data: idvg_lin, temperature: all.

Extract the temperature dependence parameters `stvfbo`, `stbeto`, `stmueo`, and `stthemueo` at $V_{bs} = 0$. From the data at high V_{bs} extract `stxcoro`.

Step 5: device: WL, data: idvg_sat, temperature: all.

Extract `stthesato` and, if `vdscaleo` is used, `stvdscaleo`.

The temperature dependence parameters for the WL device, which is not significantly affected by SHE, are

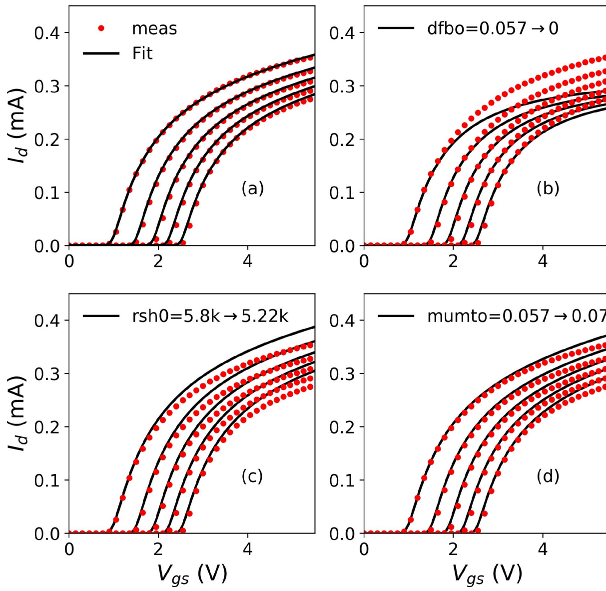


FIGURE 7. $I_d(V_{gs})$ of a WS transistor, $W/L/N_g = 25\ \mu m/1\ \mu m/2$, $V_{bs} = 0, -1.25, -2.5, -3.75, -5$ V, $V_{ds} = 0.1$ V.

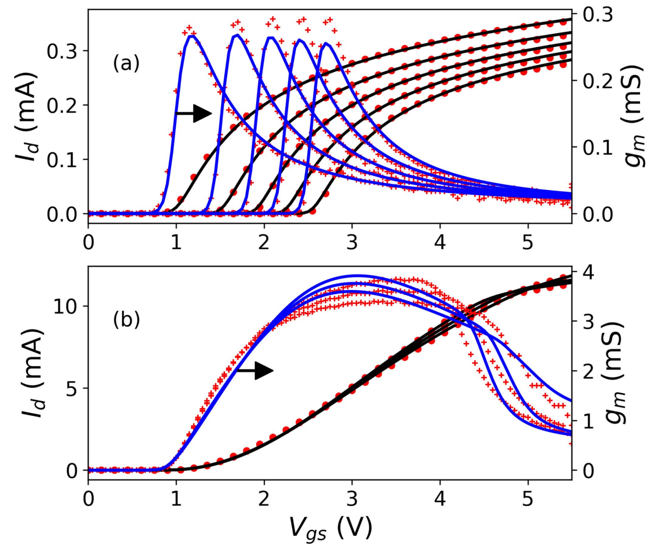


FIGURE 8. (a) $I_d(V_{gs})$ and $g_m(V_{gs})$, same transistor and biases as Fig. 7. (b) $I_d(V_{gs})$ and $g_m(V_{gs})$ for the same transistor, $V_{ds} = 12, 20, 28$ V, $V_{bs} = 0$ V.

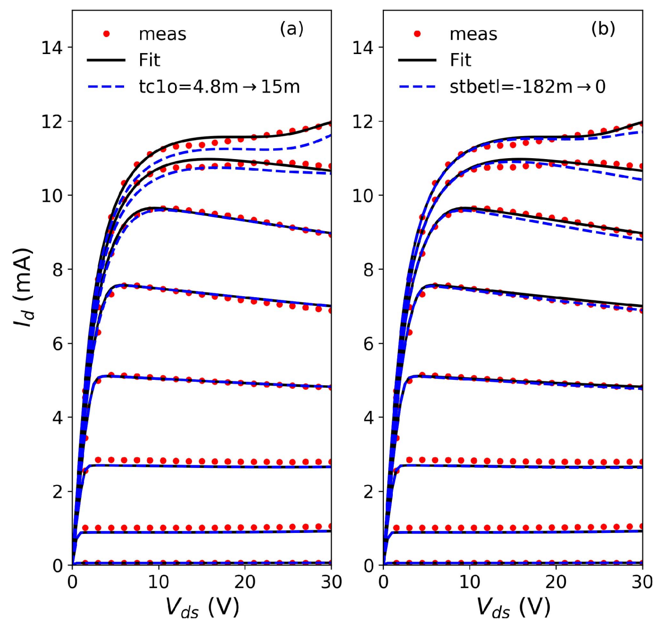


FIGURE 9. $I_d(V_{ds})$ of the WS transistor as Fig. 7 at different V_{gs}. The temperature coefficients tc1o (a) and stbetl (b), extracted from idvg_lin data, affect the saturation characteristics at T_r.

extracted before fitting the WS device, to ensure those parameters for the long channel device are correct.

Step 6: device: WS, data: idvg_lin, temperature: T_r.

Extract ctl, dphibl, and fol1 to fit I_d in weak inversion. The intrinsic series resistance rswl can be set to zero, its impact is small and can be subsumed into the drift resistance. Extract the drift region bottom gate depletion parameter dfbo to match the spacing between the curves for different V_{bs} at $V_{gs,max}$, see Fig. 7(b) for the impact of dfbo. Roughly extract the effective channel length offset parameter lvaro to fit the peak g_m. Figs. 7(c) and 7(d) show how rsh0 and mumto affect fitting; rsh0 has an influence over a wide range of V_{gs} whereas mumto affects fitting at high V_{gs}. By tuning lvaro, rsh0, and mumto, the nonsaturation data can be fitted well, as Fig. 7(a) shows. Fig. 8(a) shows g_m at different V_{bs}.

Step 7: device: WS, data: idvg_lin, temperature: all.

Extract the temperature dependence of the intrinsic MOS transistor channel mobility stbetl from peak g_m. Extract the temperature dependence of the drift region mobility, and hence resistance, tc1o and tc2o from the high V_{gs} region. Coupled through SHE, these parameters affect the saturation characteristics at T_r, see Fig. 9. This is why the temperature dependence of the nonsaturation characteristics must be extracted before fitting the saturation characteristics at T_r.

Note that tc1o and tc2o directly affect the temperature dependence of ecrito through $E_{crit} = V_{sat}/\mu$. This coupling complicates extraction but is crucial for self-consistent modeling of output characteristics with and without SHE, as noted in [1].

Step 8: device: WS, data: idvg_sat and idvd, temperature: T_r.

Here, the device characteristics are impacted by many physical effects such as the velocity saturation of the intrinsic MOS, the quasi-saturation of the drift region, and the impact ionization in both the intrinsic MOS and the drift region. This is a complicated part of LDMOS extraction: fitting at T_r, in the presence of SHE, depends on temperature coefficients of parameters that have influence in saturation, however from the previous step we only have, so far, temperature coefficients for the parameters dominant at low V_{ds}. This step is a first rough extraction, that is refined in the next step.

8.1 Extract the DIBL parameter cfl to fit idvg_sat data in weak inversion.

8.2 The thermal conductance in PSPHV scales as

$$g_{th} = g_{tho} + g_{thl}L + g_{thw}W + g_{tha}LW. \quad (2)$$

This points to "extract gtha from the WL device." However, SHE is weak for that device, to first order SHE decreases as $1/L^2$, so that is not possible. This leaves two practical options: extract gtha from the WS device; or use TCAD to develop a scaling equation based on thermal simulation, then extract a scale factor to calibrate the TCAD-based model so the PSPHV results match silicon data. It is possible to determine g_{th} for devices that exhibit negative g_o. However, in practice g_{th} scaling can be significantly more complex than (2), especially when multiple device fingers are included. Because of the high currents involved, it can be difficult to measure $I_d(V_{ds})$ at moderate to high V_{ds} for short multi-finger devices. For this reason we prefer to use TCAD to develop a scalable g_{th} model, including multi-finger devices.

g_{th} determines the (negative) slope in output characteristics at high V_{gs}. Fig. 10(a) compares idvd data with and without SHE. The scale factor for the TCAD based g_{th} scaling model is extracted to fit the slope at moderate V_{gs} biases, see the ellipse in Fig. 10(a).

8.3 Use the idvg_sat data before the onset of quasi-saturation to extract thesatl and vdscalel; their effect is the same as for the associated geometry independent parameters thesato and vdscaleo, respectively, see Fig. 6. Then use idvd data to extract the drift region velocity saturation parameters ecrito and ecorno for quasi-saturation effect; Fig. 10(b) and 10(c) show the effect of these parameters, respectively. The V_{dsat} smoothing parameter for short devices, arl, can also be used to tune the transition region, in concert with ecorno.

At high V_{gs} and moderate V_{ds}, the parameter for the Early effect in the drift region clm1l may be needed. Fig. 10(d), compared to Fig. 10(a), shows how clm1l affects the output conductance. Do not make clm1l too large otherwise it leads to overprediction of I_d in comparison to pulsed $I_d(V_{ds})$ data when SHE is turned off.

At this point, do not fit the high V_{gs} and high V_{ds} region because the avalanche current parameters have not been extracted.

8.4 To extract parameters for the avalanche current, note that it has components both from the intrinsic MOS transistor, at lower V_{gs}, and from the Kirk effect in the drift region, at higher V_{gs}, see Fig. 11(a). If you have to invoke V_{di} clamping, see Section V, set swvdimp = 1 to enable better avalanche current modeling.

Extract a1l, a3l, and a3cvdl to fit I_b at lower V_{gs}, Fig. 11(b) shows the effect of a3cvdl. Extract Kirk effect related parameters alphabo, beta, mhc, and jhc to fit I_b at higher V_{gs}. alphabo controls the magnitude of the avalanche current in the drift region, Fig. 11(c) shows the effect of setting it to zero (the increase in I_b at high V_{gs} in that plot is the result of using V(d,s) instead of V(di,s) to calculate the avalanche current, from swvdimp = 1). beta controls the spacing between the Kirk effect curves.

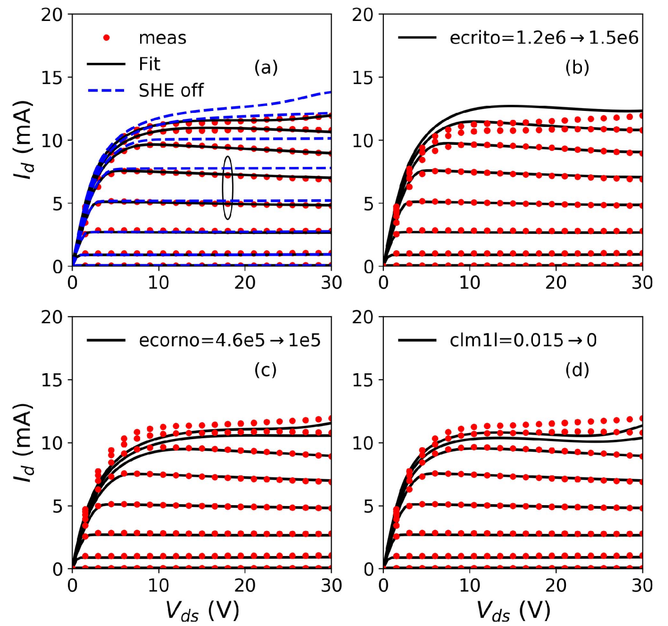


FIGURE 10. $I_d(V_{ds})$ of the WS transistor of Fig. 7 at different V_{gs}, $V_{bs} = 0$.

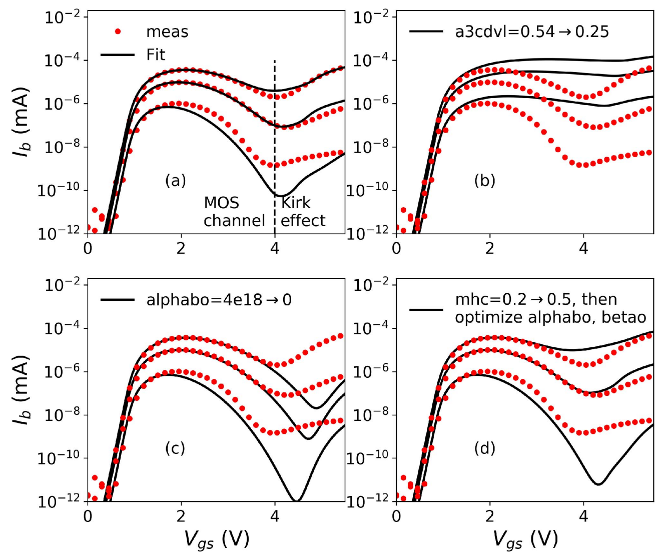


FIGURE 11. $I_b(V_{gs})$ of the WS transistor of Fig. 7 at different V_{ds}, $V_{bs} = 0$.

mhc reflects the influence of the doping profile of the drift region, increasing it lowers I_b at low V_{ds}, see Fig. 11(d).

Step 9: device: WS, data: idvd and y22, temperature: all.

First, extract tegth, the temperature coefficient of g_{th}, to fit g_o at all temperatures. Then extract xvsato, the temperature dependence of velocity saturation in the drift region, see Fig. 12(b). These temperature dependence parameters also affect fitting at T_r because of SHE, which is why WS saturation parameters need to be fitted to data from all temperatures.

Next, extract sta2o and xbeta for the temperature dependence of avalanche current. Extract the drain expansion parameters mumii1o and mumii2o (Section VI gives

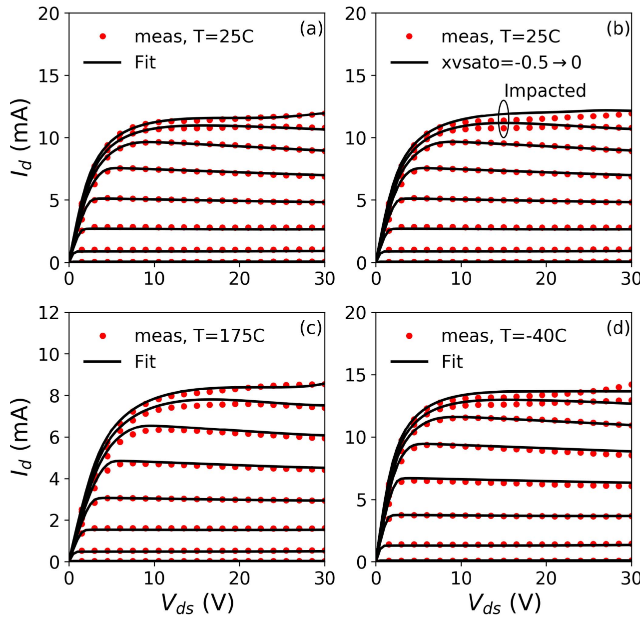


FIGURE 12. $I_d(V_{ds})$ **of the WS transistor of Fig. 7 at different** V_{gs}**, (a), (c), and (d) show fitting over temperature, (b) shows the impact of** `xvsato`**.**

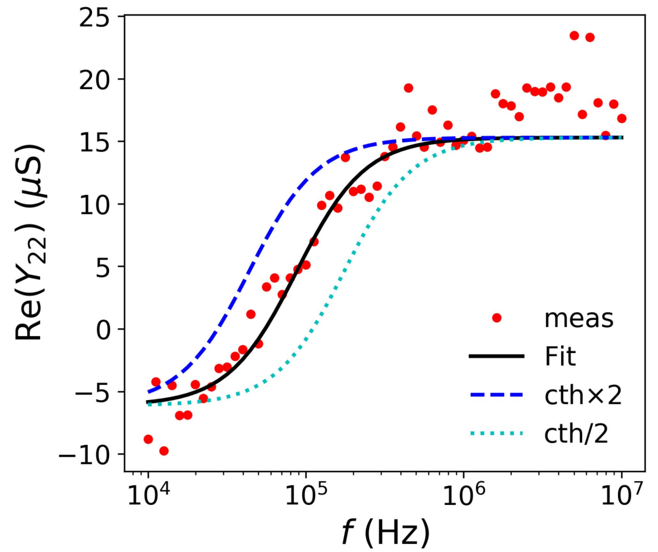


FIGURE 13. $\Re(Y_{22})$ **vs.** f **of a WS 90V p-LDMOS transistor,** $V_{gs} = 3.5$ **V,** $V_{ds} = 35$ **V,** $T = 27$ **°C.**

further details), and optimize `ecrito`, `gtha`, `tegth`, and `xvsato` to fit idvd data over all temperatures. Figs. 12(a), 12(c), and 12(d) show results after these steps at 25, 175, and −40 °C, respectively. Excellent fitting has been achieved. Fig. 8(b) shows that g_m at different V_{ds} is also modeled well.

To extract thermal capacitance parameters, the best approach is to develop a scaling model using TCAD, then use a scale factor to fit that model to $\Re$(y22) versus frequency, see Fig. 13. The thermal capacitance c_{th} adjusts the frequency at which g_o transitions from being affected, to not being affected, by SHE.

If y22 data are not available, measurements from a variety of devices show that thermal time constants for integrated devices vary from about 0.1 to 10.0 μs, with 1 μs being a typical value. So, set the scaling and value such that $c_{th}/g_{th} = 10^{-6}$ s.

Step 10: device: WS, data: idvd_pulse, temperature: T_r.

Because pulsed IV data remove the SHE they are useful to verify, and refine if necessary, the accuracy of modeling of g_o of the intrinsic transistor. If I_d in saturation in the pulsed IV data are not modeled accurately, adjust the channel length modulation parameter `clm1l` to improve the fit. See [1, Fig. 14] for an example. `clm1l` changes the slope of output curves in the quasi-saturation region. Note that pulsed IV and DC data cannot be fitted simultaneously; they are typically measured on separate structures, so local variation between devices and differences in series resistance between the structures affect the results. Factor those differences in when adjusting to fit the pulsed IV data.

Loop 1: To improve fitting in both nonsaturation and saturation for the WS device, repeat steps 6 through 10, see Fig. 4.

Loop 2: Repeat steps 1 through 10, see Fig. 4, to fine tune parameters for the WL device.

Step 11: devices: LA, data: idvg_lin, temperature: T_r.

This step determines "shape" parameters for the length dependence of wide devices in nonsaturation. Optimize `uo`, `lvaro`, and `lvarl` to fit peak g_m. (The other option is to use `fbet1` and `lp1` instead of `lvarl`.) Optimize `cto`, `ctgo`, `ctl`, and `ctlexp` to fit subthreshold slope. Optimize `nsubo`, `vfbo`, `dphibo`, `fol1`, `fol2`, `vfbl`, `dphibl`, and for devices with halo implants `lpck` and `npck`, to fit threshold voltage. Optimize `mueo`, `themuo`, `xcoro`, `rsh0`, `mumto`, and `dfbo` to fit data at high V_{gs}.

Step 12: devices: LA, data: idvg_lin, temperature: all.

This step determines "shape" parameters for temperature dependence over length of wide devices in nonsaturation. Optimize the temperature dependence parameters `stvfbo`, `stbeto`, `stmueo`, `stthemueo`, `stxcoro`, `stvfbl`, `stbetl`, `tc1o`, and `tc2o` to fit the idvg_lin data over temperature.

Step 13: devices: LA, data: idvg_sat and idvd, temperature: all.

This step determines "shape" parameters for the length and temperature dependence of wide devices in saturation. Optimize `cfl`, and `cflexp` to model DIBL in the idvg_sat data. Using both idvg_sat and idvd data, optimize `thesato`, `thesatl`, `thesatlexp`, `thesatgo` `vdscaleo`, `vdscalel`, and `vdscalele` to fit I_d before the onset of quasi-saturation onset, optimize `aro`, `arl`, `arlexp`, and `ecorno` to fit the region around the transition to saturation, and optimize `ecrito`, `gtha`, `tegth`, and `xvsato` to fit the quasi-saturation region.

Step 14: devices: WS, data: cgg, csg, and cdg, temperature: T_r.

This step fits source and drain overlap capacitances and the channel length offset for charge to fit total gate capacitance.

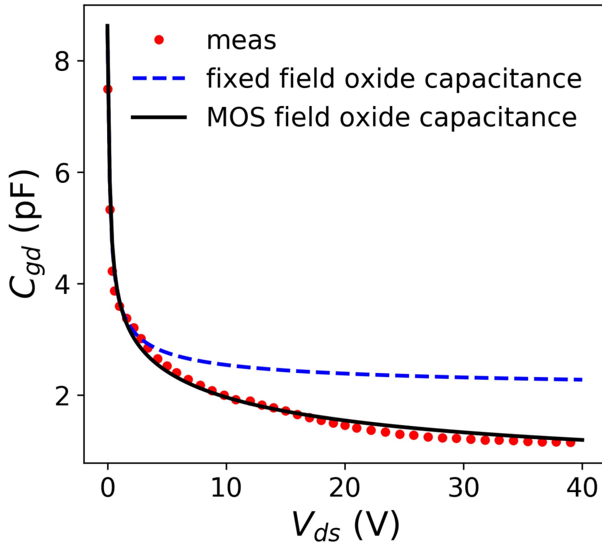


FIGURE 14. C_{gd} **vs.** V_{ds} **for a WS transistor,** $W/L/N_g = 25\ \mu m/1\ \mu m/280$**,** $V_{gs} = 0$**,** $f = 1$ **MHz,** $T = 25\ °C$**.**

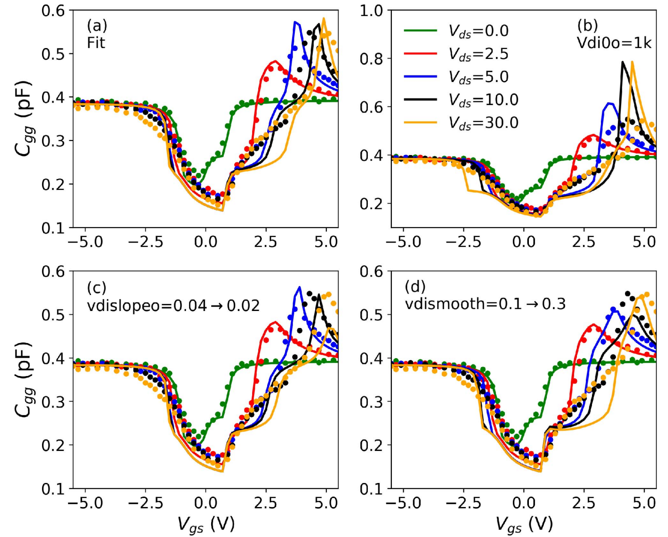


FIGURE 15. C_{gg} **vs.** V_{gs} **for a WS transistor,** $W/L/N_g = 10\ \mu m/1\ \mu m/8$**,** $f = 2$ **GHz,** $T = 25\ °C$**.**

Extract `lov`, `vfbov`, `novo`, and `cfrw` to fit csg, `xlgdovq`, `novdo`, and `vfbovd` to fit cdg, and `dlq` to fit cgg. The field plate can be modeled as a bias independent capacitor or as a MOS capacitor through `lgdov2` and `toxovd2o`. As Fig. 14 shows, the latter greatly improves C_{gd} modeling.

Step 15: devices: WA, data: idvg_lin and idvg_sat, temperature: T_r.

This step determines "shape" parameters for width dependence of long devices in both nonsaturation and saturation. From the idvg_lin data, extract the effective channel width offset parameters `wvaro` and `wvarw` to fit peak g_m (the other option is to use `fbetw1` and `betw1` instead of `wvarw`), extract `dphibw` to fit threshold voltage, and extract `muew` to fit I_d at high V_{gs}. From the idvg_sat data, extract `thesatw` and `vdscalew`.

Step 16: devices: WA, data: idvg_lin and idvg_sat, temperature: all.

This step determines "shape" parameters for temperature dependence over width of long devices in both nonsaturation and saturation. Extract `stvfbw` and `stbetw` to fit the idvg_lin data over temperature. Extract `stthesatw` and `stvdscalew` to fit the idvg_sat data over temperature.

Step 17: devices: WA, data: cgg and cbg, temperature: T_r.

This step fits gate-bulk overlap capacitance and the channel width offset for charge to fit total gate capacitance. Extract `cgbovl` to fit cbg, extract `dwq` to fit cgg.

Step 18: devices: sLA and sWA, data: idvg_lin, temperature: T_r.

This step determines "shape" parameters for coupled length and width interactions in nonsaturation. Extract `lvarw` to fit peak g_m. Extract `vfblw` and `dphiblw` to fit threshold voltage. Extract `ctlw` to fit subthreshold slope. Extract `xw` to fit I_d at high V_{gs}. Extract `dfbw` to fit the V_{bs} dependence at high V_{gs}.

Step 19: devices: sLA and sWA, data: idvg_lin, temperature: all.

This step fits the temperature parameters for coupled length and width interactions in nonsaturation. Extract `stvfblw` to fit threshold voltage, and `stbetlw`, `tc1w`, and `tc2w` to fit I_d at high V_{gs}.

Step 20: devices: sLA and sWA, data: idvg_sat and idvd, temperature: all.

This step fits coupled length and width interactions in saturation. Extract `thesatlw`, `vdscalelw`, and `ecritw` to fit both sets of data.

Loop 3: To improve fitting in both nonsaturation and saturation, over bias, geometry, and temperature, repeat steps 11 through 20, see Fig. 4.

V. V_{DI} CLAMPING AND ITS EFFECT ON C_{GD} AND Q_G

Figs. 15(a) and 15(b) show PSPHV modeling of gate capacitance with and without V_{di} clamping, respectively. The spikes at high V_{ds} visible in 15(b) are eliminated when V_{di} clamping is used, see 15(a). These spikes typically only occur for high voltage transistors; for low voltage transistors and transistors that do not exhibit such spikes in capacitance do not turn on V_{di} clamping (there is a computational cost associated with the clamping).

If the capacitances do exhibit spikes, set `swvdiclmp` = 1 and the clamping voltage parameter `vdi0o` to a starting value of $V_{gs,max}$. Note that data from *s*-parameter test structures are needed to extract V_{di} clamping parameters.

The parameter `vdislopeo` adjusts the V_{ds} dependence of the clamped V_{di}, see Fig. 15(c). `vdismooth` smooths the clamping, as Fig. 15(d) shows.

Adjust `vdi0o`, `vdismooth`, `vdislopeo`, and `vdislopego` (the V_{gs} dependence of the clamped V_{di}) to fit the measured C_{gg} data.

Fig. 16 shows the impact of V_{di} clamping on $C_{gd}(V_{ds})$, where the field plate is modeled as a bias independent plate capacitor. The modeled C_{gd} drops at the V_{di} clamping voltage because V_{ds} can no longer change the intrinsic transistor C_{gd}

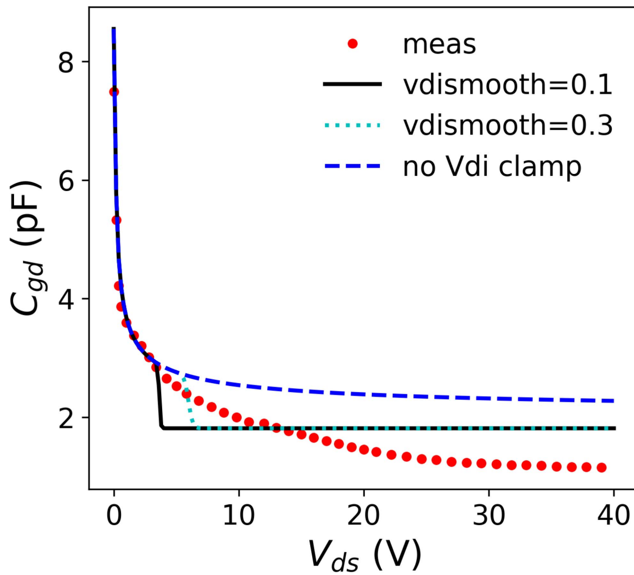


FIGURE 16. C_{gd} **vs.** V_{ds}**, same transistor as Fig. 14,** $V_{gs} = 0$**,** $f = 1$ **MHz,** $T = 25\,^{\circ}$**C.**

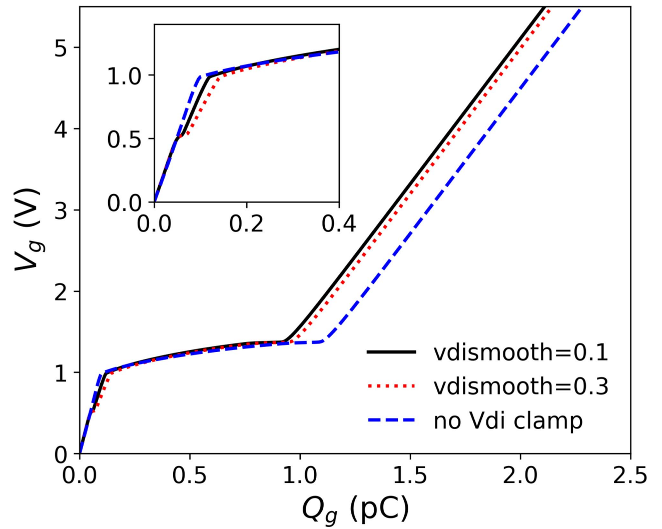


FIGURE 17. V_{gs} **vs.** Q_g **for a WS transistor,** $W/L/N_g = 30\ \mu$**m/1** μ**m/2,** $T = 25\,^{\circ}$**C.**

after V_{di} is clamped. In reality, the clamping occurs gradually, through the bias dependence of the lateral depletion in the gate-drain overlap region; this phenomena is not modeled physically in PSPHV. A larger `vdismooth` helps reduce the abruptness of the drop, see Fig. 16. For this device, the use of `lgdov2` readily gives a good fit, as Fig. 14 shows. However, for very high voltage devices, the drop in C_{gd} can happen even if a MOS, rather than fixed, capacitor is used for the second gate-drain overlap region. For such devices V_{di} clamping gives more accurate modeling of the total charge $\int C_{gd}\, dV_d$, and therefore more accurate modeling of switching losses.

Fig. 17 shows simulated gate charging characteristics, V_{gs} vs. Q_g. V_{di} clamping reduces the Q_g at which the transistor turns on, as expected. However, the clamping introduces a small kink at low V_{gs}, see the inset in Fig. 17. The kink becomes worse as `vdismooth` increases, so keep `vdismooth` ≤ 0.3.

VI. EXTRACTION FOR THE DRAIN EXPANSION EFFECT

PSPHV models the drain expansion effect [19] through modulation of the conductivity of the drift region by impact ionization. Fig. 18(a) shows $I_d(V_{ds})$ for a transistor with pronounced drain expansion; clearly, PSPHV can model this effect well. The body and source are shorted for this device, I_b is not directly available, so we fit I_d where it has a significant component from impact ionization.

Modeling the drain expansion effect requires simultaneous fitting of avalanche current and conductivity modulation by that current.

First, extract the intrinsic transistor avalanche parameters `a1o` and `a2o` to fit $I_d(V_{ds})$ at low V_{gs} and high V_{ds} (the avalanche current there is dominated by the intrinsic transistor), and to fit the data at moderate V_{gs}, where the Kirk effect

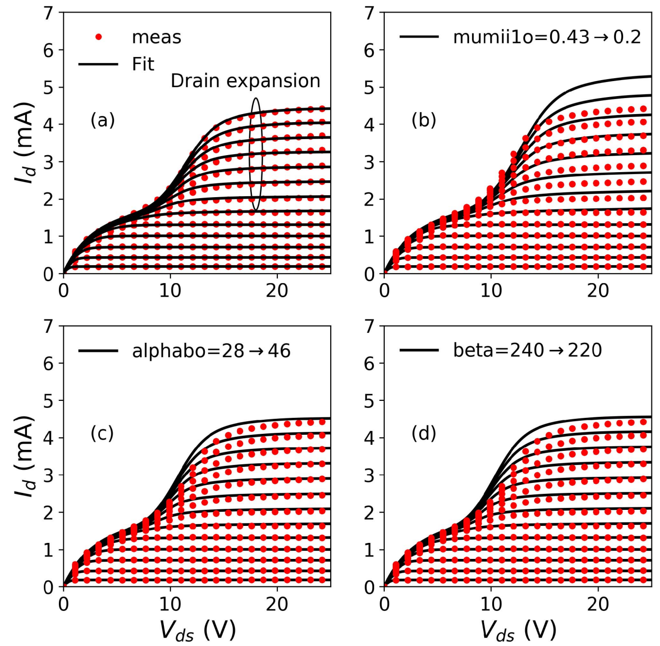


FIGURE 18. $I_d(V_{ds})$ **for a 65V power n-LDMOS transistor that exhibits strong expansion effect. Bottom to top:** $V_{gs} = 2$ **to 8 V by 0.5 V,** $T = 27\,^{\circ}$**C.**

in the drift region becomes significant, roughly initialize `beta` and `alphabo`.

Second, the parameter `mumii1o`, which models drift region conductivity modulation due to avalanche current, determines the point at which the expansion effect starts, see Fig. 18(b). Extract `mumii1o` to align this onset point between PSPHV and the data.

Third, extract `alphabo` to fit I_d at high V_{ds}. This parameter affects the whole expansion region, see Fig. 18(c). Tune `vdscaleo`, `thesato`, and `thesatgo` as well to fit I_d over all V_{ds}.

Finally, check the slope of I_d expansion just above the onset of the expansion effect. If the slope in the modeled I_d

is too small, first reduce beta and re-optimize. Fig. 18(d) shows the effect of beta on slope of the expansion effect. If the fitting is still not good enough, also include the second order conductivity modulation parameter mumii2o.

VII. CONCLUSION

We have described a global scaling, self-heating effect aware, large signal parameter extraction method for PSPHV. The parameters important for each extraction step are detailed, and graphical illustrations of the effect of key parameters for effects unique to PSP are provided, these include: drain voltage scaling; the Kirk effect in the drift region; internal drain voltage clamping to suppress spikes in capacitance; and the drain expansion effect. The extraction flow is verified against experimental DC and CV data from -40 ^{o}C to 175 ^{o}C. Fully scalable and accurate models have been extracted with this method.

APPENDIX

Below is the description of the used model parameters in alphabetical order. paramo/l/w/lw stands for the geometry independent parameter paramo and the geometry dependence parameters paraml, paramw, and paramlw. II means impact ionization, DR means drift region.

Parameter	Description
a1o/l	channel II pre-factor
a2o	channel II exponent
a3cvdo/l	drain voltage dependence of a3
a3o/l	saturation-voltage dependence of II
alphabo	DR bottom gate II magnitude
aro/l	saturation transition smoothing
beta	DR II current exponent for both gates
betw1	first higher-order width scaling coefficient of gain factor
cfl	length dependence of DIBL
cflexp	exponent for length dependence of DIBL
cgbovl	gate-bulk overlap capacitance per L_{EN}
clm1l	clm1 length dependence coefficient
ctgo	gate voltage dependence of interface states factor
ctho/l/w/a	thermal capacitance
ctlexp	exponent for length dependence of interface states factor
cto/l/w/lw	interface states factor
dfbo/w	DR bottom gate depletion factor
dfto	DR top gate depletion factor
dlq	effective channel length reduction for capacitance
dphibo /l/w/lw	offset of ϕ_b
dwq	effective channel width reduction for capacitance
ecorno	velocity saturation corner field
ecrito/w	velocity saturation critical field
fbet1/w	relative mobility decrease due to first lateral profile
fol1	first length dependence coefficient for short channel body effect
fol2	second length dependence coefficient for short channel body effect
gtho/l/w/a	thermal conductance
jhc	threshold current for DR impact ionization Kirk effect
lov	gate-source overlap length for capacitance
lpck	characteristics length of lateral doping profile
lp1	mobility-related characteristic length of first lateral profile
lvaro/l/w	difference between actual and programmed gate length
mhc	power for DR II current
mueo/w	mobility reduction coefficient
mumii1o	1st order DR II modulation effect
mumii2o	2nd order DR II modulation effect
mumto	DR top gate modulation effect on mobility
novdo	drain overlap region effective doping
novo	source overlap region effective doping
npck	pocket doping level
npo	gate poly-silicon doping
nsubo	bulk doping
psirto	twice the built-in potential of the DR top gate
rsh0	DR zero-bias sheet resistance
rsw1	Series resistance
sta2o	temperature dependence of a2
stbeto/l/lw	temperature dependence of gain factor
stmueo	temperature dependence of mue
stthemuo	temperature dependence of themu
stthesato/w	temperature dependence of thesat
stvdscaleo/w	temperature dependence of stvdscale
stvfbo/l/w/lw	temperature dependence of vfb
stxcoro	temperature dependence of xcor
tc1o/w	first order temperature coefficient for DR resistance
tc2o/w	second order temperature coefficient for DR resistance
tegth	thermal conductance temperature exponent
themuo	mobility reduction exponent

thesatbo	bulk voltage dependence of velocity saturation
thesatgo	gate voltage dependence of velocity saturation
thesatlexp	exponent for length dependence of thesat
thesato/l	temperature dependence of velocity saturation
toxo	gate oxide thickness
toxovd2o	oxide thickness for second gate-drain overlap
toxovdo	oxide thickness thickness for gate-drain overlap
toxovo	oxide thickness thickness for gate-source overlap
uo	zero-field mobility
vdi0o/l	clamping voltage for V_{di}
vdislopeo	drain voltage dependence of V_{di} clamping
vdislopgo	gate voltage dependence of V_{di} clamping
vdismooth	smoothing factor for V_{di} clamping
vdscalebo/l/w/lw	bulk voltage dependence of V_{ds} scaling
vdscalele	exponent for length dependence of V_{ds} scaling
vdscaleo/l/w/lw	V_{ds} scaling factor for NULD
vfbo/l/w/lw	flat-band voltage
vfbov	flat-band voltage for gate-source overlap
vfbovd	flat-band voltage for gate-drain overlap
wvaro/w	difference between actual and programmed field-oxide opening
xbeta	temperature exponent of DR II parameter beta
xcoro	non-universality parameter
xlgdovq	length offset for gate-drain overlap capacitance
xvsato	temperature exponent of DR saturated velocity
xw	DR width offset.

REFERENCES

[1] K. Xia, C. C. McAndrew, R. van Langevelde, G. D. J. Smit, and A. J. Scholten, "PSPHV: A surface-potential-based model for ldmos transistors," *IEEE Trans. Electron Devices*, vol. 66, no. 12, pp. 5246–5253, Dec. 2019, doi: 10.1109/TED.2019.2945832.

[2] *PSP 103.6 Model Manual*. Accessed: Sep. 2019. [Online]. Available: http://www.cea.fr/cea-tech/leti/pspsupport/Documents/psp103p6_summary.pdf.

[3] K. Xia and C. C. McAndrew, "JFETIDG: A compact model for independent dual-gate JFETs with junction or MOS gates," *IEEE Trans. Electron Devices*, vol. 65, no. 2, pp. 747–755, Feb. 2018, doi: 10.1109/TED.2017.2786043.

[4] A. J. Scholten, G. D. J. Smit, R. van Langevelde, and D. B. M. Klaassen, "The JUNCAP2 model for junction diodes," in *Compact Modeling: Principles, Techniques and Applications*. G. Gildenblat, Ed. New York, NY, USA: Springer, 2010, ch. 10, pp. 299–326, doi: 10.1007/978-90-481-8614-3.

[5] *PSPHV LDMOS 1.0.3*. Accessed: Apr. 2020. [Online]. Available: https://nanohub.org/projects/psphvldmos

[6] W. Yao, G. Gildenblat, C. C. McAndrew, and A. Cassagnes, "SP-HV: A scalable surface-potential-based compact model for LDMOS transistors," *IEEE Trans. Electron Devices*, vol. 59, no. 3, pp. 542–550, Mar. 2012, doi: 10.1109/TED.2011.2177092.

[7] H. Agarwal *et al.*, "BSIM-HV: High-voltage MOSFET model including quasi-saturation and self-heating effect," *IEEE Trans. Electron Devices*, vol. 66, no. 10, pp. 4258–4263, Oct. 2019, doi: 10.1109/TED.2019.2933611.

[8] H. J. Mattausch, M. Miyake, T. Iizuka, H. Kikuchihara, and M. M. Mattausch, "The second-generation of HiSIM_HV compact models for high-voltage MOSFETs," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 653–661, Feb. 2013, doi: 10.1109/TED.2012.2225836.

[9] Y. S. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroot, M. J. Declercq, and A. M. Ionescu, "Compact modeling of lateral nonuniform doping in high-voltage MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 6, pp. 1527–1537, Jun. 2007, doi: 10.1109/TED.2007.896597.

[10] M. B. Willemsen and R. van Langevelde, "High-voltage LDMOS compact model for RF applications," in *Int. Electron Devices Meeting (IEDM) Tech. Dig.*, Washington, DC, USA, 2005, pp. 208–211, doi: 10.1109/IEDM.2005.1609308.

[11] S. J. Sque, A. J. Scholten, A. C. T. Aarts, and D. B. M. Klaassen, "Threshold behavior of the drift region: The missing piece in LDMOS modeling," in *IEEE Int. Electron Devices Meeting (IEDM) Tech. Dig.*, Washington, DC, USA, 2013, pp. 336–339, doi: 10.1109/IEDM.2013.6724619.

[12] Y. S. Chauhan, "Compact transistor modeling of high voltage MOSFETs," Ph.D. dissertation, Eng. Sci. Tech. Gen. Electron. Lab., EPFL, Lausanne, Switzerland, 2007.

[13] A. W. Ludikhuize, "Kirk effect limitations in high voltage IC's," in *6th Int. Symp. Power Semicond. Devices Ics Tech. Dig. (ISPSD)*, Davos, Switzerland, 1994, pp. 249–252, doi: 10.1109/ISPSD.1994.583734.

[14] *HiSIM_HV 2.4.1 User's Manual*. Accessed: Mar. 2020. [Online]. Available: http://https://home.hiroshima-u.ac.jp/usdl/HiSIM_HV/index.html

[15] G. Gildenblat *et al.*, "Surface-potential-based compact model of bulk MOSFET," in *Compact Modeling: Principles, Techniques and Applications*, G. Gildenblat, Ed. New York, NY, USA: Springer, 2010, ch. 1, pp. 3–40, doi: 10.1007/978-90-481-8614-3.

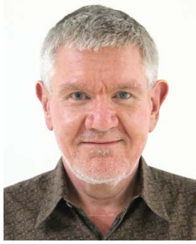
[16] K. Xia, C. C. McAndrew, R. van Langevelde, G. D. J. Smit, and A. J. Scholten, "Improved modeling of LDMOS with non-uniform lateral channel doping," in *Proc. Electron Devices Technol. Manuf. Conf.*, Singapore, 2019, pp. 124–125.

[17] C. Gupta, H. Agarwal, R. Goel, C. Hu, and Y. S. Chauhan, "Improved modeling of bulk charge effect for BSIM-BULK model," *IEEE Trans. Electron Devices*, vol. 66, no. 6, pp. 2850–2853, Jun. 2019, doi: 10.1109/TED.2019.2910107.

[18] K. Xia, "New c^{∞} functions for drain–source voltage clamping in transistor modeling," *IEEE Trans. Electron Devices*, vol. 67, no. 4, pp. 1764–1768, Apr. 2020, doi: 10.1109/TED.2020.2974790.

[19] P. Hower *et al.*, "A rugged LDMOS for LBC5 technology," in *Proc. 17th Int. Symp. Power Semicond. Devices ICs (ISPSD)*, Santa Barbara, CA, USA, 2005, pp. 327–330, doi: 10.1109/ISPSD.2005.1488017.

KEJUN XIA (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from Auburn University, Auburn, AL, USA, in 2006. From 2006 to 2014, he worked on SPICE modeling as a Senior Principal Member of Technical Staff with Maxim Integrated, Beaverton, OR, USA. From 2014 to 2019, he managed a device and product modeling team for NXP Semiconductors, Chandler, AZ, USA, where he currently manages a High Voltage and Analog Technology Development Team.



COLIN C. MCANDREW (Fellow, IEEE) received the B.E. (Hons.) degree in electrical engineering from Monash University, Melbourne, Australia, in 1978, the M.A.Sc. and Ph.D. degrees in systems design engineering from the University of Waterloo, Canada, in 1982 and 1984, respectively. From 1987 to 1995, he was with AT&T Bell Laboratories, Allentown, PA, USA. He is currently a Fellow with NXP Semiconductors, Chandler, AZ, USA.

RONALD VAN LANGEVELDE received the M.S. and Ph.D. degrees in electrical engineering from the Eindhoven University of Technology, The Netherlands, in 1994 and 1998, respectively. From 1998 to 2013, he worked with Philips Research, The Netherlands, in the fields of compact modeling for circuit simulation and analogue/RF IC-design. Since 2013, he has been worked with NXP Semiconductors, The Netherlands, as a Technical Director on spice modeling.