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Impacts of Vertically Stacked Monolithic 3D-IC Process on Characteristics of Underlying Thin-Film Transistor

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ABSTRACT In this work, the high-performance junctionless-mode (JL) and low-power inversion-mode (IM) polycrystalline-silicon (poly-Si) thin-film transistors (TFTs) with nanosheet channels (less than 10-nm in thickness) are vertically integrated in monolithic three-dimensional integrated circuit (3D-IC) structure. Both JL and IM TFTs can exhibit high on/off current ratio over 10^7 to demonstrate their performance. The JL TFT has much higher on-state current $\sim$ 24 times than it of the IM TFT. And the IM-TFT has much lower SS $\sim$ 0.104 V/decade and off-current $\sim$ 0.04 times than them of the JL TFT. However, the fabrication of the top-devices (JL TFTs) would degrade the performance of underlying-devices (IM TFTs), resulting in the threshold voltage shift of the IM TFTs from 0.61 to 2.17 V, SS increase from 0.104 to 0.218 V/decade and on-state current degradation from 16 to 3 mA. In order to further understand the reasons, the IM TFT with top-device removal process is also fabricated, which exhibits a partial recovery in performance. The results indicate the presence and fabrication process of the top-device would lead to the defect generation in the underlying-device. The results provide a new consideration for monolithic 3D-IC manufacturing technology.

INDEX TERMS Monolithic 3D-IC, nanosheet channel, low power, thin-film transistor.

I. INTRODUCTION

Polycrystalline-Silicon (poly-Si) thin-film transistors (TFTs) have been extensively studied for driving circuit of display panel, static random access memory (SRAM), dynamic random access memory, non-volatile memory, and three-dimensional integrated circuit (3D-IC) [1]–[7]. For the requirements of system-on-chip, high-performance devices and low-power devices need to be integrated in the same chip [8]–[10]. High-performance devices require high on-state driving current, although the off-state leakage current is also high. And low-power devices require low off-state leakage current, although the on-state current would also be lower. As for the high-performance characteristics of poly-Si TFT, junctionless-mode (JL) TFT is a good candidate because it can provide higher driving current due to the heavily doped poly-Si channel [11]–[15]. The JL TFT is an accumulation mode operated device, and its channel and source/drain are the same type of highly doped semiconductor, so there is no p-n junction. The conventional TFT needs to be induced the inversion layer by gate voltage for the carrier transport, so it is an inversion mode (IM) operated device. As for the low-power characteristics of poly-Si TFT, channel thickness thinning of conventional IM TFT is an effective manner to suppress the short-channel effect and leakage current [16]. Therefore, the nanosheet channel film of IM TFT is a suitable choice to realize the demand of low power characteristics. The electrical characteristics of both JL and IM TFTs are strongly related to the channel film thickness that thinner channel film thickness leads to lower subthreshold swing (SS), off-state leakage current and on-state driving current [15], [16]. Therefore, the JL TFT for high-performance applications and the IM TFT for

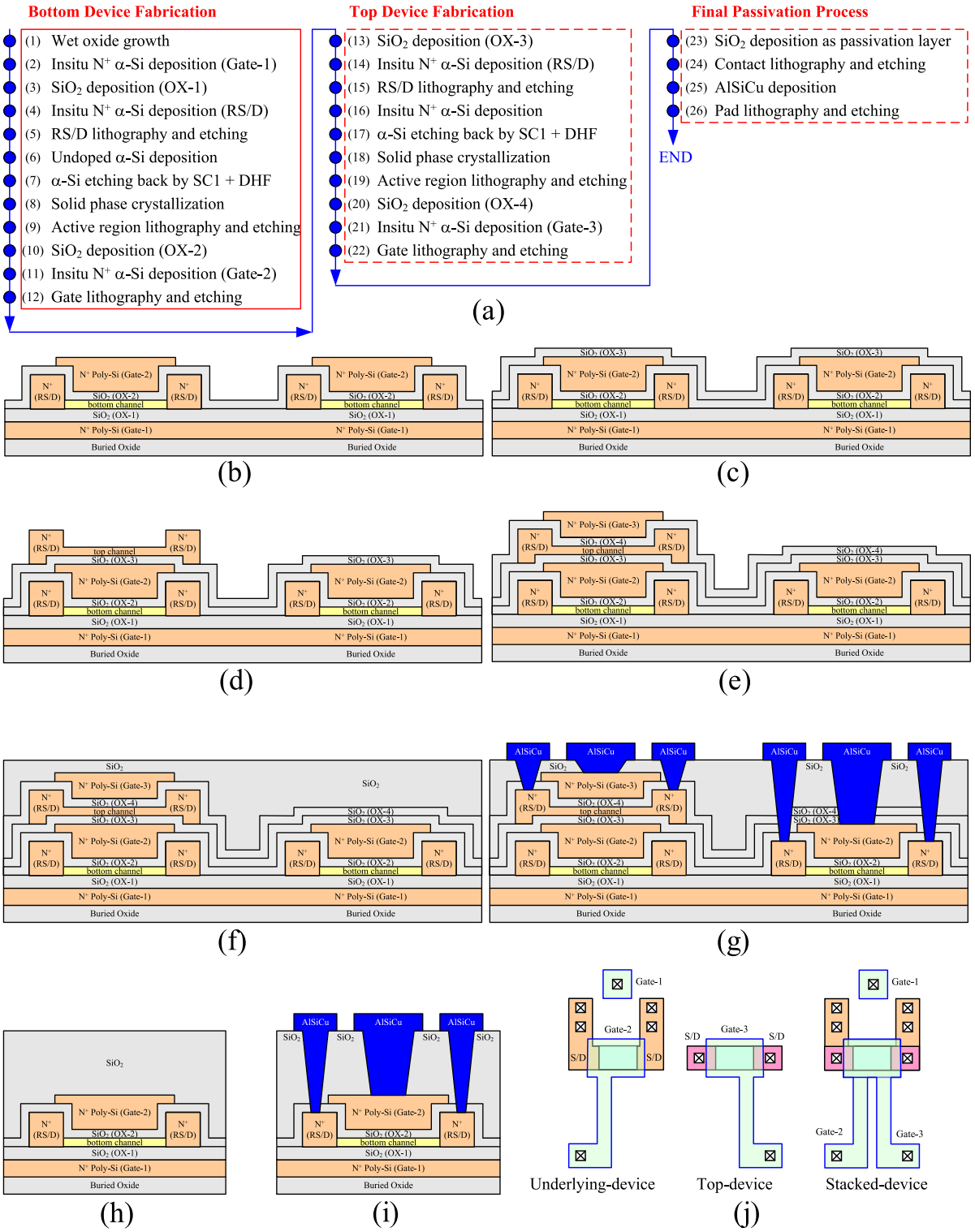

FIGURE 1. **(a) The fabrication process sequences of the vertically stacked JL and IM poly-Si TFTs in monolithic 3D-IC structure. Cross-sectional structure of vertically stacked JL and IM poly-Si TFTs after the fabrication sequence of (b) step 12, (c) step 13, (d) step 19, (e) step 22, (f) step 23 and (g) step 26. The single-layer IM TFT is fabricated by skipping process steps 13 ∼ 22 of Fig. 1(a) as shown in Fig. 1(h) and 1(i) to show the structure of IM-TFT after the fabrication process steps 23 and 26, respectively. (j) The schematic layouts of the vertically stacked JL and IM poly-Si TFTs.**

low-power applications would have different channel thickness options. In addition, high-density build-up of electronic devices is another development trend to reduce chip area and provide more functional circuit. Monolithic 3D-IC structure has been proposed to increase the device density in the same chip area by integrating devices vertically [5], [17]. It is

TABLE 1. Comparison of key parameters for IM poly-Si TFTs.

Items	unit	Single -layer	Dual -layer	Top-device Removal
W/L	μm/μm	100/10	100/10	100/10
V_{th}	V	0.61	2.17	1.50
SS	V/decade	0.104	0.218	0.169
I_{on}	μA	16	3	6
I_{min}	pA	0.7	0.1	0.1
I_{on}/I_{min}	$\times 10^7$	2.23	2.08	6.23
I_{Dsat}	μA	32.8	13.0	16.6
N_{it}	10^{12} #/cm^2	1.15	4.08	2.81
N_{GB}	10^{12} #/cm^2	2.73	3.57	3.14

ideal for use in memory circuits that require high device density stacking. In this work, the JL and IM TFTs are vertically integrated in monolithic 3D-IC structure. Moreover, the impacts of top-device (JL TFT) fabrication process on the performance of underlying-device (IM TFT) are also investigated. The comparison of electrical characteristics of the IM TFT between single-layer and dual-layer fabrication process would be important for the development of monolithic 3D-IC technology.

II. EXPERIMENTAL PROCEDURE

The fabrication process sequences of vertically integrated JL and IM TFTs are shown in Fig. 1(a). The 6-inch silicon wafer was initially oxidized to grow a 300-nm wet oxide layer as the buried oxide. The insitu doped N^+ amorphous-Si (α-Si) 50-nm and SiO_2 18-nm were deposited by low-pressure chemical vapor deposition (LPCVD) system as the bottom gate (Gate-1) and bottom gate oxide (OX-1). Then, a 50-nm N^+ α-Si was deposited by LPCVD and patterned to form the raised source/drain (RS/D) by lithography and etch process. A 20-nm undoped a-Si was deposited by LPCVD and etched back to 4-nm by $NH_4OH + H_2O_2 + H_2O$ (1:4:20) solution at 50°C and diluted-HF at room temperature. Then, solid phase crystallization (SPC) process was executed at 600°C in N_2 ambient for 24 hours. After active region patterning by lithography and etch process, a 14-nm SiO_2 and 50-nm N^+ α-Si were deposited by LPCVD and patterned as the top gate stack (OX-2 and Gate-2) to form the nanosheet IM TFT (underlying-device) and shown in Fig. 1(b). A 18-nm SiO_2 was deposited by LPCVD as the interlayer oxide (OX-3) as shown in Fig. 1(c), and a 50-nm N^+ α-Si was deposited by LPCVD and patterned to form the RS/D of top-device. A 20-nm N^+ α-Si was deposited by LPCVD and etched back to 8-nm with the same etching back process as the underlying-device. After the SPC and active region pattering process as shown in Fig. 1(d), a 14-nm SiO_2 and 50-nm N^+ α-Si were deposited by LPCVD and patterned as the top gate stack (OX-4 and Gate-5) to form the JL TFT (top-device) as shown in Fig. 1(e). A 300-nm passivation layer SiO_2 was deposited as shown in Fig. 1(f), and the contact holes were patterned. A 500-nm AlSiCu was deposited by sputter and patterned to form the probe pads. The vertically stacked JL and IM TFTs are completed in the monolithic 3D-IC structure as shown in Fig. 1(g). In order to study the impacts of top-device fabrication process on the performance of underlying-device, single-layer IM TFT is fabricated by skipping process steps 13 ~ 22 of Fig. 1(a) as shown in Fig. 1(h) and 1(i). The IM TFT with top-device removal process is also fabricated by skipping the lithography process in steps 15, 19 and 22 of Fig. 1(a) to remove the poly-Si layer of top-device after the deposition of each silicon film. The IM TFT in the top-device removal process can correspond to the case where the underlying-device and the top-device do not overlap at all in the 3D-IC process as shown in the right device of Fig. 1(b) to 1(g), which has the same thermal budget as it with dual-layer structure. The schematic layouts of the vertically stacked JL and IM poly-Si TFTs are shown in Fig. 1(j). The electrical measurement of drain current (I_D), gate voltage (V_G) and drain voltage (V_D) of devices with channel width/length (W/L) 100 μm/10 μm and 100 μm/1 μm are measured by the Keysight B1500A.

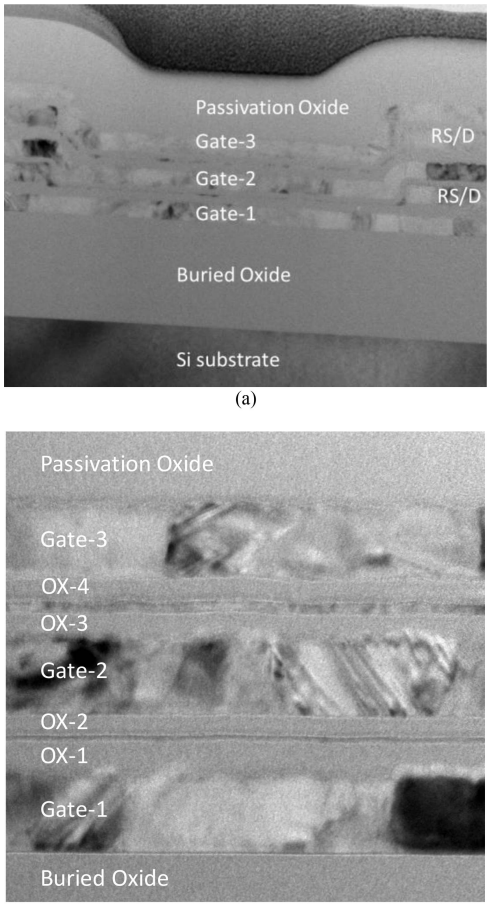

FIGURE 2. The transmission electron microscope image of (a) full structure and (b) channel region of the vertically stacked JL poly-Si TFTs and IM poly-Si TFTs with channel thickness t_{Si} = 4-nm.

III. RESULTS AND DISCUSSION

Figure 2 shows the transmission electron microscope images of vertically stacked JL and IM TFTs with nanosheet channel thickness t_{Si} = 8-nm and 4-nm respectively. The transfer

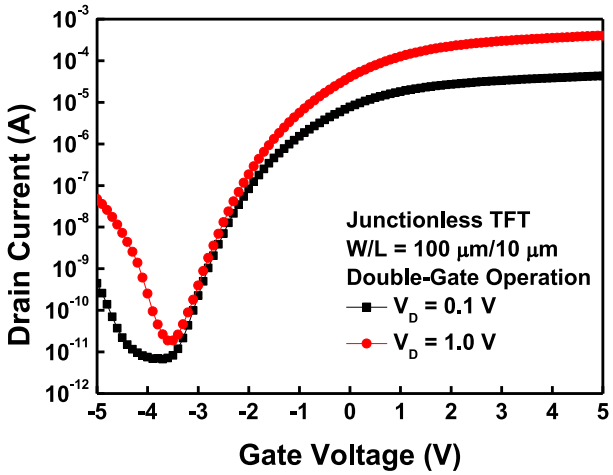

FIGURE 3. The $I_D - V_G$ curves of JL poly-Si TFT with double-gate operation.

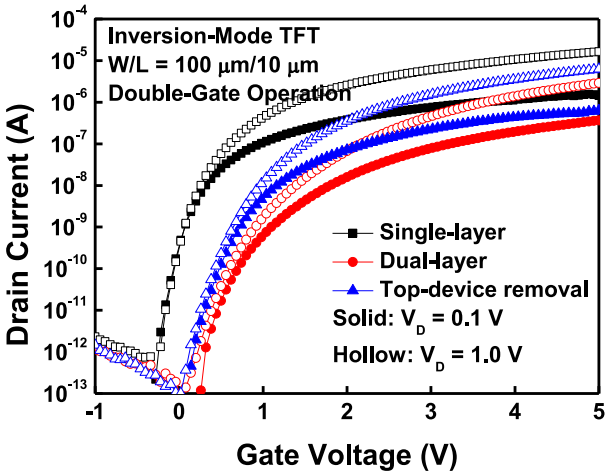

FIGURE 5. The $I_D - V_G$ curves of IM poly-Si TFT (underlying-device) with different fabrication process.

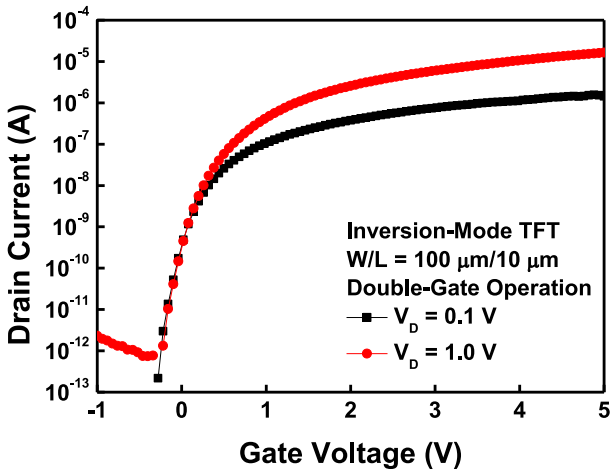

FIGURE 4. The $I_D - V_G$ curves of IM poly-Si TFT with single-layer process and double-gate operation.

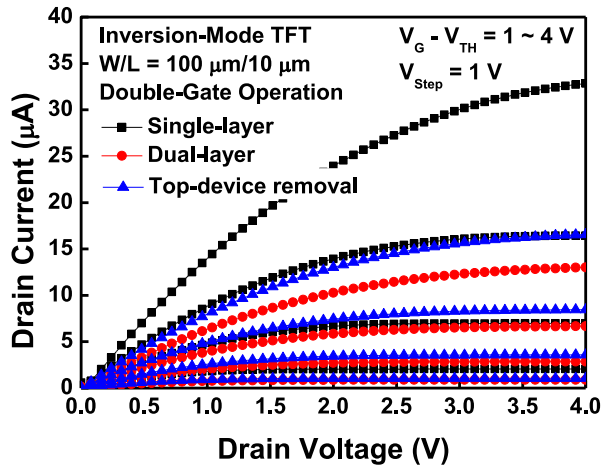

FIGURE 6. The $I_D - V_D$ curves of IM poly-Si TFT (underlying-device) with different fabrication process.

characteristics ($I_D - V_G$ curves) of JL TFT with double-gate operation are shown in Fig. 3. The JL TFT shows small threshold voltage (V_{TH}) ~ -1.58 V, low SS $\sim$ 0.341 V/decade and high on/off state current ratio (I_{on}/I_{min}) $\sim 2.13 \times 10^7$. The V_{TH} of JL TFT is defined as V_G at $I_D = 10$ nA x W/L, and the I_{on} and I_{min} are the maximum and minimum I_D at $V_D = 1$ V in Fig. 3. The transfer characteristics of IM TFT with single-layer process and double-gate operation are shown in Fig. 4. It exhibits small $V_{TH} \sim 0.61$ V, low SS $\sim$ 0.104 V/decade and high $I_{on}/I_{min} \sim 2.23 \times 10^7$. The V_{TH} of IM TFT is defined as V_G at $I_D = 10$ nA x W/L due to the thinner channel film and lower I_{on}. Both JL and IM TFTs exhibit high $I_{on}/I_{min} > 10^7$ to demonstrate their performance. The JL TFT has much higher I_{on} $\sim$ 400 mA than it of the IM TFT $\sim$ 16 μA due to the heavily doped poly-Si channel and thicker channel thickness, which is suitable as the high-performance devices. And the IM-TFT has much lower SS $\sim$ 0.104 V/decade and $I_{min} \sim 0.7$ pA than them of the JL TFT $\sim$ 0.341 V/decade and 18.8 pA due to the undoped poly-Si channel and thinner channel thickness, which is suitable as the low-power devices.

In this work, the JL and IM poly-Si TFTs are vertically integrated to form the monolithic 3D-IC structure, and the impacts of top-device (JL TFTs) fabrication process on the electrical characteristics of underlying-device (IM TFTs) are studied. The transfer characteristics of IM TFTs with different fabrication process are shown in Fig. 5, and some important parameters of IM-TFTs are listed in Table 1. All IM TFTs exhibit very low minimum leakage current I_{min} < 1 pA, which is attributed to the nanosheet channel. For the IM TFT with single-layer process, it shows good SS $=$ 0.104 V/decade, low $V_{TH} = 0.61$ V and high I_{on}/I_{min} ratio $\sim$ 2.23×10^7. However, the fabrication process of top-device degrades the performance of IM TFT. The degradation of transfer characteristics at $V_D = 1.0$ V of IM TFT with dual-layer process shows V_{TH} shift from 0.61 to 2.17 V, SS increase from 0.104 to 0.218 V/decade and I_{on} degradation from 16 to 3 μA. Figure 6 shows the output characteristics

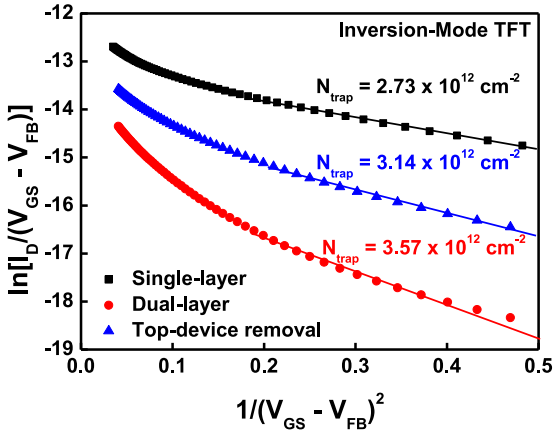

FIGURE 7. Plots of $\ln[I_D/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ curves of IM poly-Si TFT (underlying-device) with different fabrication process for the N_{GB} extraction. The flat-band voltage V_{FB} is defined as the gate voltage that yields the minimum drain current from the $I_D - V_G$ curves.

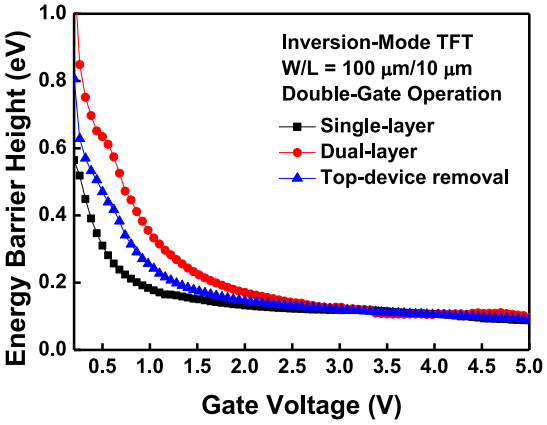

FIGURE 8. The $E_B - V_G$ curves of IM poly-Si TFT (underlying-device) with different fabrication process.

($I_D - V_D$ curves) of IM TFTs with different fabrication process, and the driving current (I_{Dsat}) at $V_G - V_{TH} = V_D = 4$ V of IM-TFTs with dual layer process also exhibits significant degradation from 32.8 to 13 μA compared to it with single-layer process. It indicates the fabrication process of top-device damages the underlying-device. In order to further understand the reasons, the IM TFT with top-device removal process is also fabricated, which has the same thermal budget as it with dual-layer structure. Figures 5 and 6 also show that the IM TFT with top-device removal process exhibits a partial recovery in performance compared to the presence of top-device that the V_{TH}, SS, I_{on} and I_{Dsat} are improved to 1.50 V, 0.169 mV/decade, 6 μA and 16.6 μA, respectively, but its performance still poor than it with the single-layer process. The SS increase of IM TFT with top-device fabrication process indicates the generation of interface trap state density (N_{it}) [18]–[20]. The N_{it} and grain boundary trap state density (N_{GB}) of the IM TFTs can be extracted from the SS and on-state current of the transfer characteristics in Fig. 5 [20]–[22], which are shown in Fig. 7 and also listed in Table 1. The results indicate the presence and fabrication process of top-device would lead to the trap state generation in the underlying-device that the N_{it} is increased from 1.15 x 10^{12} to 4.08 x 10^{12} cm^{-2} and the N_{GB} is increased from 2.73 x 10^{12} to 3.57 x 10^{12} cm^{-2}. It may be due to the film stress of several deposition of silicon film during the fabrication of top-device. Because the crystallization of a-Si would increase the atomic density and shrinkage the film thickness, it would provide a compressive strain to the underlying-device. Stress film technology has been widely used in the fabrication of advanced transistor. When a stress film is covered on a transistor using a single crystal channel material, the atomic spacing in the channel changes due to tensile or compressive stress, thereby changing the carrier mobility [23], [24]. However, the poly-Si channel films have many grain boundaries, and the grain boundary can be acted as a point of stress release to relieve stress, which causes many defects to occur and results in the generation of N_{it} and N_{GB}. In order to verify that the performance degradation is attributed to the generation of trap state density, the energy barrier height (E_B) of poly-Si channel of IM TFTs with different fabrication process are extracted and shown in Fig. 8. The E_B increase after the top-device fabrication process indicates the increase of trap state density of poly-Si channel film because the increase of trap state density would trap more charges, resulting in the higher energy barrier height [21], [25]. The removal of top-device can release the stress to decrease the N_{it} and N_{GB} from 4.08 x 10^{12} and 3.57 x 10^{12} cm^{-2} to 2.81 x 10^{12} and 3.14 x 10^{12} cm^{-2}, respectively, resulting in the reduction of E_B. The transfer and output characteristics of underlying IM TFT with shorter channel length 1 mm is also measured and shown in Fig. 9. The electrical degradation behaviors are still observed to show the V_{TH} shift from 0.90 to 1.78 V, the SS increase from 0.120 to 0.192 V/decade, and I_{on} degradation from 136 to 45 μA. The I_{Dsat} would also be degraded from 0.36 to 0.16 μA by the top-device fabrication process. The performance recovery behaviors of underlying IM TFT with top-device removal process are also exhibited that the V_{TH}, SS, I_{on} and I_{Dsat} are improved to 1.54 V, 0.177 mV/decade, 67 μA and 0.21 μA, respectively. It indicates that the performance degradation effect of underlying IM TFT with shorter channel length by the top-device fabrication process could be expected.

The underlying IM TFT with top-device removal process can correspond to the case where the locations of underlying-device and top-device have a large offset distance and do not overlap at all in the 3D-IC structure as shown in Fig. 1(g). This points out that the electrical characteristics of devices in different layers are not the same, even if the devices have the same dimension. The inconsistent electrical characteristics of devices in different layer of 3D-IC structure would cause serious performance degradation effects in circuit applications. Compared with the SRAM with a single-layer device architecture, if the SRAM with a vertically stacked 3D-IC structure uses the underlying device as the n-channel transistor, the static noise margin (SNW) in the butterfly curve of

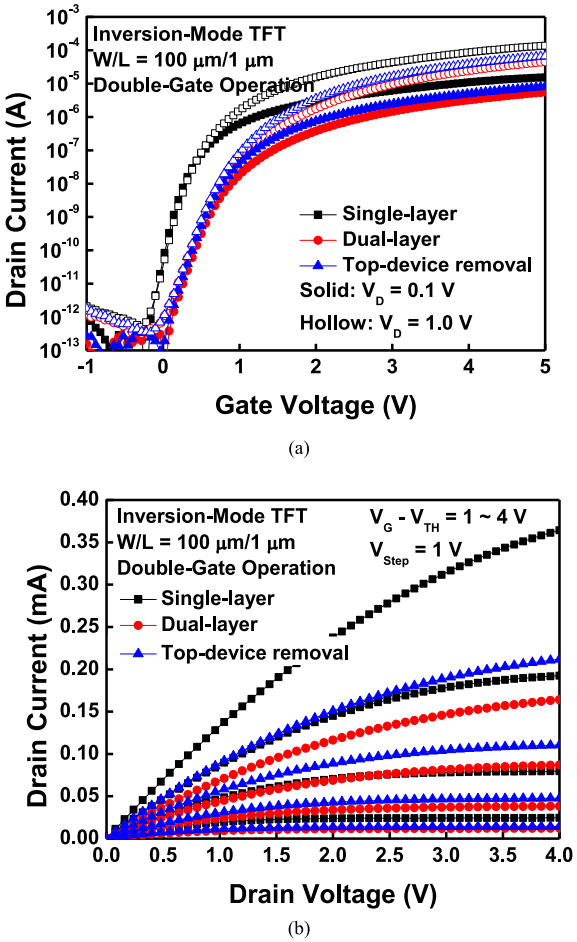

FIGURE 9. **(a) The $I_D - V_G$ and (b) $I_D - V_D$ curves of IM poly-Si TFT (underlying-device) with W/L = 100 μm/1 μm and different fabrication process.**

the SRAM becomes smaller. If the SRAM made of top-layer devices are used in part and the underlying-layer devices are used in part, the SNW in the butterfly curve will not only be decreased but also be asymmetric [26]. In order to reduce the top-device fabrication effect, the inter-layer dielectric (ILD) between top and underlying devices should be thicker to release the stress originating from process steps of top-device [27], [28]. A thicker ILD can relieve the effect of the stress layer on the upper layer to reduce the deterioration of the underlying devices. In addition, the use of thinner poly-Si channel and gate oxide layer of TFT is more suitable for 3D-IC fabrication. This is because the thinner channel thickness has less stress on the underlying-device, resulting in lower degradation effect. Thanks to the higher gate capacitance, the poly-Si TFT with thinner gate oxide would have stronger immunity against the variation of trap state density caused by the top-device fabrication process, alleviating degradation of V_{TH} and SS [29]. The effect of trapped charges due to the increased defects on the gate electrostatic control of the device can be reduced by increasing the gate capacitance [30]. It would provide a new consideration for monolithic 3D-IC manufacturing technology.

IV. CONCLUSION

High-performance JL TFTs and low-power IM TFTs with nanosheet channel have been demonstrated and vertically integrated to form the monolithic 3D-IC structure. The impacts of the fabrication process of top-device on the performance of underlying-device are also analyzed. The performance degradation of the underlying-device with dual-layer structure is attributed to the defect generation during the top-device fabrication. The performance of the underlying-device with dual-layer fabrication process can be partially recovered when the top-device is removed. The results indicate the presence and fabrication process of top-device would result in the trap state generation in the underlying-device. The defect generation may due to the film stress of silicon film during the fabrication of top-device.

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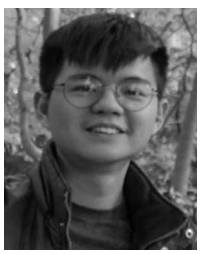

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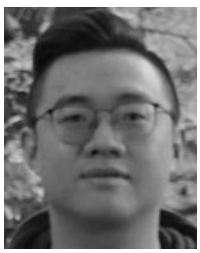

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