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Compact Modeling of IGBT Charging/Discharging for Accurate Switching Prediction

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ABSTRACT The trench-type IGBT is one of the major devices developed for very high-voltage applications, and has been widely used for the motor control of EVs as well as for power-supply systems. In the reported investigation, the accurate prediction of the power dissipation of IGBT circuits has been analyzed. The main focus is given on the carrier dynamics within the IGBTs during the switching-off phase. It is demonstrated that discharging and charging at the IGBT's gate-bottom-overlap region, where electron discharging is followed by hole charging, has an important influence on the switching performance. In particular, the comparison of long-base and short-base IGBTs reveals, that a quicker formation of the neutral region within the resistive base region, as occurring in the long-base IGBT, leads to lower gate-bottom-overlap capacitance, thus realizing faster electron discharging and hole charging of this overlap region.

INDEX TERMS IGBT, switching characteristics, potential distribution, overlap capacitance, charging/discharging, compact model, power loss.

I. INTRODUCTION

The demand for high-voltage devices is expanding in various applications, which leads to an urgent request for improved stability and predictive capability of the related circuit-simulation tasks, to enable the movement towards highly accurate design capability. A prerequisite to fulfill above requirements is the development of accurate compact power-device models, for realizing accurate simulation of circuits with any power-device type and thus helping to expand the application fields of these power devices. Here, we focus on the IGBT device, for which high-voltage operation even up to 10kV has been verified through the usage of advanced materials [1]–[7]. Since the IGBT structure can realize low on-resistance and fast switching at the same time, it is widely utilized in the active-core part of circuits, such as power-converter circuits for motor control of electrical vehicles [8]–[12].

The IGBT is internally a combination of a MOSFET and a bipolar transistor (BJT), as shown in Fig. 1, aiming at the realization of fast switching similar to MOSFETs and in addition low on-resistance similar to bipolar transistors [1]. Further, the highly resistive base region can sustain extremely high applied voltages. There are several compact models developed previously by different research groups, where the modeling focuses mainly on the functionally-active intrinsic part of the IGBT [13]–[17]. The IGBT modeling causes often numerical instabilities during circuit simulation, resulting from steep local-electric-field increases, which occur during switching predominantly within the base region. Therefore, instead of a compact-modeling approach in a closed physical-structure-related mathematical form, a macroscopic-modeling approach, using sub-circuits of basic standard models provided by the circuit simulator, is often applied for simplification [18]. However, the accuracy of the IGBT-switching waveforms, obtained with the previously reported compact IGBT models, is still not sufficient for predicting the switching losses of circuits with the required precision. These accuracy deficiencies become

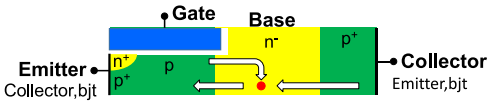

FIGURE 1. Studied IGBT structure with indicated current flows.

particularly large for recently developed improvements of the basic IGBT structure [19], [20].

In an IGBT, the gate of the MOSFET part controls the base-current supply of the bipolar part. For modeling the IGBT performance accurately, it has thus been demonstrated that both MOSFET and bipolar contributions must be accurately modeled on the basis of their physical origins. It has further been shown that the potential within the base region contributes in two different ways [17]. On one hand, it strongly controls the MOSFET features and on the other hand, an accurate base-region-potential distribution is also essential for correct reproduction of the bipolar features. Therefore, our previously developed compact IGBT model solves this key potential within the base region iteratively, to achieve the highest possible accuracy [15], [17]. It is our purpose in this investigation, to analyze the origin of the IGBT-specific features of the switching characteristics in more detail. Our findings are then applied for further IGBT-model improvements to achieve highly-accurate prediction of the switching losses [21], [22]. The main focus in the developed approach is given on the induced carrier dynamics during switching. It is demonstrated that the IGBT-switching features are, in particular for modern trench-type IGBT structures, determined to a large extent by both the electron and the hole dynamics within the gate-overlap region, which is modeled by considering the related capacitive charging and discharging delay.

For our investigation 2D numerical device simulations are studied [23]. Further, measurements are also analyzed to verify the developed model accuracy. Since the 2D numerical simulation provides microscopic insight of the carrier dynamics within the IGBT, thus enabling an understanding of the physics behind these IGBT features, the origin of the measured phenomena can be clarified at the same time. In the reported study we mainly analyze the switching-off condition. The reason is that the switching-on condition includes large contributions from the free-wheeling diode included in the circuit, so that the switching-off condition better reveals in rather pure form the carrier dynamics within the IGBT.

II. IGBT-SWITCHING FEATURES

The trench-type IGBT structures, studied with a 2D-device simulator, are depicted in Fig. 2 [24], [25]. The left side of Fig. 3 shows the simulated results for the switching performance with the long-base IGBT of the test circuit on the right side. Calculation results with the compact model HiSIM_IGBT [26] are also depicted together in Fig. 3. Some clear deviations from 2D-device simulation results are observed in the compact model results. Especially, the

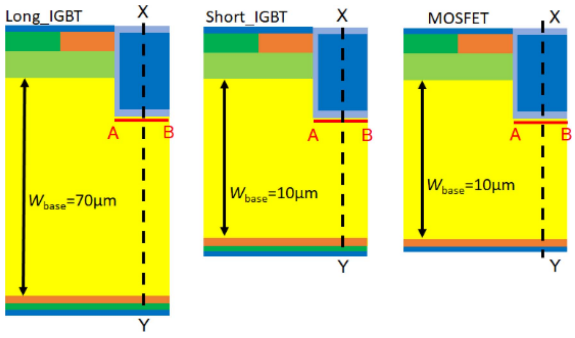

FIGURE 2. IGBT structures with nMOSFET + pnp BJT part (left side and middle) and nMOSFET-only structure (right side), which are studied in this report. The X-Y line is through the middle of the bottom-gate oxide and the A-B line is directly underneath the bottom-gate oxide.

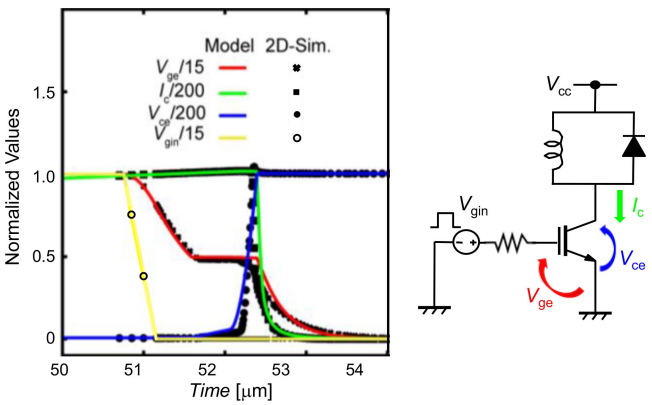

FIGURE 3. 2D-device-simulation and HiSIM-IGBT1 results of the switching-off characteristics for the long IGBT shown in Fig. 1. The circuit applied for the simulation is depicted on the right side.

reduction of the effective gate-emitter voltage V_{ge} after the plateau is not well reproduced. Since the V_{ge}-switching characteristic determines the whole IGBT characteristics such as the switching power loss, accurate prediction of the V_{ge}-switching waveform is of high importance. To study the origin of the observed deviations, the IGBT characteristics are investigated for two different base lengths, 70μm (long IGBT) and 10μm (short IGBT), as can be seen in Fig. 2. A MOSFET structure with the same resistive drift length of 10μm as the short IGBT is studied in addition. The only difference between these two structures is that a p+ implantation is included at the collector side of the short IGBT, while this implantation is excluded in the MOSFET. Namely, the former device operates under the ambipolar condition while the latter device operates under the unipolar condition. Base-, collector- and channel-impurity concentrations are set to $N_{\text{base}} = 2\text{x}10^{15}\text{cm}^{-3}$, $N_{\text{collector}} = 1\text{x}10^{18}\text{cm}^{-3}$ and $N_{\text{channel}} = 1\text{x}10^{17}\text{cm}^{-3}$, respectively, for long IGBT and short IGBT. The MOSFET's impurity concentrations (except for the deleted collector) are the same as in the IGBT structures.

Figure 4 shows the switching-off performance, obtained by the 2D-device simulation for the three studied devices

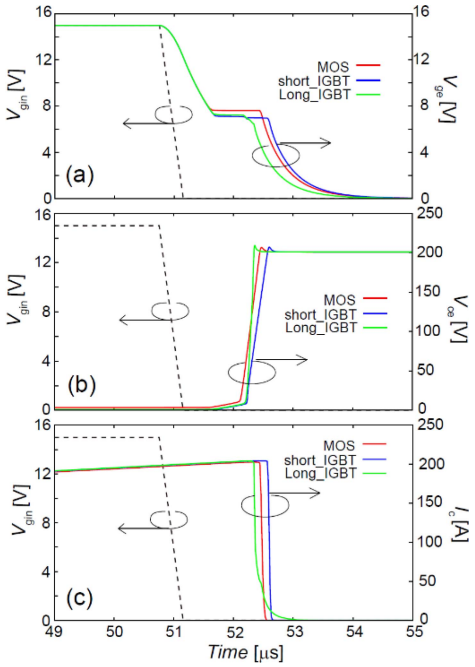

FIGURE 4. 2D-device-simulation results for the switching-off waveforms of the 3 device structures (nMOSFET, short IGBT, long IGBT), depicted in Fig. 2. Subfigures (a), (b) and (c), correspond to V_{ge}, V_{ce} and I_c, respectively.

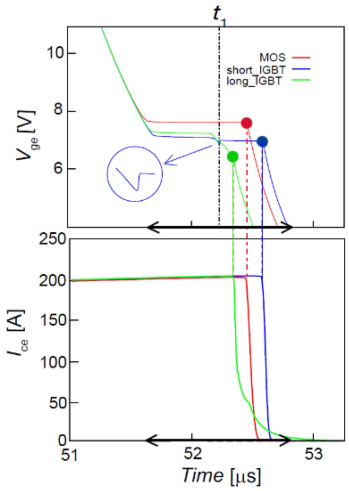

FIGURE 5. Enlarged 2D-device-simulation results of the V_{ge} plateau and of the corresponding collector current I_{ce}, observed in Fig. 4.

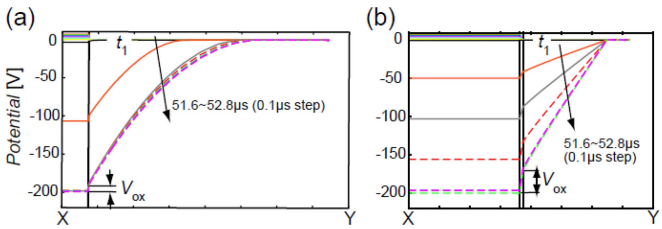

FIGURE 6. 2D-device simulation results of the potential distribution along the X-Y direction (see Fig. 2) of the devices, (a) for the long IGBT and (b) for the short IGBT at $V_{ce} = 200V$.

of Fig. 2. The reduction of the internal potential V_{ge} starts when the input voltage V_{gin} is turned off, but it can be seen that the V_{ge} turn-off is drastically delayed. The V_{ge} response delay is an RC delay, where "R" is the gate resistance and "C" is the gate capacitance. The clear plateau in the V_{ge} waveform, called a Miller plateau, is caused by the discharging of the gate-overlap charge [27]. Here, long and short IGBTs show clear differences in the plateau characteristics. However, short IGBT and MOSFET characteristics of the Miller plateau are quite similar, namely, similar length with quite a high degree of flatness, i.e., a very small gradual reduction, is observed for V_{ge}. Figure 5 shows the zoomed characteristics of the V_{ge} plateau, observed in Fig. 4, and the corresponding collector current I_{ce}. It can be seen that the short IGBT has a longer plateau than the long IGBT. On the other hand, a clear small pit is observed in the V_{ge} waveform of the short IGBT at time $t = t_1$. This time "t_1", indicated in Figs. 5, further corresponds closely to the starting time of the final tailed V_{ge} reduction of the long IGBT. On the contrary, such behavior is not observable for the MOSFET, showing no pit and a smaller gradual reduction. The starting times of the final tailed V_{ge} and of the I_{ce} reduction are closely correlated for all device structures. Thus, the filled circles in Fig. 5 indicate the time conditions for the finished overlap-capacitance discharge and for the start of the remaining base-carriers disappearance at the electrodes. In spite of the increased length of the long IGBT, sustaining higher biases applied between emitter and collector, the final switching-off phase starts earlier than for the other shorter devices.

III. DYNAMICAL CARRIER DISTRIBUTION IN IGBT

When switching-off V_{gin} (see Fig. 4), a depletion layer is formed underneath the bottom-gate oxide immediately. Fig. 6 plots the potential-distribution change along the X-Y line, defined in Fig. 2, during the switching-off time from $t = 51.6\mu s$ to $52.8\mu s$, as indicated by arrows on the time axis in Fig. 5. For the long IGBT, the potential-distribution change occurs quite abruptly when $t > t_1$, and the depletion extension within the base follows the theoretical prediction when assuming complete carrier depletion, i.e., that no carriers exist [28], [29]. On the other hand, it takes much longer until the distribution approaches its final form for the short IGBT, and the distribution itself is approximating a linear function, due to the narrow space for the depletion extension, as verified in Fig. 6(b). Fig. 7 shows the hole and electron distributions along the X-Y line for both long and short IGBTs. It is seen how both holes and electrons start to disappear for $t > t_1$.

Fig. 8 compares the charge-density distributions of long and short IGBT at the gate bottom along the A-B line, about 1nm below the gate oxide (see Fig. 2). Here, rapid electron-density reduction is observed for $t > t_1$, similar to the observation along the X-Y line in Fig. 7. However, a hole-density increase occurs for $t > t_1$ at this gate-bottom surface. The increased hole density becomes even a factor

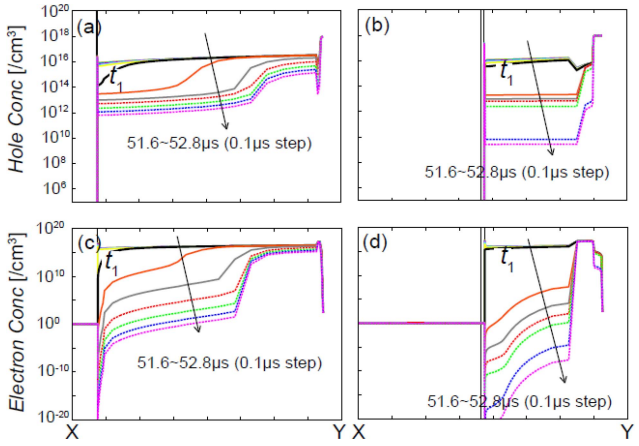

FIGURE 7. 2D-device simulation results of hole- and electron-density distributions during switching-off along the X-Y direction (see Fig. 2) for the long IGBT (left) and the short IGBT (right).

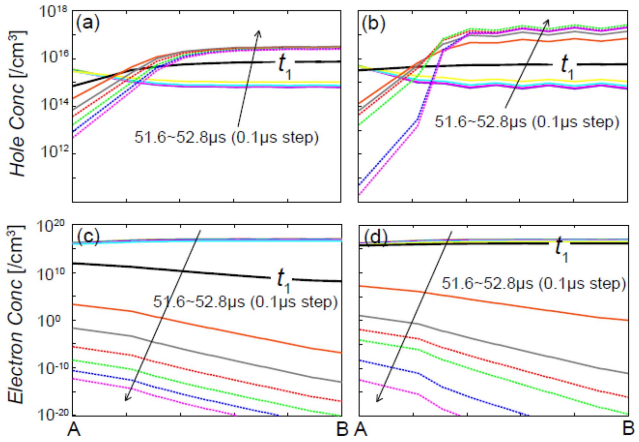

FIGURE 8. 2D-device simulation results of hole and electron density distributions during switching-off along the A-B direction (see Fig. 2) for the long IGBT (left) and the short IGBT (right).

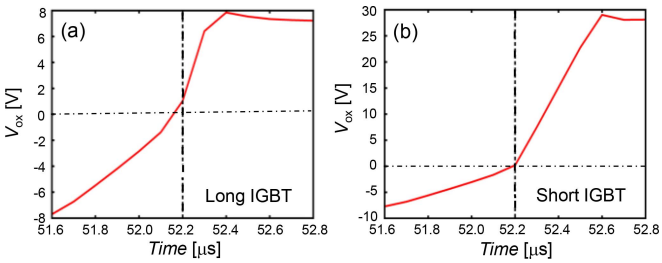

FIGURE 9. 2D-device-simulation results of the potential drop within the gate bottom oxide (a) for the long IGBT and (b) for the short IGBT during the switching-off as shown in Fig. 5.

10 higher than the impurity concentration in the case of the short IGBT. The potential drop within the bottom-gate oxide V_{ox} is depicted in Fig. 9 for both IGBTs. It is obvious that the short IGBT experiences a larger potential drop V_{ox}, because of the higher field induced by the large V_{ce} within the shorter base region (see Fig. 6b). It is also seen that the sign of the potential drop changes so that a crossing of zero, referring

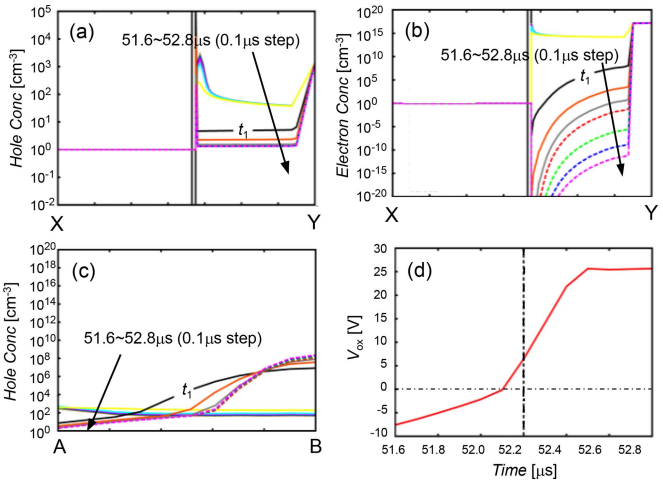

FIGURE 10. Carrier distributions for the studied MOSFET along the X-Y direction (a) for holes and (b) for electrons. Hole concentration along the A-B direction is depicted in (c). (d) shows the potential drop within the gate-bottom oxide.

the flat-band condition, occurs. The time $t = t_1$ gives approximately the condition when both the discharging of electrons and also the hole charging are starting at the bottom-overlap region. The necessary high hole-density storage leads to a relatively long time until the required total amount of holes is collected. The involved switch from electron depletion to hole storage at the bottom of the overlap region is the reason for the observed pit and the inclined reduction start in the plateau region for the V_{ge} switching-off waveforms of short- and long IGBT, respectively. Fig. 8 shows furthermore a rapid reduction of the electron density, namely, the fact that the region near to the gate-oxide corner is rapidly depleted. In case of the long IGBT, the stored hole density becomes nearly constant for $t > t_1$. Thus, a reduction of the total overlap charge is observed for the long IGBT. This can be modeled as a reduction of the effective overlap length. On the contrary, a further density increase is observed for the short IGBT, which requires more time until the overlap charge reaches the saturation value, resulting in a constant V_{ge} for a longer time.

2D-device simulation results of the carrier densities for the studied MOSFET are depicted in Fig. 10, where hole storage at the surface of the bottom-gate-overlap region is observed, even though the amount is quite small. Since no hole injection is possible in unipolar MOSFETs within a certain time interval, the excess-hole density remains very small. Though hole storage does practically not occur for the MOSFET, the field induced within the bottom-gate oxide is as high as that for the short IGBT, as can be seen in Fig. 10d (compare with Fig. 9b).

From above analysis, it can be concluded that the different V_{ge}-plateau characteristics, observed in Fig. 5, are due to the different carrier-movement characteristics under the gate-bottom oxide, which are dependent on the specific device construction. Ambipolar transistors show two independent

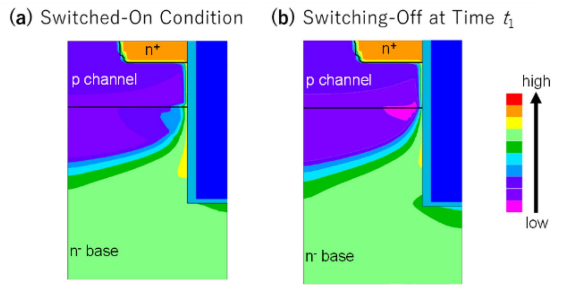

FIGURE 11. 2D-device simulation results for the electron-density distribution in the long IGBT near the gate and the overlap region, (a) under the switched-on condition and (b) during switching-off at time $t = t_1$.

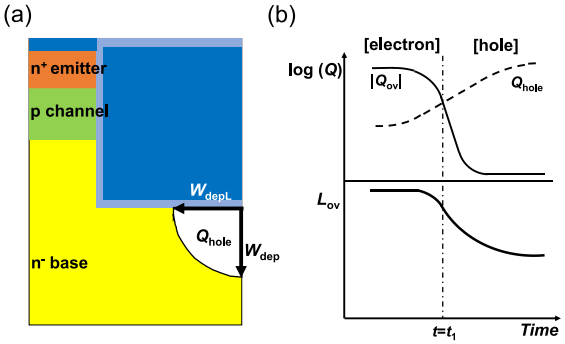

FIGURE 12. Schematics of (a) depletion extension at the gate-bottom-overlap region during switching-off, and (b) charge densities gathered (upper part) and modified effective-overlap length (lower part).

step-like processes, namely, the electron discharging starts to occur first and is then accompanied by the hole charging. On the other hand, the MOSFET is a unipolar device, and thus the electron discharging is the main origin for V_{ox} while the hole storage requires time. This small amount of the hole storage balances the total system at the gate-bottom oxide. The reason for the second inclined reduction of V_{ge} in the long IGBT, different from the flat V_{ge} in the short IGBT, is due to the gradual hole storage required for balancing the system. The build-up of the hole storage requires time due to the long base length. No quick hole storage is possible due to the remaining neutral region within the base (see Fig. 7a). As the result, the hole charging at the bottom-gate oxide is delayed.

IV. COMPACT MODELING OF BOTTOM-OVERLAP CHARGE

Fig. 11 shows 2D-device simulation results of the two-dimensional electron-density distribution around the gate-overlap region for the long IGBT. Fig. 11a depicts the distribution result during the switched-on condition, while Fig. 11b depicts the distribution result at the $t = t_1$ time condition. Electrons are disappearing during the switching-off process from the bottom-edge point B shown in Fig. 2, and holes are gathering from the same place, as schematically shown in Fig. 12a. Thus, both electron and hole dynamics must be modeled together. During the on-state, high densities of both electrons and holes exist in the base, because of the high-injection condition of the device. During the switching-off process, a part of the excess holes moves towards the bottom of the overlap region to form an inversion condition, especially for the short IGBT. Therefore, the total overlap charge Q_{over} at the gate bottom consists of two terms

$$Q_{over} = Q_{ov} + Q_{hole} \tag{1}$$

where Q_{ov} is the accumulated electron charge, including that during depletion, and Q_{hole} describes the hole charge. Q_{ov} and Q_{hole} are written in the form

$$Q_{ov} = W_{eff} \cdot L_{ov} \cdot Q_{ov,dep} \tag{2}$$

$$Q_{hole} = \alpha \cdot q \cdot W_{eff} \cdot W_{depL} \cdot W_{dep} \cdot N_{over} \tag{3}$$

Here, N_{over} is the impurity concentration within the overlap region. The unit charge is denoted by q and the bottom-overlap charge $Q_{ov,dep}$ can be written as

$$Q_{ov,dep} = C_{ox}\left(V_G - \phi_{S,ov}\right) \tag{4}$$

$$V_G = -V_{gs} + V_{fb} \tag{5}$$

where C_{ox} is the oxide capacitance. The surface potential $f_{S,ov}$ is the solution of the Poisson equation at the gate-bottom oxide along the overlap region [30]. The depletion width W_{dep} in the vertical direction is further written as a function of $f_{S,ov}$ as

$$W_{dep} = \sqrt{\frac{2\varepsilon_{si} \cdot \left(-\phi_{S,ov}\right)}{q \cdot N_{over}}} \tag{6}$$

Under the depletion condition, the total charge density is small in comparison to the inversion as well as the accumulation condition. Therefore, the gate-bottom part in depletion condition is excluded from the overlap length as

$$L_{ov} = L_{ovB} - W_{depL} \tag{7}$$

The depletion-width extension, induced along the gate-overlap edge W_{depL}, is assumed to be equal to that at the overlap region vertical to the gate oxide W_{dep} for simplified compact-modeling purposes, as depicted in Fig. 12a. The length L_{ovB} is that of the gate-bottom length A-B (see Fig. 2). The relationships between the charge densities and the overlap length are depicted schematically in Fig. 12b. Modeling concepts for the overlap charge along the channel direction can be found in literature [31].

Since we solve the Poisson equation explicitly within the overlap region, the Q_{over} equation is valid for any bias condition, including the depletion, accumulation, and even the inversion condition. For the hole charge Q_{hole}, the impurity concentration N_{over} is simply applied with a model parameter a, instead of a treatment as the inversion charge. The reason is that the hole movement is influenced by the resistance within the base, which would require additional modeling concepts. The developed model for the gate-bottom-overlap region is implemented into HiSIM_IGBT by considering the time constant τ of the carrier-transit delay, being required to

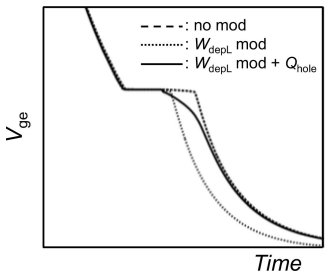

FIGURE 13. Simulation result with the developed model for the gate-bottom-overlap region. Comparison is done for simulation conditions with inclusion of different model parts.

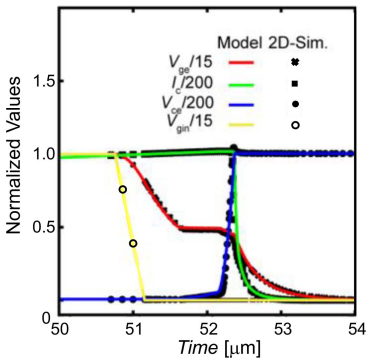

FIGURE 14. Transient-simulation results of HiSIM_IGBT with the developed model in comparison to the 2D-device simulation results.

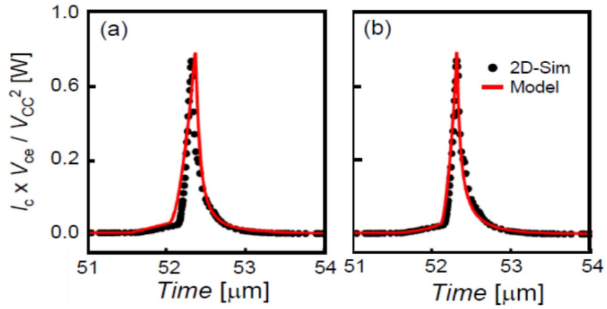

FIGURE 15. Comparison of calculated switching loss with HiSIM_IGBT to 2D-device simulation results (a) without and (b) with the developed model.

form the charges of Q_{ovB} as well as Q_{over}. This is accompanied by the modeling of the W_{dep} as well as W_{depL} delay as [32], [33]

$$W_{\mathrm{depL,nqs}}(t_i) = W_{\mathrm{depL,nqs}}(t_{i-1}) + W_{\mathrm{depL,nqs}}(t_{i-1})\frac{\Delta t}{\Delta t+\tau} \times \left(W_{\mathrm{depL,qs}}(V(t_i)) - W_{\mathrm{depL,nqs}}(t_{i-1})\right) \quad (8)$$

A simulation result with the developed model for the gate-bottom-overlap region is depicted in Fig. 13, showing also the influence of the different modeled phenomena.

V. MODEL VERIFICATION AND DISCUSSION

Switching characteristics calculated with HiSIM_IGBT, including the developed gate-bottom-overlap-region model,

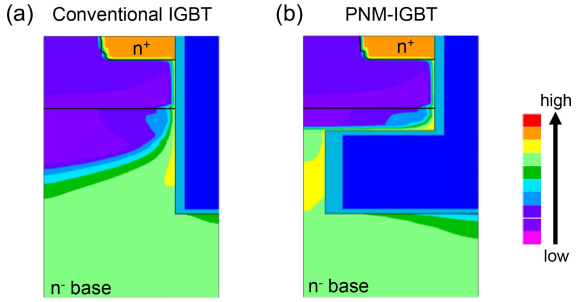

FIGURE 16. 2D-device-simulation results of the electron distribution under the switched-on condition, (a) for the more conventional trench-type IGBT, and (b) for the Partially-Narrow-Mesa (PNM) IGBT.

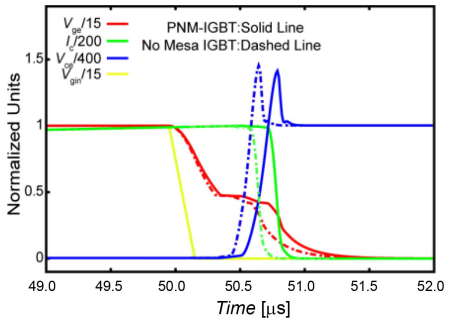

FIGURE 17. 2D-device-simulation results of the switching-off characteristics for the PNM-IGBT in comparison to the conventional trench IGBT.

is compared to 2D-device-simulation results in Fig. 14 for the long IGBT. The comparison is the same as shown in Fig. 3 with HiSIM_IGBT, where the developed gate-bottom-overlap-region model is not included. Calculated switching losses are compared in Fig. 15 for both cases without and with the developed model. The much better agreement with the implemented gate-bottom-overlap-region model verifies that the transient V_{ge} characteristics is strongly influenced by the carrier dynamics at the surface of the bottom-gate oxide. During the electron depletion, holes are gathered. This gathering process is controlled by the potential distribution between the gate V_{ge} and that in the base along the gate-oxide bottom. Therefore, the key to model the switching performance more accurately, is an accurate solution for the potential distribution within the device.

To verify the applicability of the developed model, a specific modified IGBT structure, developed to improve the driving capability, which is called Partially-Narrow-Mesa IGBT (PNM-IGBT) [34], [35], is investigated. The specific feature of this PNM-IGBT is a longer extended bottom-gate length, as shown in Fig. 16b, which enhances the switching-characteristics impact coming from the gate-overlap region at the trench bottom. As can be seen, the electron depletion starts to occur from the bottom-edge point B in the same way as for the more conventional trench-IGBT structure. The switching-off characteristics of the PNM-IGBT are compared with those of the conventional trench-IGBT in Fig. 17. All device parameters are kept the same for the

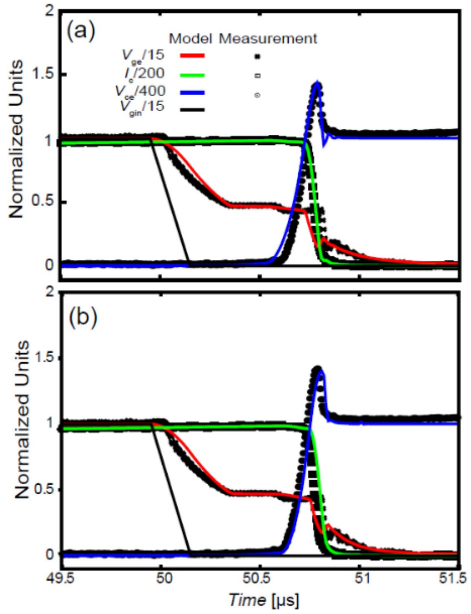

FIGURE 18. Calculated switching-off characteristics of the PNM-IGBT with HiSIM_IGBT in comparison to the measurement results (a) without (b) with the developed gate-bottom-overlap-region model. The resulting switching-loss error is improved from 19.6% in (a) to 6.2% in (b).

both cases, with the exception of the gate-bottom length. This difference between the two IGBT structures leads to a much longer V_{ge} plateau continuation for the case of the PNM-IGBT. It can be seen, that this extended V_{ge} plateau is accompanied by a slower response of the internal node potential V_{ce}. The reason being that the depletion extension as well as the hole storage take both a longer time to complete for the PNM-IGBT case. Fig. 18 compares the model-calculation results for the switching-off characteristics to the measurement results. The accuracy of the calculated switching loss is improved from 19.6% to 6.2% due to the increased accuracy for the modeling of the V_{ge}-plateau characteristics.

VI. CONCLUSION

The IGBT performance is determined by the dynamics of the two carrier types, namely those of electrons and holes, leading to an improvement of the IGBT-switching characteristics in comparison to MOSFETs. It is demonstrated that the V_{ge} characteristics, observed during switching-off, is strongly affected by both, the electron and the hole dynamics at the gate-bottom oxide. The specific switching features are dependent on the details of the device geometry, which determines the potential distribution within the resistive drift region. The dynamics of electron and hole movements determines characteristics of this potential distribution. Thus, the charge densities of electrons and holes must be modeled by the potential distribution within the device. The investigated short IGBT collects a very large number of holes at the bottom of the gate oxide during the switching-off process, which induces an experimentally observed V_{ge}-plateau extension. On the other hand, the longer base length in the long IGBT prevents an excessive hole collection at the bottom-gate surface by forming a neutral region, resulting in the shortening of the V_{ge} plateau, i.e., in a smaller capacitance which has to be charged during the switching-off process.

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