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# Modeling of RRAM With Embedded Tunneling Barrier and Its Application in Logic in Memory

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**ABSTRACT** This paper proposes a modeling technique for the evaluation of RRAM with embedded tunneling barrier that serves as an embedded selector, enabling high density integration while reducing the leakage current in a memory array. The further exploration of various biasing and pulsing schemes is provided so as to optimize programming efficiency for logic-in-memory application.

**INDEX TERMS** Resistive random access memory (RRAM), compact model, selectorless RRAM, logic in memory.

## I. INTRODUCTION

Along with the exponential technological growth in semiconductor industry over the past decades, resistive random access memory (RRAM), one of the most promising emerging memory options, has advanced in its capacity. RRAM has demonstrated its advantages in high speed of operation, simple device structures, great power efficiency, low energy consumption, and long retention time. It is well-studied that the switching mechanism of binary metal-oxide RRAM between the low-resistance state (LRS) and the high-resistance state (HRS) is generally considered as the formation and rupture of conductive filaments (CF), which consist of oxygen vacancies (Vo), in the high-k dielectric material stack between the top electrode and bottom electrode [1], as illustrated in Fig. 1.

Due to the increasing demand for the deployment of artificial intelligence (AI), the technical requirements of memory have become more stringent. For example, the traditional Von Neumann architecture has come to its physical limitation because of the data transfer bandwidth between the memory unit and arithmetic unit. The concept of computing in memory is proposed to overcome this kind of issue. The emerging memories with bi-stable switching condition are rather suitable for this application. RRAM with the aforementioned advantages has been studied for neuromorphic computing application [2]–[4]. However, current RRAM technology still has its limits. Compared with human brain, in terms of neuron number (100 billion neurons), synapse number (100 trillion) and power consumption (sub 10 pJ), artificial neuron chips that had been proposed are still not able to compete with the work of our mother nature [5]. To reach high density of artificial synapses, an RRAM device with an embedded selector (or selectorless RRAM), as opposed to a separate selector and an RRAM device, is needed.

Each of the electronic neurons should be integrated with more synapses in order to increase the compatibility for emerging applications, such as edge computing. The traditional “one transistor one resistor (1T1R)” scheme has low energy consumption as a result of low leakage current. It can also reach multi-level switching by controlling the gate voltage of the transistor. In comparison, “one selector one resistor (1S1R)” scheme is capable of higher integration level with reasonably suppressed leakage current. When the tunneling barrier is integrated with the high-k dielectric stack, it serves as an embedded selector (Fig. 1), enabling high density integration while reducing the leakage current in a memory array for in-memory computing. A modeling technique for evaluating RRAM with tunneling barrier will be demonstrated in detail in the subsequent section.

Criteria of selector devices for emerging memory devices include high on-off ratio (rectification ratio or nonlinearity

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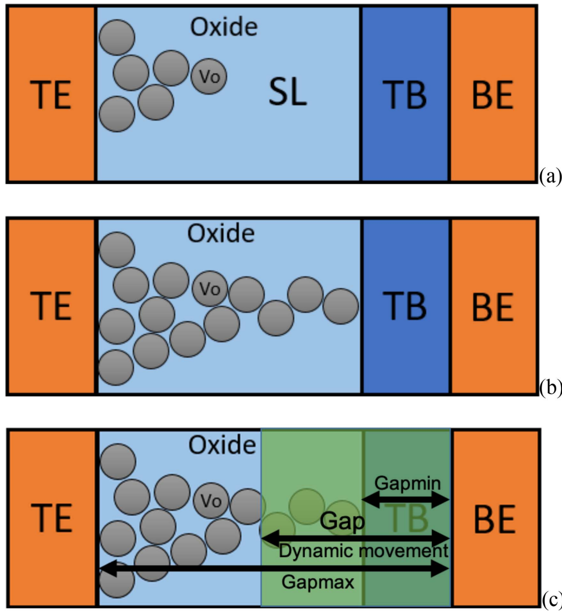


**FIGURE 1. Schematics of RRAM with embedded tunneling barrier in different states. The whole device consists of top electrode (TE), bottom electrode (BE), switching layer (SL) and tunneling barrier (TB). (a) The device under voltage stress can start the filament formation process. (b) The tunneling barrier blocks the ion migration process and suppress the leakage current when the device is in stand-by condition. (c) The dynamic tunneling gap due to the change of the filament accounts for a large part of output current characteristics.**

ratio), minimized threshold voltage, sufficiently high on-current for memory operation, scalability, robust endurance, fast switching speed, and operation polarity comparable with memory elements [6]. Selector devices for high density applications, relying on tunneling mechanism, can meet the aforementioned requirements, as reported in [7].

The functions of the selector based on embedded tunneling barrier can be delivered by energy band engineering with properly chosen thickness of barrier oxide (e.g., $TaO_x$, $TiO_x$, and $AlO_x$) and electrode work function (e.g., TiN), As the electric field increases, the highly field-dependent Fowler-Nordheim tunneling mechanism becomes predominant at high voltage level. When the device starts to form filament, the actual gap that is the tunneling distance starts to decrease until being restricted by the barrier layer. At low voltage level, the electrons are able to tunnel through the thin barrier layer after set operation [8], [9]. For the barrier layer thinner than 5nm, the direct tunneling effect is the main transport mechanism [10]. For the switching layer thicker than 20nm, the usual mechanisms could be identified as Pool-Frenkel effect or Schottky emission, commonly seen in oxide leakage current or in selector devices [11], [12].

## II. MODELING METHODOLOGY

To assess the switching mechanism of the RRAM cell with an embedded tunneling barrier, the compact model is built by SPICE compatible language Verilog-AMS [13] which is widely used for simulating analog behaviors of semiconductor devices. The model modules are mainly composed of current calculation module, gap formation module, and temperature calculation module.

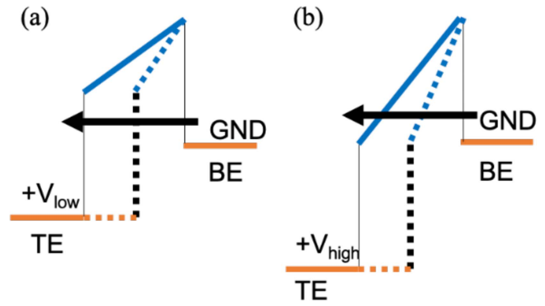


**FIGURE 2. Schematic of the nonlinear resistive switching characteristic contributed by tunneling mechanism. Transport in MIM tunneling device is dominated by (a) direct tunneling at low voltage and (b) Fowler-Nordheim tunneling at high voltage. The dashed line represents the change of tunneling gap after set operation.**

### A. CURRENT CALCULATION

Traditionally the ionic current is calculated by the following equation:

$$J_{drift} = N \times q \times \mathrm{v} \tag{1}$$

where $N$ is the number of ionic charges per unit volume that contributes to the drift current, $q$ is the electron charge, and $v$ is the drift velocity as follows:

$$v = afexp\left(\frac{-Ea}{KT}\right)sinh\left(\frac{qaE}{2KT}\right) \tag{2}$$

where $a$ is the oxide lattice constant of the material, $\underline{Ea}$ is the activation energy, $K$ is the Boltzmann constant, $T$ is the temperature and $E$ is the electric field.

In this compact model, tunneling mechanism is used in the current calculation module. At low fields, the direct tunneling (DT) limits the output current of RRAM in LRS. When it comes to high field, the Fowler-Nordheim tunneling (FNT) becomes the predominant output current. Thus, the tunneling barrier creates the high selectivity of RRAM devices. The tunneling current can be expressed as follows:

$$J = \frac{q^2}{8\pi h\varphi}E^2 exp\left(\frac{-8\pi\sqrt{2m^* q\varphi^3}}{3hE}\right) \tag{3}$$

and

$$J = \frac{q^2}{8\pi h\varphi}E^2 exp\left(\frac{-8\pi\sqrt{2m^* q\varphi^3}}{3hE}\left(1-\left(1-\frac{d}{\varphi}E\right)^{\frac{3}{2}}\right)\right) \tag{4}$$

where $h$ is the Plank constant, $\varphi$ is the band offset between electrode and tunneling oxide, $d$ is the direct tunneling distance, $m^*$ is the effective mass, and $E$ is the electric field across the tunneling gap. The tunneling current (3) and (4) are lumped into:

$$J = AE^2 exp(-B/E) \tag{5}$$

and

$$J = AE^2 exp(-BD/E) \tag{6}$$

where $A$ and $B$ represent $\frac{q^2}{8\pi h\varphi}$ and $\frac{8\pi\sqrt{2m^*q\varphi^3}}{3h}$, respectively, which can be extracted from experiment data, and $D$ is the correction term $(1 - \left(1 - \frac{d}{\varphi}E\right)^{\frac{3}{2}})$ for direct tunneling. And then the total current is calculated by multiplying J and the filament contact area.

### B. GAP FORMATION

The tunneling gap changes with the filament growth (or rupture) until it is stopped by TB. The gap ranges from (SL + TB) to only TB, and they are defined as Gapmax and Gapmin, respectively, as indicated in Fig. 1(c). The gap formation occurs when the oxygen vacancies start to generate. It could quickly form a leakage path. The time and the thermal related positive feedback behavior are expressed as [14]

$$\frac{dg}{dt} = v_0 exp\left(\frac{-U_a}{kT}\right) sinh\left(\frac{qa\gamma E}{kT}\right) \tag{7}$$

where $g$ is the gap between electrode and filament, $Ua$ is the activation energy, $a$ is the oxide lattice constant, $v_0$ and $\gamma$ are fitting parameters, and $E$ is the electric field across the oxide.

### C. TEMPERATURE CALCULATION

The evolution of gap would increase the current and the temperature due to Joule heating. Then the increased temperature would accelerate the gap formation. A compact temperature calculation model helps the evaluation of this thermal runaway process. The temperature in the active region ($T_{RRAM}$) is evaluated with Joule heating ($W_j$) and thermal dissipation ($W_d$) [17], [18] as

$$T_{RRAM} = \int_{t0}^{t1} \frac{W_j - W_d}{CV} dt \tag{8}$$

where $C$ is the heat capacity of the material and $V$ is the volume of the device. The Joule heating in the device is from the product of the two-terminal current ($I_{pn}$) and voltage ($V_{pn}$) as follows:

$$W_j = I_{pn} V_{pn} \tag{9}$$

and the general expression for heat ($Q$) dissipation is evaluated as [19], [20]

$$W_d = \frac{\partial Q}{\partial t} = -k\nabla T \tag{10}$$

where $k$ is the heat transfer coefficient.

In a simplified 1D case, the heat dissipation path is modeled along the two terminals of the device, so the temperature of RRAM can be calculated as

$$T_{RRAM} = \frac{d_{hd} W_j}{kA}\left(1 - exp\left(\frac{-kA}{d_{hd}CV}t\right)\right) + T_{room} \tag{11}$$

where $d_{hd}$ is heat dissipation distance of RRAM, $T_{room}$ is the room temperature, $C$ is the heat capacity of the material

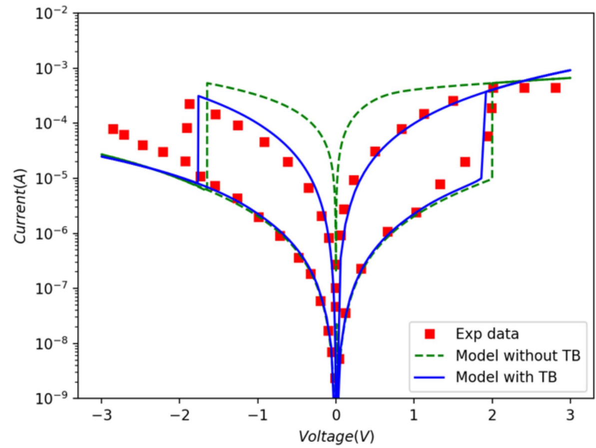


**FIGURE 3. Simulated I-V characteristics of RRAM with tunneling barrier (TB) under quasi-DC condition with ramp rate at 1V/s. The red dots are extracted from the 3nm device of [7]. The green line is the simulated result without TB based on our previous study [17]. The current level difference in low bias regime is clearly shown here, illustrating the supressed current from the TB as an embedded selector.**

and $V$ is the volume of the heated device. Due to the simplification of 1D thermal dissipation, the parameter $A$ which is the area of the conductive filament is used for correction. The time constant associated with the thermal capacitance of the device is expressed as

$$\tau = RC = \frac{d_{hd}CV}{kA}. \tag{12}$$

For memory array application, the high-density design is preferred. When the device is under biased condition, Joule heating effect raises the temperature not only within the device itself but also in the surrounding materials. Studies show that the increase of the local temperature may also affect the neighbor cells. This is known as the thermal cross talk issue [15] that is not included in this work. For instance, when the neural network accelerator is under supervised learning, it should go through a huge amount of weight updates. Under this condition, the accumulated heating effect influences the resistance level since the ionic movement could be affected by the temperature as well [16]. Therefore, both the thermal effects in the device and the surrounding materials need to be evaluated as a whole. Including such a phenomenon is worth an extended study based on the thermal effect of the single device with modified and coupled boundary conditions for large scale simulation.

## III. SIMULATION RESULTS AND DISCUSSION

Using the model discussed above, the simulated I-V characteristics of the RRAM cell with an embedded tunneling barrier is shown in Fig. 3 where the case without the embedded barrier is included for comparison.

### A. VARIATIONAL STUDY

The resistance variation as a significant drawback that hinders RRAM from applications in industry and mass production needs to be investigated thoroughly. Because the

**TABLE 1. Model card of the simulated RRAM.**

| Parameter description | Symbol | Value (nm) |
|---|---|---|
| Initial temperature of environment | $T_0$ | 300 K |
| Activation energy | $U_a$ | 0.5 eV |
| Lattice constant | $A$ | $0.25 \times 10^{-9}$ m |
| Escape attempt velocity | $v_0$ | 0.1 m/s |
| Local enhancement factor | $\gamma$ | 10 |
| Heated volume of RRAM | *Volume* | $10^{-24}$ m$^3$ |
| Filament contact area | *F_cr* | $2.5 \times 10^{-17}$ m$^2$ |
| Heat dissipation distance of filament | *dr_T* | $12 \times 10^{-9}$ m |
| Minimum thickness of tunneling gap | *Gapmin* | $2 \times 10^{-9}$ m |
| Maximum thickness of tunneling gap | *Gapmax* | $12 \times 10^{-9}$ m |

resistance switching phenomenon is dominated by the change of CF, its physical dimension would directly affect the resistance distribution of every RRAM resistance state. The variation could be caused by either the stochastic nature of filament geometry [18] or the process induced variation in ALD deposited high-k dielectric stacks like $HfO_2$ [21]–[23]. Considering the FNT and DT transport mechanisms of the device, the variations of filament length formation and tunneling barrier thickness would vary the electric field across the barrier and output current. In order to study the variations of the RRAM resistance states, the aforementioned tunneling barrier variation of an embedded selector is translated into *Gapmin* and *Gapmax* variation by using Monte Carlo simulation in HSPICE [24]. The simulation results show that the thickness variation of the tunneling barrier would affect the read margin and the write margin, as shown in Fig. 4. Other variations of the devices switching parameters could be set up empirically by tuning the model card provided in Table 1.

### B. PULSING SCHEME OF RRAM OPERATION IN VARIATION

Various pulsing schemes are evaluated for RRAM operation while considering variations. By considering the worst case scenario, the write error under a designated operation scheme could be predicted. The power consumption that leads to over set/reset condition could be reduced as well. As one of the emerging memories, its performance metrics are not well defined as commercial memory devices yet, but there are still some technology assumptions for MOS-accessed and cross-point emerging NVM [23], which are of interest to evaluate our desired performance metrics. For the consistent comparison of pulsing scheme, we obtained some technology assumption such as pulse width and Set/Reset voltage listed in Table 2.

As shown in Fig. 5, three types of pulsing condition—PWL pulse (PP), triangular pulse (TP) and dynamic pulse (DP) – are tested for the write performance evaluation. In the case of PP with 50ns pulse width, most of cases with gap thickness variation could be properly switched. In many of the cases, however, the over set condition wastes a lot of energy.

The triangular pulses consume less energy due to less thermal loss. But in most cases, the devices cannot properly switch to LRS. The dynamic pulse treatment obtained from

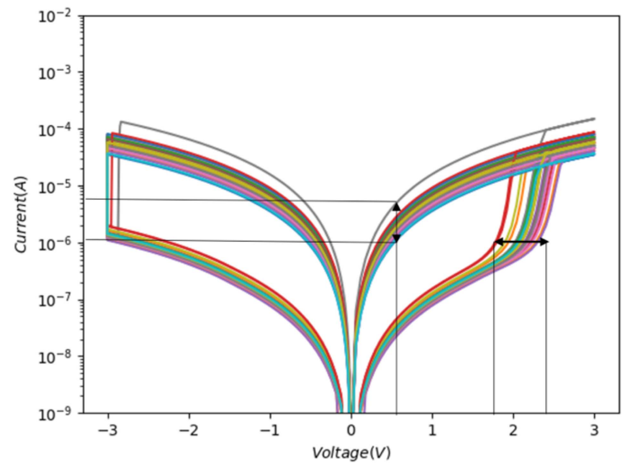


**FIGURE 4. Simulated I-V variation characteristics with the change of model parameter *Gapmin* and *Gapmax* that represent the actual tunneling distance of electrons in the selectorless device. Each of the switching layer and barrier layer is set up with 1nm variation that would be induced during thin film deposition process [21]–[23] for 3 standard deviations using Monte Carlo simulation. As a result, the switching-on point in set operation varies between 1.8V and 2.4V while the read current could change as much as more than half an order of magnitude.**

**TABLE 2. RRAM technology assumptions [23].**

| | Value |
|---|---|
| Cell size | $4F^2$ |
| Set/Reset voltage | 2/-2V |
| Read voltage | 0.5V |
| Conditional voltage | 1.5V |
| Write pulse duration | 50ns/pulse |
| Rise/Fall time | 10ns |
| HRS resistance | 500k ohm |
| LRS resistance | 10k ohm |
| Half-select resistance | 100k ohm |
| Write endurance | $10^{12}$ |

flash memory programming technique [25] shows a better result for reducing the energy consumption while suppressing the write error (half switched) condition. The switching condition could be overserved by the gap transition. Then the write operation window could be determined by modulating the steps of the dynamic pulse.

## IV. APPLICATION FOR NON-VON-NEUMANN MACHINE

### A. LOGIC IN MEMORY (LIM)

The highly scalability of two-terminal RRAM crossbar shows its advantage as storage class memory and provides opportunities for non-von-neumann machine operating concept like computing in memory. Here, we evaluate the novel operating scheme – logic in memory – proposed by Borghetti *et al.* [26]. By utilizing the state switching characteristics of memristive devices, the logic operation called material implication (IMP) can further perform the NAND gate operation by a three-step sequence [26]. Table 3 shows the truth table of IMP. Since the NAND gate is a common logic gate, the application of IMP can be used to realize various ultra-high-density logic gates while reducing the

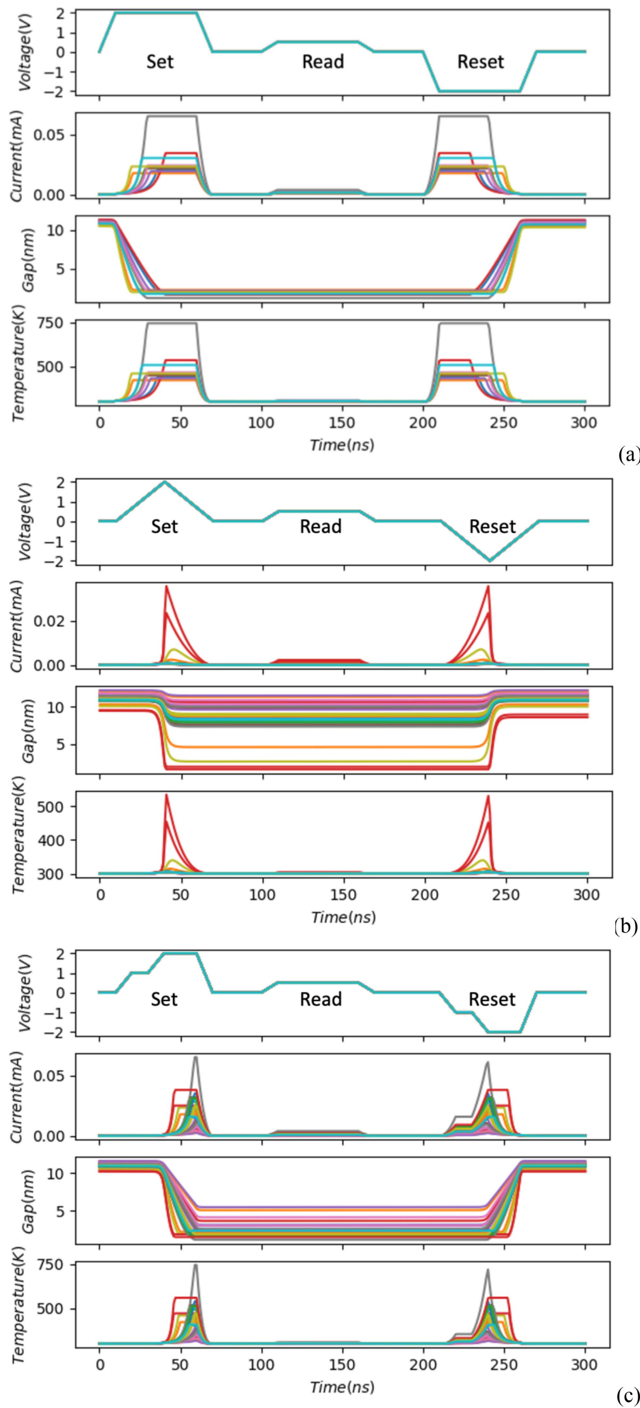


**FIGURE 5.** The dynamic behaviors of current, gap and temperature in transient simulation under (a) PWL pulse (b) triangular pulse and (c) dynamic pulse indicate that the pulsing scheme could largely impact on device characteristics during fast switching operation.

data transfer cost which is one of the major issues existing in state-of-the-art hardware when dealing with machine learning.

The analysis of IMP operation is conducted by a three-step sequence, as shown in Fig. 6. Both of the devices are in HRS in the beginning. The first pulse is for the initial condition set up for $R_p$ based on Table 3. If the initial condition of $R_p$ needs to be in state 1, the Set $R_p$ operation is applied, otherwise only read voltage is applied on both devices. For the operation 0 IMP 1 $\rightarrow$ 1, $R_p$ is initially at state 0. The second pulse $V_{set}$ applies IMP to $R_q$ and $V_{con}$ to $R_{p,}$ respectively. The current output of $I_{set}$.

Clearly shows that $R_q$ is now switched from state 0 to state 1. Finally, the third pulse reads the state of $R_q$ demonstrating the 0 IMP 1 $\rightarrow$ 1 logic. On the other hand, the operation of 1 IMP 0 $\rightarrow$ 0 (Fig. 6(c)) needs the resistor $R_g$ that serves as the voltage divider. When $R_p$ is at LRS after initial condition set up, it would short out the voltage $V_{con}$. As a consequence, the voltage drop across the $R_g$ would reduce the voltage across $R_q$ and the state of $R_q$ would be left unchanged. The final read-out value of $R_q$ is at 0 state (HRS).

**TABLE 3.** Truth table of material implication (IMP) [26].

| In p | In q | Out q' |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**TABLE 4.** Power consumptions of IMP.

| | Conditional voltage (V) | Power consumption (W) |
|---|---|---|
| Dynamic pulse | 1.5 | 6.4626μ |
| | 1 | 2.3083μ |
| PWL pulse | 1.5 | 6.7838μ |
| | 1 | 4.1740μ |

### B. ENERGY CONSUMPTION OPTIMIZATION FOR LIM OPERATION

Based on the technology assumptions in Table 2, this section discusses the optimization of the three-step operation because such a novel operation would benefit from the pulsing scheme design mentioned in Section III-B. The simulated results are shown in Fig 7.

In order to ensure the successful switching condition and the relevant operation window, operation schemes of PP and DP are compared here as well. Since the write error of TP is higher than those of the other two schemes, it is less preferred to be used for the discussion in this section. The RRAM devices in LIM cell operating in dynamic pulsing scheme consume less energy during the whole IMP operation, which is shown in Table 4. Meanwhile, the RRAM devices could still stay in relatively stable switching condition, as discussed in Section III-B. Thus, better power consumption, which is crucial for the neuromorphic application in large scale cell array, of the cell circuit could be expected.

Although the DP scheme is beneficial to energy consumption, the variation in LRS could be observed from the distribution of Gap in Fig. 5. This phenomenon could further lead to an error in LIM. In order to examine the distribution of resistance state after DP scheme, Monte Carlo simulation following the same parameters of simulated cases in Fig. 4

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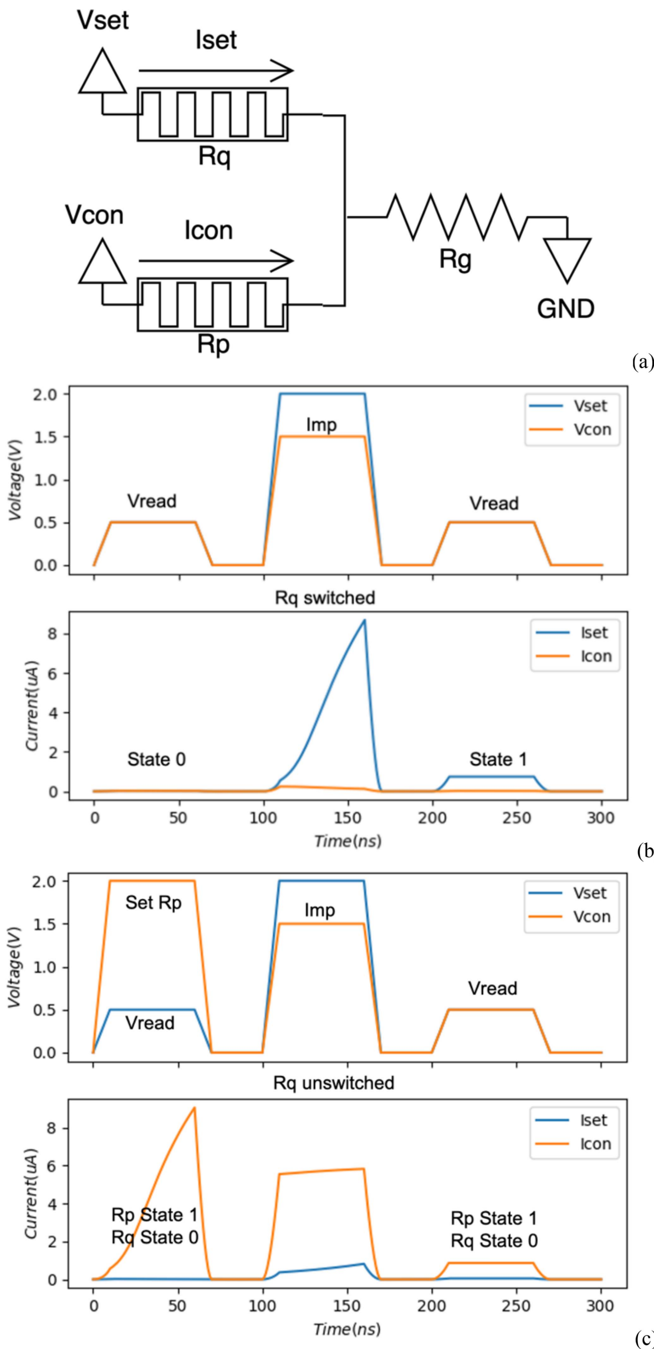


**FIGURE 6.** **(a) Circuit diagram of IMP (b) The operation of 0 IMP 1 → 1. (c) The operation of 1 IMP 0 → 0. The $I_{set}$ represents the output of $R_q$ and the $I_{con}$ represents $R_p$. Note that $R_{HRS} > R_g > R_{LRS}$. The operation follows the technology assumptions in Table 2 as well. The choice of $R_g$ value falls in between $R_{HRS}$ and $R_{LRS}$ in order to let the IMP work properly. Here, the $R_g$ is set to 50k-ohm for the following discussion.**

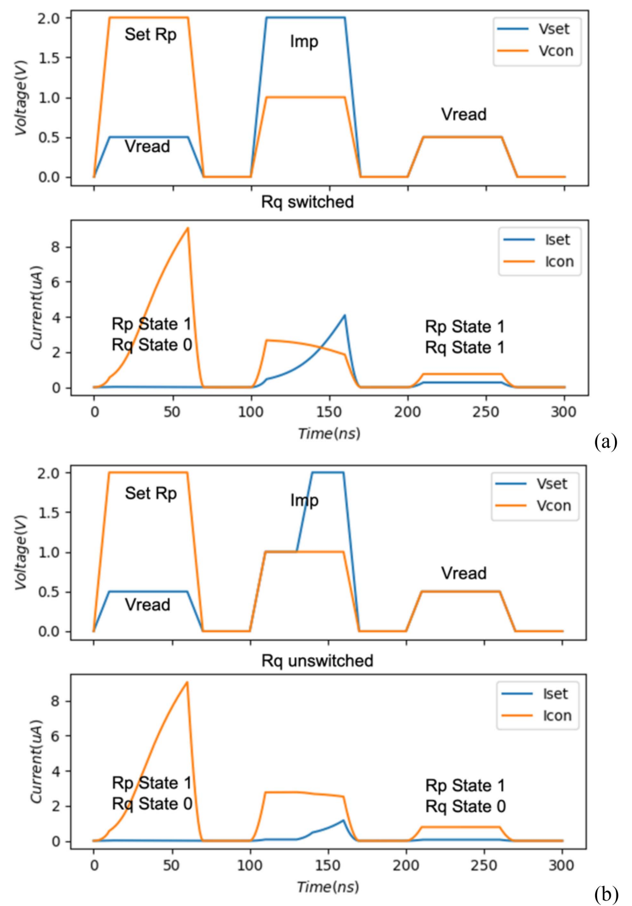


**FIGURE 7.** **The operation of 1 IMP 0 → 0. Pulsing scheme is tested (a) at lower $V_{con}$ (compared with Fig 6(c)) and (b) in dynamic $V_{set}$ conditions. Although (a) shows lower power consumption than that in Fig. 6(c), the final read-out level is higher than expected, implying the unstable state for the following sequential logic operation. By using the scheme in (b), better power consumption could be achieved while maintaining operation stability.**

and Fig. 5 was conducted. By observing the LRS distribution level, the different device stack and process induced variations could be evaluated case by case. From the technology assumption in Table 2, the defined LRS resistance and half-select resistance are set up as the margin to judge whether the device is properly switched. The distributed LRS readout current should be at least higher than the half-select resistance level with the applied read voltage. In Fig. 8(a), the second step in DP is one-fourth of the pulse width in PP case, and only two out of thirty cases pass the margin. On the other hand, when the step width shown in Fig. 8(b) is increased to three times the case in Fig. 8(a), only two out of thirty cases do not meet the requirement, that could be translated to a yield rate of 93.3%. Thus, if one wishes to further optimize the yield rate and energy efficiency, the DP step pulse width could be considered as a design parameter for the given technology node.

## V. CONCLUSION

A modeling technique for evaluating RRAM with an embedded tunneling barrier was presented in this paper. The tunneling barrier serves as an embedded selector, enabling high density selectorless RRAM integration. Owing to the stochastic nature of RRAM, its stability suffers from distributed read/write characteristics. Thus, various biasing and pulsing schemes for better programming efficiency were

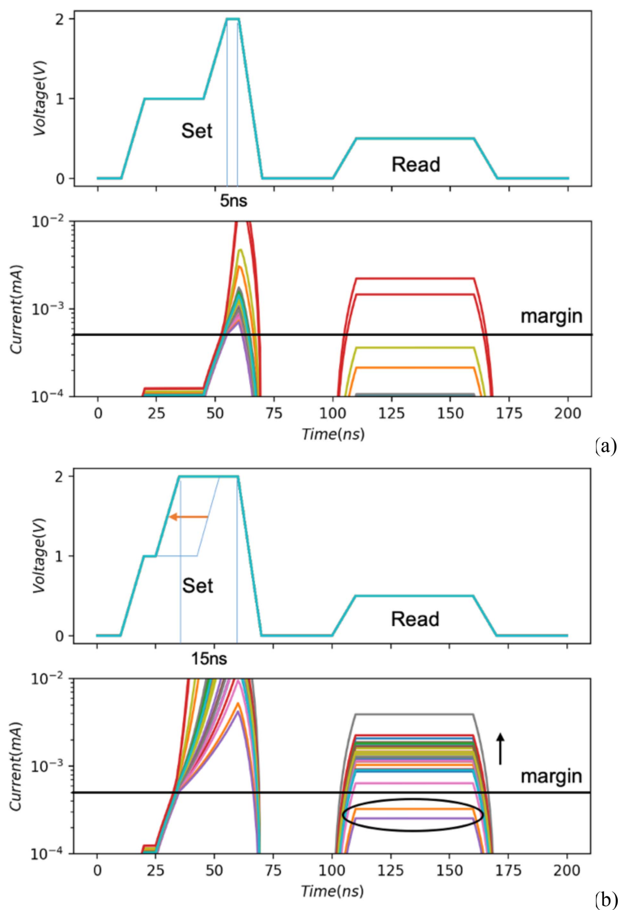


**FIGURE 8.** **The shift of the second step in DP would also vary the programmed device characteristics. Within the margin of the half-select resistance, the DP step may shift during the pulse width of PP scheme. The current level is zoomed into the order of $10^{-2}$ and $10^{-4}$ mA due to the assumption that the read current at half-selected resistance should fall at $5x10^{-4}$ mA according to Table 2.**

demonstrated by using the proposed model. While the high biasing voltage is usually needed to avoid non-fully set condition for conventional RRAM, the proposed novel operation scheme under specified technology node for the selectorless RRAM at a lower voltage and a dynamic programming condition could be used for the reduction of energy consumption. As a promising candidate for in-memory computing application, the evaluation of the proposed scheme applied to LIM was demonstrated as well.

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