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Channel Length Optimization for Planar LDMOS Field-Effect Transistors for Low-Voltage Power Applications

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ABSTRACT We identify an optimum channel length for planar Laterally Diffused Metal-Oxide-Semiconductor (LDMOS) field-effect transistors, in terms of the specific on-resistance, through systematic device simulation and optimization. We simulate LDMOS devices with different channel lengths ranging from 100 nm to 10 nm, modifying the length of the drift region and doping concentration of the body region to match a pre-determined leakage current suitable for low-voltage power applications (3.3V and 5V). For devices with a channel length exceeding 40 nm, reducing the channel length decreases the on-resistance as expected. Below 40 nm, an increase in resistance is observed as the result of an increased body doping concentration leading to significant electron mobility degradation in the channel area.

INDEX TERMS Automatic optimization, on-resistance, power LDMOS, RESURF, scaling limits.

I. INTRODUCTION

Laterally diffused metal-oxide semiconductor (LDMOS) field-effect transistors (FETs) are commonly used for low-voltage ($<$ 30 V) [1]–[4], mid-voltage (30 V – 100 V) [5]–[7], and high-voltage ($>$ 100 V) [8, 9] power applications. Many novel LDMOS device technologies with different device configurations have been proposed recently to achieve a better figure-of-merit ($FOM = BV^2/R_{on}$), i.e., a high breakdown voltage (BV) with a low on-resistance (R_{on}), for different practical voltage ranges [10]–[14]. However, complex device structures are often introduced in these proposed technologies which make the industrial fabrication process very difficult and costly. Furthermore, even though device miniaturization is crucial for all voltage ranges, in the past few decades, most studies have been done on large LDMOS devices for mid-voltage and high-voltage applications [15]–[27]. And unfortunately, a thorough study on scaling of the planar LDMOS technology, limited to a straightforward planar device design, has not yet been performed.

In this paper, we analyze how the LDMOS on-resistance depends on channel length, investigating channel lengths ranging from 100 nm down to 10 nm. We conduct our systematic investigation through an automated simulation procedure and the drift-diffusion model as implemented in a commercial technology computer-aided design (TCAD) package [28]. We find an optimum channel length, revealing a fundamental scaling limit for LDMOS technology.

II. DEVICE STRUCTURE AND SIMULATION SETUP

In Fig. 1, we show the general cross-section of the LDMOS under study, with doping profiles indicated. The LDMOS structure has a uniform p-type background. Gaussian doping profiles are considered for all other regions: source, drain, p-body, drift, and the lightly-doped n-well (LDW). The p-body is a p-type Gaussian profile which controls the barrier height in the off-state, and thus the drain-to-source subthreshold leakage current (I_{leak}). The drift region is a shallower n-type Gaussian implant which improves the drain-to-source breakdown voltage (BV_{DSS}) by diminishing

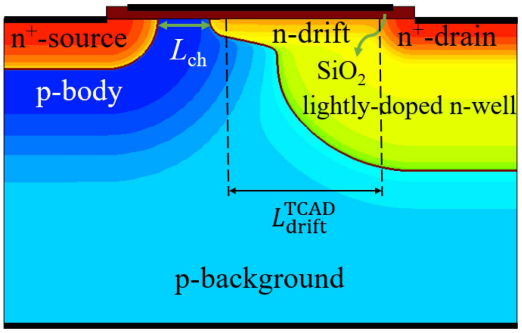

FIGURE 1. Cross section of the simulated n-channel LDMOS. The color scale represent the n-type (red) and p-type (blue) doping density, showing the idealized Gaussian doping profiles.

the electric field peaks at the p-n junctions, based on the RESURF principle [29]. The drift length ($L_{\text{drift}}^{\text{TCAD}}$) is the simulation parameter (TCAD input) that determines the drift region as indicated in Fig. 1. Note that the drift doping extends a little further than $L_{\text{drift}}^{\text{TCAD}}$ because of the roll-off of the Gaussian profile. The LDW acts as an extension of the drain region, providing a more gradual doping gradient from the heavily n-type doped drain to the p-background, preventing a sharp electric field at the p-n junction and resulting in a higher breakdown voltage [30].

The channel length (L_{ch}) is defined as the distance between the p-n metallurgical junctions of the p-body/n-drift and the n^+-source/p-body, measured at the surface of the semiconductor under the gate oxide. In our device optimization, L_{ch} is controlled by the drift region length, i.e., a longer drift region results in a shorter channel length. The total device length is scaled in conjunction with the changing channel length to investigate only the influence of the channel length on on-resistance, excluding the effects of other parts of the device.

We use a commercial drift-diffusion based device simulation tool [28] to model the LDMOS devices and study the electrical characteristics of the devices through solving the Poisson and drift-diffusion equations self-consistently. To account correctly for device characteristics, we consider the effects of impact ionization using the van Overstraeten avalanche model [31], a doping dependent and transverse-field dependent mobility model [32], [33] and the doping-dependent Shockley–Read–Hall (SRH) generation–recombination model.

To compare devices with different channel lengths fairly, we target a leakage current (I_{leak}) of 10^{-13} A/μm for all configurations. To this end, we develop an optimizing computer code which iteratively calls the drift-diffusion simulation package and updates the device structure. The algorithm automatically determines the best values for the $L_{\text{drift}}^{\text{TCAD}}$ and the p-body doping concentration (N_{body}) in order to reach the intended L_{ch} and I_{leak}.

For each optimized device, the specific on-resistance, R_{SP}(on), and the breakdown voltage, BV_{DSS}, are extracted. R_{SP}(on) is the on-resistance, R(on), normalized to the total

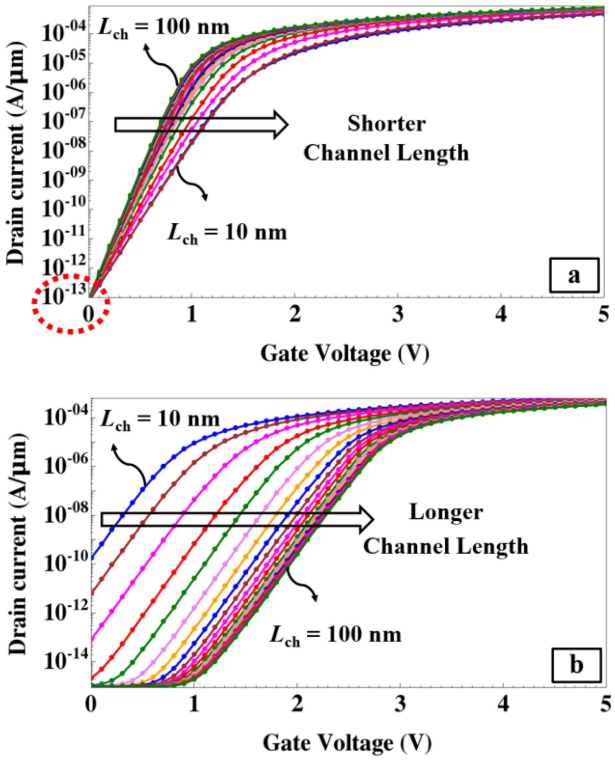

FIGURE 2. Transfer characteristics ($I_{\text{DS}} - V_{\text{GS}}$) of 5V LDMOS devices. (a) All devices have a fixed leakage current, 10^{-13} A/μm, fixed by the optimization algorithm. I_{leak} is extracted at $V_{\text{GS}} = 0$ V and $V_{\text{DS}} = 5$ V. (b) $I_{\text{DS}} - V_{\text{GS}}$ for devices before applying optimization algorithm. Shorter channel length devices have higher leakage current because of the lower electrostatic control along the channel.

layout area, and is extracted for $V_{\text{GS}} = 5$ V and $V_{\text{DS}} = 0.1$ V. We also calculate drift resistance (R_{drift}) and channel resistance (R_{ch}) to investigate the impact of the drift and channel regions on R(on) separately. R_{drift} can be extracted by plotting $V_{\text{DS}}/I_{\text{DS}}$ versus $1/(V_{\text{GS}} - V_{\text{th}})$ and extrapolating to $1/(V_{\text{GS}} - V_{\text{th}}) = 0$ [34], while $R_{\text{ch}} = R(\text{on}) - R_{\text{drift}}$.

III. RESULTS

We first demonstrate the necessity of our optimization procedure in Fig. 2 (a), showing the transfer characteristic of 5V LDMOS devices ($t_{\text{ox}} = 12$ nm) with channel lengths varying from 10 nm to 100 nm. The current-voltage characteristics of devices are calculated with the optimization algorithm. All devices have been optimized to $I_{\text{leak}} = 10^{-13}$ A/μm $\pm$ 10^{-15} A/μm while $BV_{\text{DSS}} \geq 10$ V. $L_{\text{drift}}^{\text{TCAD}}$ and N_{body} are updated in each simulation to attain a particular L_{ch} and $I_{\text{leak}} = 10^{-13}$ A/μm $\pm$ 10^{-15} A/μm. Note that, while the I_{leak} target has been met for all channel lengths, the threshold voltage increases for decreasing channel lengths due to subthreshold slope degradation. To determine the correct N_{body} and $L_{\text{drift}}^{\text{TCAD}}$, about 1,000 simulations are automatically performed for each channel length.

In Fig. 2 (b), we plot current-voltage behavior of the devices with different channel lengths without applying our optimization procedure while keeping the p-doping constant.

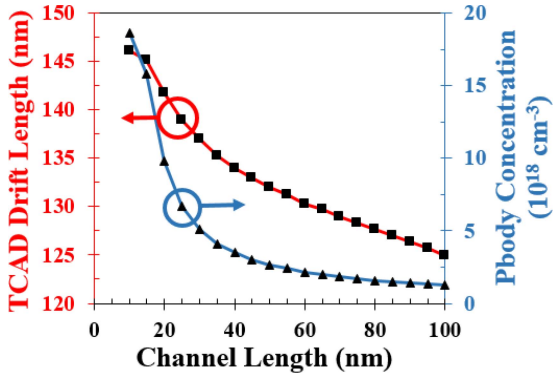

FIGURE 3. Calculated TCAD drift length and p-body doping concentration by the optimization algorithm for different channel lengths.

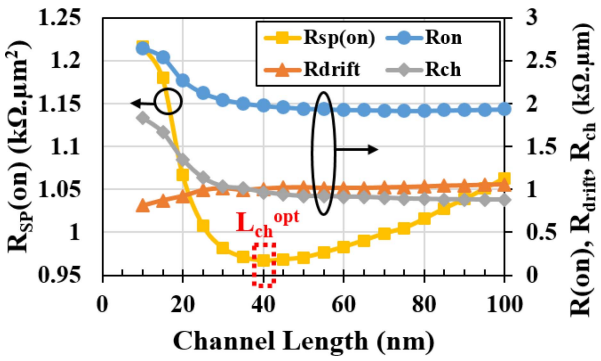

FIGURE 4. R_{SP}(on), R(on), R_{drift}, and R_{ch} for 5V LDMOS devices with different channel lengths revealing $L_{ch}^{opt} = 40$ nm. A tradeoff between the reduction in channel length and the accompanying in electron mobility degradation results in an optimum value.

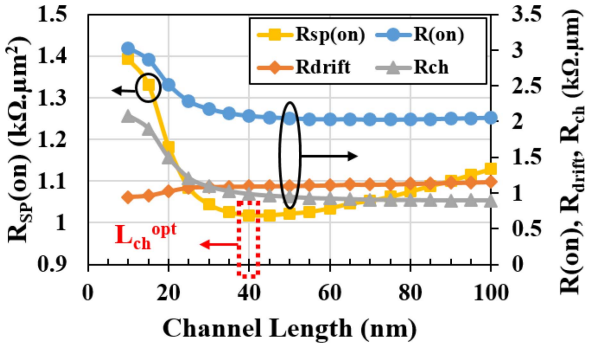

FIGURE 5. R_{SP}(on), R(on), R_{drift}, and R_{ch} for 3.3-V devices with different channel lengths ($V_{GS} = 3.3$ V and $V_{DS} = 0.1$ V). Similar to 5V LDMOS devices, optimum channel length is 40 nm.

The drain-to-source leakage current is critically determined by the electrostatic control over the channel. Indeed, devices with shorter channel lengths have lower threshold voltage which gives rise to a higher leakage current. In short channel devices, the drift region is closer to the source. As a result, the p-body region is depleted more and the effective barrier decreases. Therefore, more carriers are able to overcome the barrier and leakage current increases.

Fig. 3 shows the calculated L_{drift}^{TCAD} and N_{body} for the optimized devices with different channel lengths. Fig. 3 reveals that a longer drift region is needed to have a shorter channel-length device that maintains the target breakdown behavior. On the other hand, a higher doped p-body region is required for devices with a shorter channel length to maintain the leakage current criterion, $I_{leak} = 10^{-13}$ A/μm. Because the depletion region occupies more of the channel region for shorter channel length devices, the p-body doping concentration needs to be increased to reduce the depletion width. In addition, the loss of electrostatic control along the channel for shorter channel length devices is compensated by increasing the doping in the p-body region.

To determine the device performance, we extract the dependence of R_{SP}(on), R(on), R_{drift}, and R_{ch} on the channel length for 5V LDMOS devices, as shown in Fig. 4. The interplay of reducing the channel length and increasing the doping concentration yields an optimum value for the channel length, $L_{ch}^{opt} = 40$ nm, for which the specific on-resistance is minimized. Decreasing the channel length of a FET generally decreases the on-resistance. However, a higher p-body doping is required for shorter channel length devices which, in turn, increases the impurity scattering in the channel. More scattering degrades the electron mobility along the channel and results in a higher on-resistance. This is confirmed by inspecting the channel resistance (R_{ch}), shown in Fig. 4, for decreasing channel length, which shows that the increase in total resistance is caused by the increase in the channel resistance. Note that, for shorter channel lengths, the drift resistance (R_{drift}) reduces slightly because the net doping in the drift region is increased by increasing the TCAD drift length.

With the same optimization algorithm, R_{SP}(on), R(on), R_{drift}, and R_{ch} are calculated for 3.3V LDMOS devices ($t_{ox} = 8$ nm) and plotted in Fig. 5. Interestingly, the optimum channel length for 3.3V LDMOS devices is similar to 5V LDMOS devices, at 40 nm. Analogous to 5V devices, the increase in R_{ch} for shorter channel lengths, due to the higher doped p-body regions and lower electron mobility, increases the R(on) and consequently, makes the optimum channel for 3.3V LDMOS devices.

IV. DISCUSSION

To further confirm that mobility degradation is the cause of the degradation at $L_{ch} < 40$ nm, we plot the average electron mobility in the channel area, as well as the threshold-voltage for different channel length devices in Fig. 5. Here, we clearly see that the electron mobility decreases rapidly for channel lengths below the optimal L_{ch}^{opt}. As the concentration of ionized dopants (p-body) increases, impurity scattering increases, reducing the mobility and decreasing the current passing through the channel. Lower current causes higher on-resistance for shorter channel length. Additionally, Fig. 6 shows the threshold voltage. As seen before in Fig. 2, the threshold increases for shorter channel lengths due to an increase in channel doping concentration. However, the

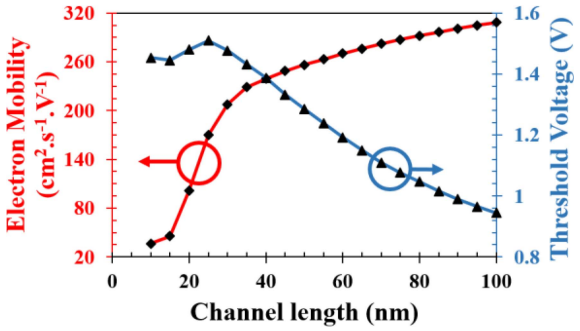

FIGURE 6. Electron mobility and threshold voltage for 5V LDMOS devices. Threshold voltage is extracted at $I_{DS} = 10^{-7}$ A/μm and $V_{DS} = 0.1$ V. Higher channel doping, for shorter channel lengths, results in a higher impurity scattering and threshold voltage.

sub-threshold shift is minimal below L_{ch}^{opt} pointing to mobility degradation as the main cause of the increase in R(on).

The drift doping-concentration ($N_{drift} = 5 \times 10^{18}$ cm^{-3}) and drift depth ($D_{drift} = 25$ nm) also affect the depletion region and can influence the electron mobility in the p-body region. However, the general behavior of R_{sp} with channel-length scaling is independent of these parameters. Changing N_{drift} to 3×10^{18} cm^{-3} and 7×10^{18} cm^{-3}, we obtain optimal channel lengths of 35 nm and 45 nm, respectively, while increasing D_{drift} to 40 nm yields an optimum channel length of 50 nm. Indeed, performing a study of a combined drift depth/concentration variation reveals a landscape of optimum channel lengths with the same overall scaling behavior.

In a practical application, LDMOS transistors are often incorporated into a CMOS technology thanks to the Si-compatibility of LDMOS. As a result, LDMOS process parameters, such as doping profiles, cannot easily be adjusted independent of the other CMOS transistors, as we do in this study. However, in our study, we identified that the existence of an optimal channel length is due to a reduced electron mobility caused by an increased channel doping, needed to control the off-state current of short channels. This fundamental mechanism will be present in all LDMOS with a scaled channel length, regardless of the precise doping profile limitations.

The optimum channel length of 40 nm we find for planar LDMOS is somewhat longer than that found in conventional planar CMOS, where devices are found to maintain good performance down to approximately 32 nm [35], [36]. Here, we provide a few important differences between the channel scaling of power LDMOS and CMOS. The first major difference is that the absolute requirement in leakage current in power transistors is more stringent compared to CMOS technology. An I_{off} specification of 10^{-10} A/μm is in place for CMOS technology [37] whereas we used 10^{-13} A/μm in LDMOS devices for power applications. Second, in CMOS, the operating voltage is reduced with node scaling, which helps to control source-to-drain leakage current. Whereas, in power applications, the LDMOS drain voltage rating has to align to application requirements such as battery voltage and inductive switch-node ringing.

Moreover, the breakdown is generally not considered in nanoscale CMOS. In addition, some important planar enhancement technologies such as strained silicon and high-k metal gates were not taken into consideration in our simulation to maintain a straightforward comparison. Overall, a longer channel length is required for planar LDMOS transistors to simultaneously meet leakage current, breakdown voltage, and on-resistance requirements. The differences in LDMOS and CMOS scaling, necessitate a separate study on the channel length scaling of power LDMOS, as presented in this paper.

V. CONCLUSION

We have presented 5V and 3.3V LDMOS devices which are able to satisfy the optimization criteria $I_{leak} \leq 10^{-13}$ A/μm and $BV_{DSS} \geq 10$ V for devices with channel lengths down to 10 nm. The channel length influence on specific on-resistance was investigated by an automated computer code, iteratively calling a drift-diffusion simulation package. Interestingly, we found that there is an optimum channel length value $L_{ch}^{opt} = 40$ nm, that minimizes the specific on-resistance for the both 5V and 3.3V optimized LDMOS devices, i.e., the on-resistance increases by decreasing the channel length for devices with channel lengths shorter than $L_{ch}^{opt} = 40$ nm, which proves to be a scaling limit for planar LDMOS devices.

REFERENCES

[1] J. Ha, H. Kang, K. Baek, and J. Lee, "Enhancement of device performance in LDMOSFET by using dual-work-function-gate technique," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 848–850, Jul. 2010, doi: 10.1109/LED.2010.2051134.

[2] S. Liu *et al.*, "A review on hot-carrier-induced degradation of lateral DMOS transistor," *IEEE Trans. Device Mater. Rel.*, vol. 18, no. 2, pp. 298–312, Jun. 2018, doi: 10.1109/TDMR.2018.2833490.

[3] T. Efland, C. Tsai, and S. Pendharkar, "Lateral thinking about power devices (LDMOS)," in *Int. Electron Devices Meeting Tech. Dig. (IEDM)*, San Francisco, CA, USA, 1998, pp. 679–682, doi: 10.1109/IEDM.1998.746447.

[4] G. Wang *et al.*, "Investigation on LDMOS characteristics of layout dependence in FinFET technology," in *Proc. China Semicond. Technol. Int. Conf. (CSTIC)*, Shanghai, China, Jul. 2019, pp. 1–3, doi: 10.1109/CSTIC.2019.8755646.

[5] W. Ge *et al.*, "Ultra-low on-resistance LDMOS with multi-plane electron accumulation layers," *IEEE Electron Device Lett.*, vol. 38, no. 7, pp. 910–913, Jul. 2017, doi: 10.1109/LED.2017.2701354.

[6] J. Wei, X. Luo, D. Ma, J. Wu, Z. Li, and B. Zhang, "Accumulation mode triple gate SOI LDMOS with ultralow on-resistance and enhanced transconductance," in *Proc. 28th Int. Symp. Power Semicond. Devices ICs (ISPSD)*, Prague, Czechia, Jun. 2016, pp. 171–174, doi: 10.1109/ISPSD.2016.7520805.

[7] X. Luo *et al.*, "Ultralow ON-resistance SOI LDMOS with three separated gates and high-*k* dielectric," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3804–3807, Sep. 2016, doi: 10.1109/TED.2016.2589322.

[8] J. Roig, D. Flores, I. Cortes, S. Hidalgo, and J. Millan, "Thin film SOI and SOS LDMOS structures with Linear Doping Profile and enlarged field plate," in *Proc. 24th Int. Conf. Microelectron.*, Nis, Serbia, May 2004, pp. 141–144, doi: 10.1109/ICMEL.2004.1314574.

[9] W. Zhang *et al.*, "A novel high voltage ultra-thin SOI-LDMOS with sectional linearly doped drift region," *IEEE Electron Device Lett.*, vol. 40, no. 7, pp. 1151–1154, Jul. 2019, doi: 10.1109/LED.2019.2919074.

[10] Z. Wang, Z. Yuan, X. Zhou, M. Qiao, Z. Li, and B. Zhang, "Ultra-low specific on-resistance lateral double-diffused metal-oxide-semiconductor transistor with enhanced dual-gate and partial P-buried layer," *Nanoscale Res. Lett.*, vol. 14, p. 38, Jan. 2019, doi: 10.1186/s11671-019-2866-5.

[11] D. Kim, K. Lee, J. Kim, J. Choi, J. Lee, and I. Cho, "The lowest on-resistance and robust 130nm BCDMOS technology implementation utilizing HFP and DPN for mobile PMIC applications," in *Proc. 31st Int. Symp. Power Semicond. Devices ICs (ISPSD)*, Shanghai, China, May 2019, pp. 391–394, doi: 10.1109/ISPSD.2019.8757571.

[12] J. Cheng, H. Huang , B. Yi , W. Zhang, and W. T. Ng, "A TCAD study on lateral power MOSFET with dual conduction paths and high-k passivation," *IEEE Electron Device Lett.*, vol. 41, no. 2, pp. 260–263, Feb. 2020, doi: 10.1109/LED.2019.2963299.

[13] R. K. Williams, M. N. Darwish, R. A. Blanchard, R. Siemieniec, P. Rutter, and Y. Kawaguchi, "The trench power MOSFET—Part II: Application specific VDMOS, LDMOS, packaging, and reliability," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 692–712, Mar. 2017, doi: 10.1109/TED.2017.2655149.

[14] Z. Xu *et al.*, "Demonstration of improvement of specific on-resistance versus breakdown voltage tradeoff for low-voltage power LDMOS," *Microelectron. J.*, vol. 88, pp. 29–36, Jun. 2019, doi: 10.1016/j.mejo.2019.04.011.

[15] Y. Zhang, S. Pendharkar, P. Hower, S. Giombanco, A. Amoroso, and F. Marino, "A RESURF P-N bimodal LDMOS suitable for high voltage power switching applications," in *Proc. 27th Int. Symp. Power Semicond. Devices ICs (ISPSD)*, Hong Kong, China, May 2015, pp. 61–64, doi: 10.1109/ISPSD.2015.7123389.

[16] S. T. Kong, P. Stribley, C. Lee, and M. Ong "Integration of 100 V LDMOS devices in 0.35 μm CMOS technology," in *Proc. 23rd Int. Symp. Power Semicond. Devices ICs (ISPSD)*, San Diego, CA, USA, May 2011, pp. 176–179, doi: 10.1109/ISPSD.2011.5890819.

[17] M. Qiao, Y. Li, X. Zhou, Z. Li, and B. Zhang, "A 700-V junction-isolated triple RESURF LDMOS with N-type top layer," *IEEE Electron Device Lett.*, vol. 35, no. 7, pp. 774–776, Jul. 2014, doi: 10.1109/LED.2014.2326185.

[18] M. Saremi, M. Saremi, H. Niazi, M. Saremi, and A. Y. Goharrizi, "SOI LDMOSFET with up and down extended stepped drift region," *J. Electron Mater.*, vol. 46, no. 10, pp. 5570–5576, Jun. 2017, doi: 10.1007/s11664-017-5645-z.

[19] M. Mehrdad, M. Zareiee, and A. A. Orouji, "Controlled kink effect in a novel high-voltage LDMOS transistor by creating local minimum in energy band diagram," *IEEE Trans. Electron Devices*, vol. 64, no. 10, pp. 4213–4218, Oct. 2017, doi: 10.1109/TED.2017.2737531.

[20] W. Zhang *et al.*, "Novel superjunction LDMOS (>950 V) with a thin layer SOI," *IEEE Electron Device Lett.*, vol. 38, no. 11, pp. 1555–1558, Nov. 2017, doi: 10.1109/LED.2017.2751571.

[21] S. E. J. Mahabadi, S. Rajabi, and J. Loiacono, "A novel partial SOI LDMOSFET with periodic buried oxide for breakdown voltage and self heating effect enhancement," *Semicond. Sci. Technol.*, vol. 26, pp. 872–879, Jul. 2016, doi: 10.1016/j.spmi.2015.07.011.

[22] J. Li, P. Li, W. Huo, G. Zhang, Y. Zhai, and X. Chen, "Analysis and fabrication of an LDMOS with high-permittivity dielectric," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1266–1268, Sep. 2011, doi: 10.1109/LED.2011.2158383.

[23] X. Zhou *et al.*, "Total-ionizing-dose irradiation-induced dielectric field enhancement for high-voltage SOI LDMOS," *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 593–596, Apr. 2019, doi: 10.1109/LED.2019.2900370.

[24] T. Erlbacher, A. J. Bauer, and L. Frey, "Reduced on resistance in LDMOS devices by integrating trench gates into planar technology," *IEEE Electron Device Lett.*, vol. 31, no. 5, pp. 464–466, May 2010, doi: 10.1109/LED.2010.2043049.

[25] S. E. J. Mahabadi, A. A. Orouji, P. Keshavarzi, and H. A. Moghadam, "A new partial SOI-LDMOSFET with a modified buried oxide layer for improving self-heating and breakdown voltage," *Semicond. Sci. TEchnol.*, vol. 26, no. 9, Jul. 2011, Art. no. 095005, doi: 10.1088/0268-1242/26/9/095005.

[26] K. Mao, H. Nie, and Y. Yao, "Effect of p-type buried layer dose on hot carrier degradation of R_{ON} in 700 V Triple RESURF nLDMOS," *IEEE Electron Device Lett.*, vol. 37, no. 3, pp. 242–244, Mar. 2016, doi: 10.1109/LED.2016.2518303.

[27] F. Ma *et al.*, "High holding voltage SCR-LDMOS stacking structure with ring-resistance-triggered technique," *IEEE Electron Device Lett.*, vol. 34, no. 9, pp. 1178–1180, Sep. 2013, doi: 10.1109/LED.2013.2272591.

[28] *Sentaurus User Guide*, Synopsys Inc., Mountain View, CA, USA, Dec. 2016.

[29] J. A. Appels and H. M. J. Vaes, "High voltage thin layer devices (RESURF devices)," in *Int. Electron Devices Meeting Tech. Dig. (IEDM)*, Washington, DC, USA, 1979, pp. 238–240, doi: 10.1109/IEDM.1979.189589.

[30] G. Mitros *et al.*, "High-voltage drain extended MOS transistors for 0.18-μm logic CMOS process," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1751–1755, Aug. 2001, doi: 10.1109/16.936703.

[31] R. V. Overstraeten and H. D. Man, "Measurement of the Ionization Rates in Diffused Silicon $p - n$ Junctions," *Solid-State Electron.*, vol. 13, pp. 583–608, May 1970, doi: 10.1016/0038-1101(70)90139-5.

[32] G. Masetti, M. Severi, and S. Solmi, "Modeling of carrier mobility against carrier concentration in arsenic-, phosphorus-, and boron-doped silicon," *IEEE Trans. Electron Devices*, vol. 30, no. 7, pp. 764–769, Jul. 1983, doi: 10.1109/T-ED.1983.21207.

[33] S. A. Mujtaba, "Advanced mobility models for design and simulation of deep submicrometer MOSFETs," Ph.D. dissertation, Dept. Elect. Eng., Stanford Univ., Stanford, CA, USA, Dec. 1995.

[34] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. Princeton, NJ, USA: Wiley, Apr. 2005, ch.4, pp. 211–212, doi: 10.1002/0471749095.

[35] M. T. Bohr and I. A. Young, "CMOS scaling trends and beyond," *IEEE Micro*, vol. 37, no. 6, pp. 20–29, Nov./Dec. 2017, doi: 10.1109/MM.2017.4241347.

[36] K. J. Kuhn, "Moore's law past 32nm future challenges in device scaling," in *Proc. 13th Int. Workshop Comput. Electron.*, May 2009, pp. 1–4, doi: 10.1109/IWCE.2009.509112.

[37] (2015). *International Technology Roadmap for Semiconductors (ITRS)*. [Online]. Available: http://www.itrs2.net/itrs-reports.html