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Monolithically Integrated Catalyst-Free High Aspect Ratio InAs-on-Insulator (InAsOI) FinFETs for pH Sensing

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ABSTRACT In this work, we report a novel Indium Arsenide-on-insulator (InAsOI) FinFET platform designed with record high aspect ratio that favors the use of the devices as charge sensors. InAs has very high mobility among III-V semiconductors and an intrinsic surface accumulation layer yielding good ohmic contacts thus making it an interesting choice for chemical and biological sensing platforms. Template Assisted Selective Epitaxy (TASE) enables the integration of III-V highly scaled devices, monolithically integrated on Silicon, within a fully CMOS compatible fabrication scheme hence without any catalyst-induced growth. With a new geometry, high-aspect-ratio (HAR) InAs fins and a new application of pH sensing the versatility of TASE is exhibited. HAR InAs fins, fin height to fin width in excess of 4 for fin width down to 30 nm are fabricated on a Si substrate. The HAR InAs-on-insulator fins are characterized as pH sensors. A sensitivity of 38.8 mV per pH is extracted at 6 μA drain current from a 40 nm wide 20 multi-finger array.

INDEX TERMS III-V, high-aspect ratio, FinFET, InAs, ISFET, pH Sensor.

I. INTRODUCTION

Ion sensitive field effect transistors (ISFETs) have been proposed by Bergveld in 1970s and have evolved considerably since. ISFETs are modified MOSFETs where the gate metal electrode is replaced with a liquid under test via a reference electrode [1]. Recently three-dimensional (3D) structures, such as nanowires (NW) or FinFETs have become of interest for sensing applications rather than their planar counterparts [2]. In 3D structures, higher surface-to-volume ratios and sizes comparable to chemical/biological elements enable surface interactions to affect the bulk of semiconductor. Also, 3D architectures such as High Aspect Ratio (HAR) structures are known to be more favorable for sensing since they facilitate the capture of the species arriving from three different directions. This is perceptible especially at very low analyte concentrations where a reasonably fast response time or short settling time may still be obtained [3]. The settling time is the time taken by a sensor to capture a certain number of analyte molecules and produce a stable shift in device characteristics. Indium arsenide (InAs) is an interesting material choice for chemical and biological sensing platforms due to high electron mobility and to the formation of a surface accumulation layer that enables high quality ohmic contacts. InAs NWs have been used in gas sensing [4], protein sensing [5], interfacing live mammalian cells [6] and also pH sensing [7]. Moreover, InAs NWs have been shown to exhibit charge dragging effect [8]. Charge dragging refers to a situation where ionic fluid flow energy can generate a voltage or current. This particularity of InAs NWs can potentially enable bio-sensing in

combination with energy harvesting. For sensing, it is agreed that the fabrication of high density arrays enables detection of multiple target analytes. Moreover, a CMOS compatible process allows signal conditioning circuitry to be integrated along with the sensor for improved noise performance. However, in the afore-mentioned InAs platforms, invariably NWs are grown on a different substrate and then manually transferred to a Si substrate. The NW deposition is random and subsequent processing always needs customization. In some cases, high-density NW arrays were fabricated by the use of Au-catalyst particles, making the process non-CMOS compatible. This work addresses some of the shortcomings of these InAs NW sensing platforms. Using Template Assisted Selective Epitaxy (TASE) various III-V nanoscale devices are grown by means of metal organic chemical vapor deposition (MOCVD) on Si-substrate [9], [10]. In this work we demonstrate monolithically integrated, catalyst free High-Aspect-Ratio (HAR) InAs FinFETs for pH sensing.

II. DEVICE FABRICATION

Device fabrication is explained first as template fabrication and next as the device processing where process steps to demonstrate sensing are carried out. Template fabrication begins with the definition of alignment markers and ends when InAs fins grown with TASE process on Si substrate. Device processing consists of the subsequent steps of source/drain metallization, gate oxide deposition and channel isolation.

The starting substrate is a silicon-on-insulator wafer with 110 nm silicon device layer and 2 μm buried oxide. The side view cross sections of the main template fabrication steps are illustrated in Fig. 1(a) to (d). In Fig. 1 (a) an array of fins with the width ranging from 20nm to 70nm are patterned into the silicon layer using a 2% diluted HSQ e-beam resist with Electron Beam Lithography (EBL). The fin pattern is transferred into silicon with an anisotropic HBr dry etch. Then in Fig. 1(b) template deposition steps consist of Atomic Layer Deposition (ALD) and Chemical Vapor Deposition (CVD) of 80nm oxide here on referred to as template oxide.

Further, access regions are patterned on one end of the template structure using PMMA e-beam resist. A short dilute HF (DHF) dip then exposes the underlying silicon as illustrated in Fig. 1(b). Next, using 2% diluted TMAH the silicon inside the template is emptied in a controlled manner such that a combination of a silicon seed segment and hollow region remain as shown in Fig. 1(c). Then a very short DHF step is carried out right before Metal Organic Chemical Vapor Deposition (MOCVD) to remove native oxide on Si seed. This step expands the inner dimensions of the template oxide in all directions and determines the difference between the InAs width of the fins and the designed Si fin width. Finally, InAs is selectively grown using MOCVD at 550°C using trimethylindium (TMIn) and arsine (AsH_3) as precursors. As seen in Fig. 1(d) there is a template oxide on almost all sides of the grown InAs except the access region.

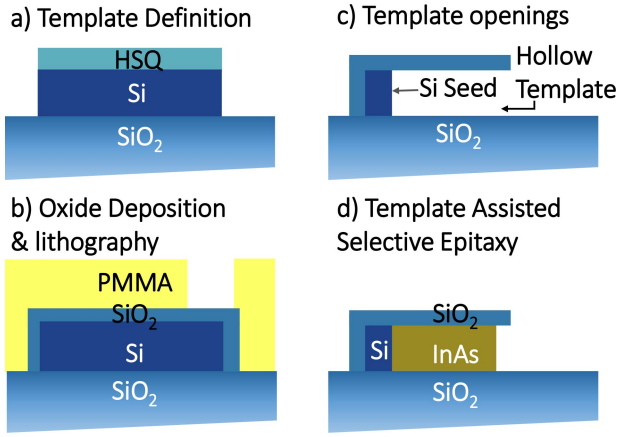

FIGURE 1. Side view of the main template fabrication steps- (a) Template definition using EBL and dry etching, (b) template deposition using ALD and LPCVD oxide & patterning access regions using EBL, (c) template openings in PMMA using EBL, (d) template assisted MOCVD growth of InAs from Silicon seed.

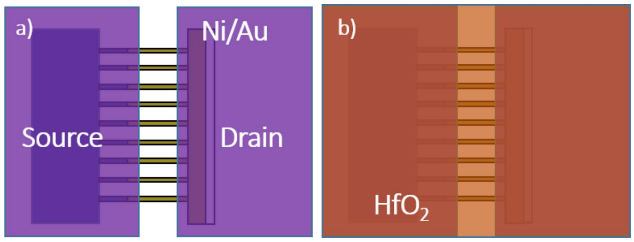

FIGURE 2. Top view of device processing steps- (a) Source/drain metallization using e-beam patterning and resist lift-off (b) ALD deposited HfO_2 behaves as gate oxide and isolation oxide.

Hence, a DHF dip partially removes this template oxide. Only 10nm of template oxide is left in order to preserve the structure integrity during the subsequent fabrication steps. Source & drain region definition is carried out with an EBL step as depicted in Fig. 2(a) using PMMA resist.

After EBL, the samples are dipped in DHF to remove the template oxide on the source/drain contact regions. Then the samples are transported quickly from the wet bench into the evaporation chamber using a vacuum transfer box to minimize re-oxidation of the surface. 20nmNi/150nmAu is evaporated to ensure good fin sidewall coverage. The samples are kept in solvent to lift-off the resist such that all residues are cleared away. Then the sample is loaded into an ALD reactor for 20nm HfO_2 deposition at 200°C as shown in Fig. 2 (b). HfO_2 functions as the gate sensing oxide and also isolates the channel region from source/drain metallized areas.

III. CHARACTERIZATION RESULTS

A. PROCESS CHARACTERIZATION

Scanning Electron Micrograph (SEM) images shown in Fig. 3 (a) to (d) correspond to those illustrated in Fig. 1 (a) to (d). Fig. 3 (a) is a tilted SEM image of etched Si fins with remaining HSQ resist; this step determines the fin template width and height. Next, Fig. 3 (b) shows access

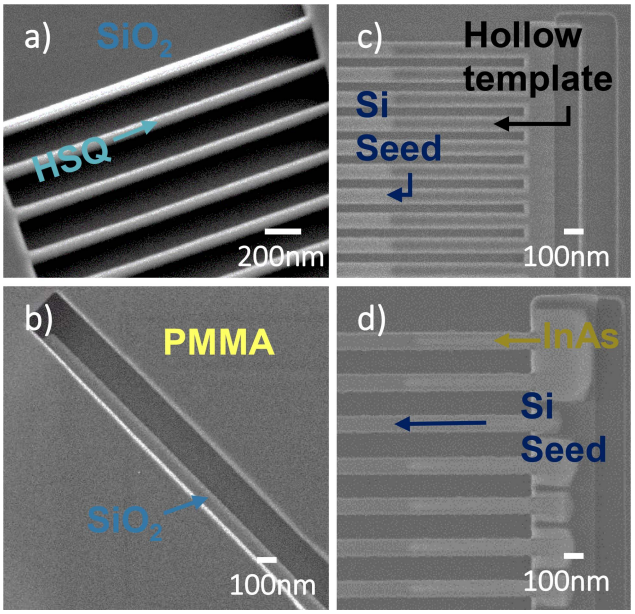

FIGURE 3. SEM images taken at steps as shown in the fabrication schematic (a) tilted view of template definition (b) tilted view of Oxide template deposition using ALD and LPCVD oxide, (c) tilted view of PMMA resist opening underlying template, (d) top view of MOCVD grown 40 nm wide InAs fins inside SiO_2 template.

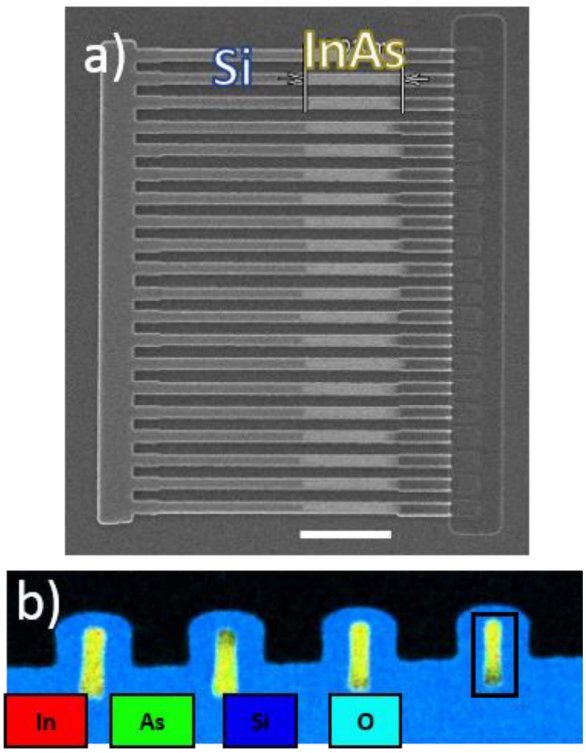

FIGURE 4. (a) Top view of multiple fin array of InAs grown uniformly from Silicon seed, scale bar = 1μm (b) EDX elemental analysis of In, As, Si, O constituents.

windows in PMMA e-beam resist well aligned to the underlying template structure which underwent oxide deposition. In this step the SiO_2 covering the silicon fins is etched away in DHF dip.

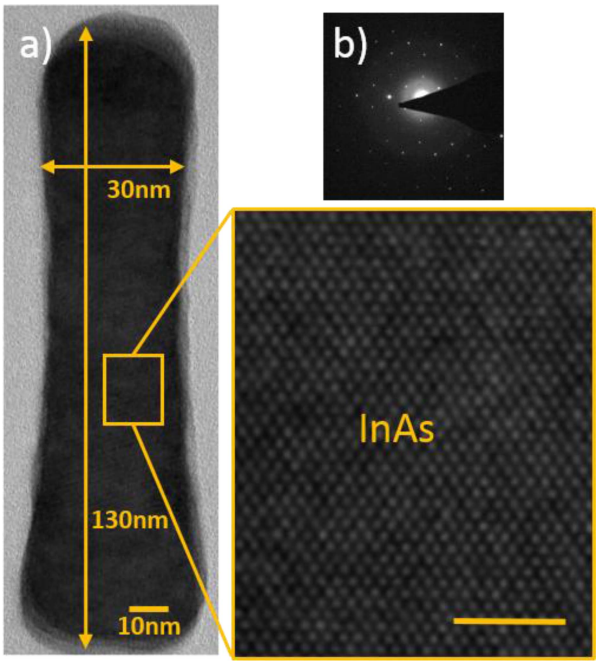

FIGURE 5. (a) HR TEM image of HAR fin with aspect ratio in excess of 4 and a zoom on the right of highly crystalline grown InAs, scale bar = 5nm (b) SEAD diffraction pattern at the center of the zoom confirms the monocrystalline nature.

Then PMMA resist is stripped and the sample is ready for the next step. After a controllable TMAH wet etch a partially hollow SiO_2 template remains with a Si seed as imaged in Fig. 3(c). Finally, as shown in Fig. 3(d) using MOCVD InAs is selectively grown from the silicon seed. The grown InAs region can be clearly distinguished as the lighter part in contrast to the darker silicon seed.

A device with grown fins is pictured in the scanning electron micrograph in Fig. 4(a). It consists of an array of 20 InAs fins with $W_{FIN} = 50$ nm each and a pitch of 250 nm grown uniformly inside the template to a length of 1μm. Next in Fig. 4 b), using Energy Dispersive X-ray (EDX) spectroscopy an elemental material analysis map confirms selective growth of InAs inside the SiO_2 template. No dopants were intentionally introduced during the MOCVD growth.

Detailed high resolution microscopy enables us to examine the quality of InAs grown. In Fig. 5 (a) to (b) Transmission Electron Microscope (TEM) is used for characterization of the narrowest fins grown. The highest aspect ratio of the InAs fin is calculated as the height ($H_{FIN} = 130$ nm) to width ($W_{FIN} = 30$ nm) ratio of $\sim$ 4:1. Also we see in Fig. 5(b) that the Selective Area Electron Diffraction (SAED) image in the specific region shows bright spots that confirm mono-crystallinity of the InAs.

In Fig. 6 (a) an optical microscope image of the source/drain wiring on the devices is displayed. A very clean lift-off is indeed seen. In Fig. 6 (b), a SEM image shows the device after source/drain metallization and deposition of ALD oxide.

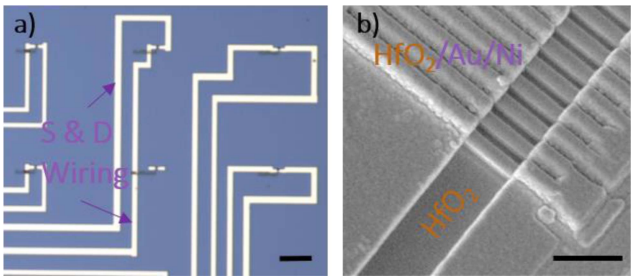

FIGURE 6. (a) Optical microscope image of source/drain metallization showing a clean lift-off step, scale bar = 50 μm (b) Tilted SEM image after ALD oxide is deposited on the channel region and S&D isolation, scale bar = 500 nm.

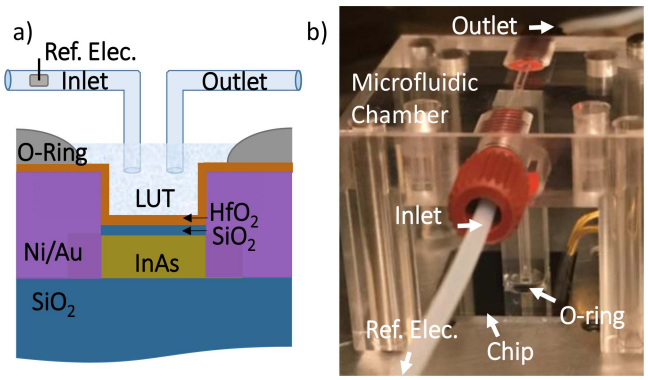

FIGURE 7. (a) Side view schematic of the main components in pH measurement setup (b) Photograph of pH measurement setup.

B. PH CHARACTERIZATION

The setup for pH characterization is depicted and photographed in Fig. 7(a) and (b) respectively. A specially fabricated fluidic chamber is clamped to the sample. Hence, the Liquid under test (LUT) is contained in a 5mm diameter O-ring to cover devices of interest. A commercial external Ag/AgCl reference electrode in the inlet ensures a stable potential, i.e., reference voltage (V_G) is applied to the gate of the device via LUT.

Fig. 8 to 10 show graphs and data analysis for the same device with 50 nm fin width. It is visible in Fig. 8 that there is a systematic shift in the drain current (I_D) curves when the reference voltage is swept through various pH buffer solutions from pH 7 to pH 4, with a decrease in sensitivity near pH 4, which may indicate a limited buffer capacity of the oxide surface. It is worth noting that due to a partial fluid gate overlapping over the FinFET structure, the InAs Fin-ISFET is not fully depleted and the device is never completely turned OFF by gate action. Moreover, rest of the measurements taken were on devices with $W_{FIN}>$ 50 nm, along with high doping levels contributing further to this problem. However, this does not prevent the use in sensing applications maintaining high linearity, a high ON current and high sensitivity.

It can be further seen in Fig. 8 that the ON current is a couple of microamperes even with a drain-source voltage as low as 10 mV. This is due to the presence of a surface

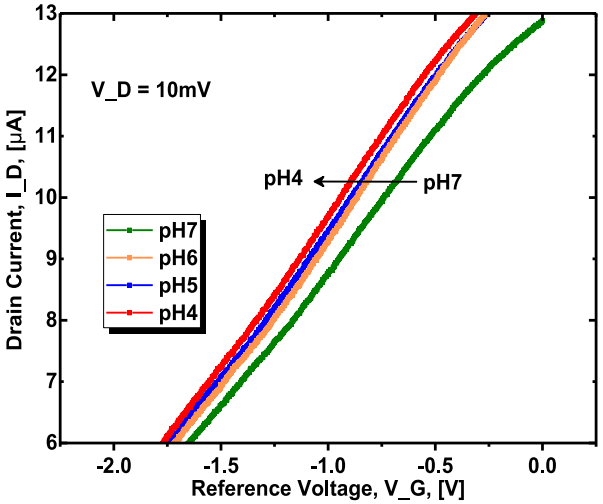

FIGURE 8. Drain current through the device as V_G is swept through different pH buffers pH 7 to pH 4. Device fin width is 50 nm.

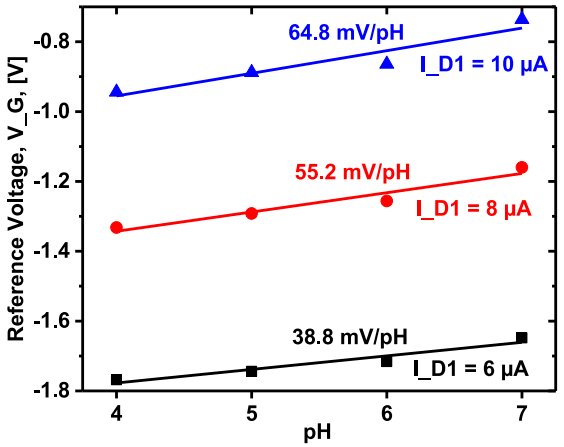

FIGURE 9. Linear pH response extracted at different current levels. Device fin width is 50 nm.

electron accumulation layer in InAs leading to good n-type contacts.

The shift in the drain current curves is further inferred in Fig. 9, where a highly linear response is observed in the reference voltage shift from pH 6 to pH 4 for all the extracted drain current values. When pH 7, is also taken into account the Nernstian sensitivity of 64.8 mV/pH is extracted at 10 μA drain current whereas the difference from the Nernstian limit is probably an artifact of experimental linearity related to fitting the data. This sensitivity appears to be lower at a smaller level of the constant current used for extraction, where the sensor response is more linear. In this region we extract a sensitivity of 38.8 mV/pH at 6 μA drain current.

In Fig. 10 a double sweep of drain current vs reference voltage is plotted for two pH values. The device displays hysteretic behavior. In the inset, the hysteresis value is calculated to be 108 mV for pH 7 and also lies in the same interval for pH 4.

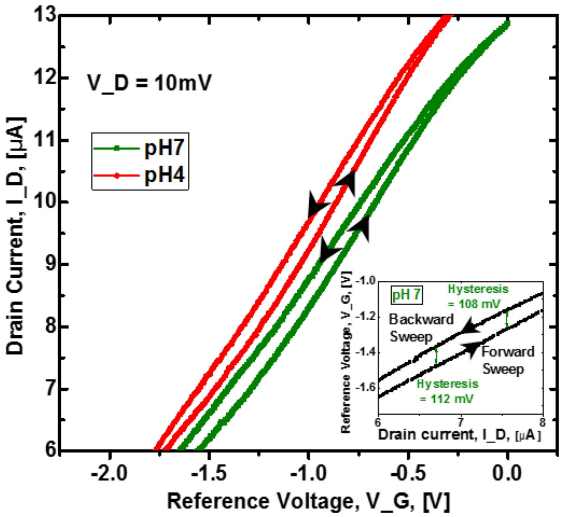

FIGURE 10. Double sweep of drain current vs reference voltage for pH7 and pH4. Inset: pH7 hysteresis is calculated to be in the range of 0.1 V.

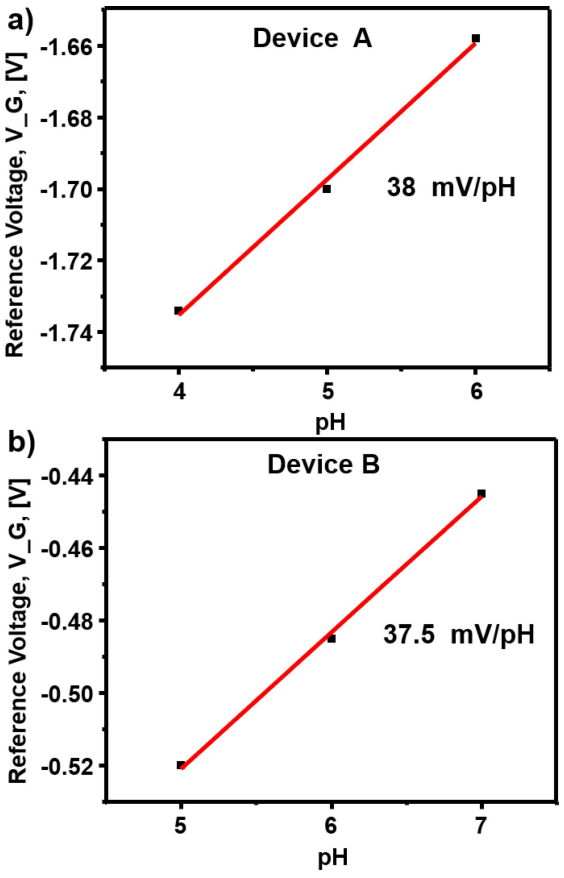

FIGURE 11. Linear pH response extracted at 19 μA different current levels.

In Fig. 11 (a) – (b), data from two separate devices with the same fin width of 80 nm are compared. To show the reproducibility in same geometry, sensitivity is extracted at a common current level of 19 μA drain current and plotted in Fig. 11 (a) – (b). The pH response is seen to be linear but also close to 40 mV/pH as for the previous device.

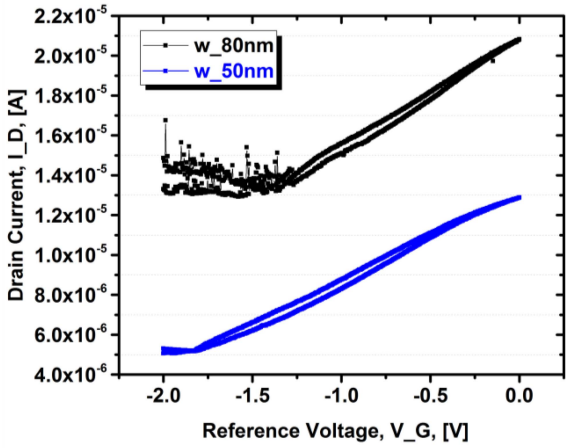

FIGURE 12. Modulation of the ON current for fins of different widths 50 nm and 80 nm.

In Fig. 12 we compare the I_D vs V_G characteristics from two devices with fin widths of 50 nm and 80 nm at pH 5. The reported curves are a double sweep showing also the hysteresis. From these characteristics, we see that for the wider fin (80 nm) the modulation of the ON current is about 30%, whereas in the case of the narrower fin (50 nm), the modulation of the ON current improves to about 60%. Clearly the devices are still only partially depleted.

Further characterization was performed on selected devices. A metal gating was realized by means of electron beam induced deposition of platinum and subsequent patterning of this layer using the Focused Ion Beam (FIB) tool. The characteristics of a metal gate FinFET, used for the mobility extraction, are shown in Fig. 13.

A charge-based model for a junctionless transistor has been derived previously [11], [12], leading to an explicit formula describing the drain current. The current equation in the saturation region used for mobility calculation is taken from [12] and it is adapted to our symbol notation:

$$I_{DS} \approx \mu \frac{\beta t_{ox}}{2\varepsilon_{ox}} \frac{H_{Fin}}{L} \left(qN_{InAs}W_{Fin}\right)^2$$

where $\beta = 1 + \frac{\varepsilon_{ox} W_{Fin}}{4 t_{ox} \varepsilon_{InAs}}$.

From this equation the mobility is calculated to be 165 cm^2/Vs.

IV. SIMULATION

In order to verify the depletion condition for the FinFET structures, Sentaurus TCAD simulations were performed. The FinFET structure is entirely made of InAs with H_{Fin} = 130 nm and W_{Fin} = 40 nm, 80 nm. It is entirely n-doped. The doping level is varied between 4e17 cm^{-3} and 2e18 cm^{-3} as the previously known doping limits possible with the MOCVD deposition tool. The gate length (L_G) is 200 nm. The gate oxide stack consists of 10 nm SiO_2 and 20 nm HfO_2 resembling the fabricated structures. The Shockley-Read-Hall recombination model was applied whereas no trap assisted tunneling models were included. The simulated transfer characteristics are shown in Fig. 14. For the

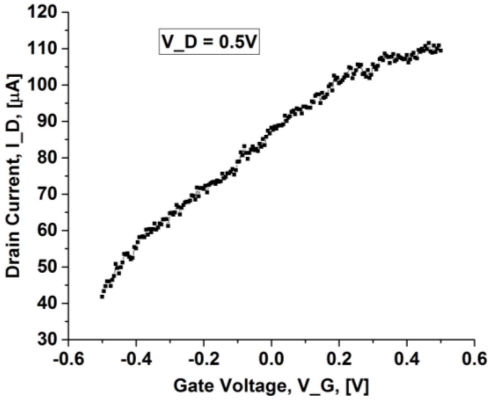

FIGURE 13. I_D vs V_G of the metal gate device with V_D = 0.5V.

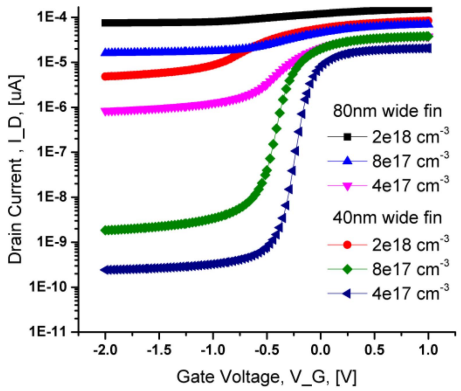

FIGURE 14. TCAD simulation of I_D vs V_G transfer characteristics.

80 nm wide fin, even for doubling the doping level, i.e., 4e17 cm^{-3} and 8e17 cm^{-3}, the modulation of drain current varies much drastically from less than two orders of magnitude (pink curve) to a percentage of the modulated current (bright blue curve).

All the measured devices characteristics correspond to the modulation close to the ON current with high OFF current because there always remained a conducting channel in the FinFET due to a partial liquid gating. Hence, a better control of the non-intentional doping level, narrower fin width and easing pitch design are necessary to observe better modulation of drain current, as indicated by the simulation results obtained for the 40 nm fin.

V. CONCLUSION

First of all, the proposed method allows for a large scale production of InAs based sensor devices compared to other state of the art platforms. Second, thanks to the inherent surface electron accumulation layer a good contact to InAs is obtained, which is confirmed by high drain current levels even at low drain-source voltages. Finally, from an explicit drain current model we extract mobility of the device to be 165 cm^2/Vs enabling charge sensing with high level of output current. In this work, we explored and demonstrated, as a proof of concept, that TASE has the capability to achieve a new geometry of HAR InAs FinFETs difficult to be achieved by other technologies serving pH sensing. In Table 1 the state- of-the-art geometrical parameters in various III-V FinFET technologies are compared to this work, where InAs FinFETs on Si substrates with one of the highest aspect ratios (4:1) are presented.

TABLE 1. State of the art III-V fin geometry technologies.

Ref	Substrate	III-V Type	Indium Mole Fraction	Etching or Growth	H_{FIN} (nm)	W_{FIN} (nm)	Aspect Ratio, H_{FIN} : W_{FIN}
[13]	InAs	InAs	1	Etching	20	25	4:5
[14]	InAlAs	InGaAs	0.53	Etching	50	30	5:3
[15]	InP	InGaAs	0.53	Etching	20	30	2:3
[16]	InP	InGaAs	0.7	Etching	120	38	~3:1
[17]	InP	InGaAs	0.53	MOVPE	16	40	2:5
[18]	InP	InGaAs	0.53	Etching Digital Etch	170 170	25 8	~7:1 ~20:1
[19]	Si	InGaAs	0.7	Epitaxy	25	50	1:2
[20]	Si	InAs	1	Etching	9	40	~1:4
Our Work	Si	InAs	1	MOCVD	130	30	~4 :1

In summary, we demonstrated a monolithically integrated, scalable, catalyst-free, CMOS compatible, high aspect ratio InAs-On-Insulator FinFET platform for pH sensing. A good sensitivity of 38.8 mV/pH has been extracted for a couple of devices. The partial depletion is attributed to the high doping level.

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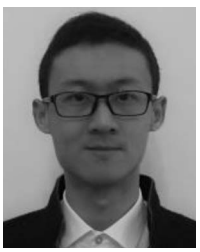

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