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Unified Analytical Model for SOI LDMOS With Electric Field Modulation

BAOXING DUAN, JINGYU XING, ZIMING DONG, AND YINTANG YANG (Senior Member, IEEE)

Key Laboratory of the Ministry of Education for Wide Band-Gap Semiconductor Materials and Devices, School of Microelectronics, Xidian University, Xi'an 710071, China

CORRESPONDING AUTHOR: B. DUAN (e-mail: bxduan@163.com)

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ABSTRACT The unified analytical model is proposed for SOI LDMOS (Silicon On Insulator Lateral Double-diffused Metal Oxide Semiconductor) based on the electric field modulation in this paper for the first time. The analytical solutions of the surface electric field distributions and potential distributions are derived on the basis of the 2-D Poisson equation. The variation of the buried layer parameters modulates the surface electric field by the electric field modulation effect to optimize the surface electric field distribution of the device. Also, the simulation results obtained through the simulation software ISE are consistent with the expected results of the analytical model. This not only proves the feasibility of the electric field modulation theory, but also shows that the accurate analytical model will be of great guiding significance for designing and optimizing the same LDMOS based on SOI structures.

INDEX TERMS Analytical model, SOI LDMOS, electric field modulation effect, Poisson equation, surface electric field.

I. INTRODUCTION

As the most widely used lateral power device, SOI LDMOS devices combine SOI technology, microelectronic technology and power electronics technology [1]. With its unique isolation performance, small leakage, fast speed and low power consumption, it has always occupied a unique advantage in high-performance single-chip power integration technology, and has been rapidly developed in the past decade [2]–[3]. The new high-speed, high-integration, low-power switching circuit and power amplifier circuits required by various power conversion and energy processing devices are core devices based on SOI LDMOS devices [4]. However, on the one hand, the SOI power device isolates the surface of the device from the substrate due to the buried layer of the dielectric, thereby generating a self-heating effect, which affects the normal operation and reliability of the device [5]–[6]. On the other hand, at the S_i / SiO_2 interface of conventional SOI LDMOS structure, the critical breakdown electric field of S_i is lower than that of S_iO_2, so the breakdown usually occurs at the S_i layer of the interface, which makes the high critical breakdown electric field of S_iO_2 underutilized and the breakdown voltage of the device low [7]–[8]. Therefore, how to further improve the performance characteristics of SOI power devices has always been a hot research topic in the field of power integrated circuits (PIC) at home and abroad [9]–[10].

In order to improve the performance of lateral SOI high voltage devices, design researchers have proposed a variety of optimization schemes for new device structures: air partial SOI (APSOI) structure [11], single step buried oxide layer SOI (SBOSOI) structure [12], double step buried oxide layer SOI (BODSSOI) structure [13], P-type buried layer SOI (BPSOI) structure [14], variable low-k dielectric buried layer BPSOI (VLKD BPSOI) structure [15], and low-k dielectric buried layer PSOI (LK PSOI) structure [16]. Under the effect of electric field modulation [17], these changes in buried layer will introduce new electric field peaks on the surface of the drift region, which will make the surface electric field distribution more evenly and improve the performance of SOI LDMOS significantly. At the same time, in order to further guide the optimization of device structure parameters, and analyses the working mechanism of the device, and shorten the device development cycle, many researchers have conducted in-depth research on the analytical model of the lateral power device. Appels and Vaes proposed a Reduce Surface Field (RESURF) criterion that

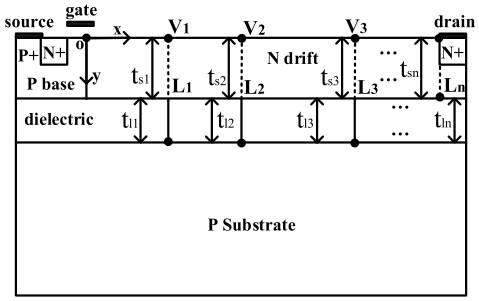

FIGURE 1. Cross-sectional view of electric field modulated SOI LDMOS.

can be universally applied to lateral power devices [18]. Chung and Han assumed that the vertical electric field on the surface of the drift region is zero and the vertical electric potential distribution of the top silicon can be expressed as a quadratic function, and the two-dimensional electric potential distribution and electric field distribution in drift region of the SOI lateral power device were obtained [19]. Yuan *et al.* obtained a two-dimensional analytical model of the SBOSOI and BODSSOI by using drift region partitioning [20]–[21]. However, these analytical models are built for specific structures. For SOI LDMOS based on electric field modulation, there is no uniform analytical model to explain the electric field modulation effect in these structures in essence. Therefore, further research about these are of great guiding significance to the design and analysis of SOI LDMOS structures.

In this paper, a unified numerical model of SOI LDMOS based on electric field modulation is proposed. Several SOI LDMOS structures based on electric field modulation are taken as examples to check on the accuracy of the unified numerical model and explain the mechanism of electric field modulation in detail.

II. THE UNIFIED NUMERICAL MODEL OF ELECTRIC FIELD MODULATED SOI LDMOS

The cross-sectional view of electric field modulated SOI LDMOS is shown in Fig. 1, there are n regions with different buried layers as interfaces in the drift region, and the boundaries are $L_1, L_2, L_3, \ldots L_n$, respectively. The thickness of buried layer in each region are respectively $t_{11}, t_{l2}, t_{l3}, \ldots t_{ln}$, and the thickness of drift region in each region are respectively $t_{s1}, t_{s2}, t_{s3}, \ldots t_{sn}$. The drift region doping concentrations are $N_{d1}, N_{d2}, N_{d3}, \ldots N_{dn}$, and N_t is the doping concentration of substrate layer. A voltage V_d is applied to the drain, and the substrate and the source are grounded. When the device is operating in reverse, the gate is connected to the zero potential.

In the case of device reverse bias, when the drift region is completely depleted, the potential distribution of each region of the drift satisfies the 2-D Poisson equation [22].

$$\frac{\partial^2\varphi_{\rm i}(x,y)}{\partial x^2}+\frac{\partial^2\varphi_{\rm i}(x,y)}{\partial y^2}=-\frac{qN_{\rm di}}{\varepsilon_{\rm s}},\ i=1,2,3,\ldots n \tag{1}$$

The drift region potential distribution $\varphi_{\rm i}(x,y)$ is subjected to three Taylor expansions in the y direction to obtain (2).

$$\varphi_{\rm i}(x,y)=\varphi_{\rm i}(x,0)+\frac{\partial\varphi_{\rm i}(x,0)}{\partial y}y+\frac{\partial^2\varphi_{\rm i}(x,0)}{2\partial y^2}y^2 \tag{2}$$

Since the vertical component of the electric field on the top silicon surface is much less than the lateral component, we treat it as zero to obtain equation (3).

$$\left.\frac{\partial\varphi_{\rm i}(x,y)}{\partial y}\right|_{y=0}=0 \tag{3}$$

According to the continuity of electrical displacement on the lower surface of the drift region, equation (4) can be obtained. When the buried layer is a silicon window, it can be expressed as (4a). When the buried layer is a insulating medium with other dielectric constant, it is (4b). Where the electric field distribution of the dielectric layer is approximately uniform, t_{subi} is the depth of depletion layer [30], $\varepsilon_{\rm s}$ and $\varepsilon_{\rm li}$ are respectively the dielectric coefficient of Silicon and buried layers.

$$-\left.\frac{\partial\varphi_{\rm i}(x,y)}{\partial y}\right|_{y=t_{\rm si}}=\frac{2\varphi_{\rm i}(x,t_{\rm si})}{t_{\rm subi}} \tag{4a}$$

$$-\varepsilon_{\rm s}\left.\frac{\partial\varphi_{\rm i}(x,y)}{\partial y}\right|_{y=t_{\rm si}}=\varepsilon_{\rm li}\frac{\varphi_{\rm i}(x,t_{\rm si})-\varphi_{\rm i}(x,t_{\rm si}+t_{\rm li})}{t_{\rm li}} \tag{4b}$$

According to the continuity of electric field and electric potential in the limiting surface of adjacent areas in drift region, equation (5)-(6) can be obtained.

$$\frac{\partial\varphi_{\rm i}(L_{\rm i},y)}{\partial x}=\frac{\partial\varphi_{\rm i+1}(L_{\rm i},y)}{\partial x} \tag{5}$$

$$\varphi_{\rm i}(L_{\rm i},0)=\varphi_{\rm i+1}(L_{\rm i},0)=V_{\rm i} \tag{6}$$

Equation (7) represents the electric potential at the boundary of the drift region.

$$\varphi_1(0,0)=0,\varphi_{\rm n}(L_{\rm n},0)=V_{\rm d} \tag{7}$$

On the basis of the equation (1), the first-order partial derivatives are simultaneously obtained for both sides of the formula (2), and combined with equation (3)-(7), the surface potential distribution of the device can be expressed as (8). And where $t_{\rm i}$ is the characteristic thickness of each region [20], [21], [28], [30].

$$\frac{\partial^2\varphi_{\rm i}(x,0)}{\partial x^2}-\frac{\varphi_{\rm i}(x,0)}{t_{\rm i}^2}=-\frac{qN_{\rm di}}{\varepsilon_{\rm s}} \tag{8}$$

On this basis, using boundary conditions (3)-(7) to solve the equation (8), the expression of surface potential in each region can be obtained as (9).

$$\varphi_{\rm i}(x,0)=\frac{qN_{\rm di}t_{\rm i}^2}{\varepsilon_{\rm s}}+\left(V_{\rm i}-\frac{qN_{\rm di}t_{\rm i}^2}{\varepsilon_{\rm s}}\right)\frac{\sinh\left(\frac{x-L_{\rm i-1}}{t_{\rm i}}\right)}{\sinh\left(\frac{L_{\rm i}-L_{\rm i-1}}{t_{\rm i}}\right)}+\left(V_{\rm i-1}-\frac{qN_{\rm di}t_{\rm i}^2}{\varepsilon_{\rm s}}\right)\frac{\sinh\left(\frac{L_{\rm i}-x}{t_{\rm i}}\right)}{\sinh\left(\frac{L_{\rm i}-L_{\rm i-1}}{t_{\rm i}}\right)},\quad L_{\rm i-1}\le x\le L_{\rm i} \tag{9}$$

According to equations (1), (2) and (14) and boundary condition (3), we can get the potential expression at any point of the device by using the formula $\frac{\partial^2\varphi_i(x,0)}{\partial y^2} = -\frac{\varphi_i(x,0)}{t_i^2}$ obtained in solving the equation (8) as follows:

$$\varphi_i(x, y) = \left(1 - \frac{y^2}{2t_i^2}\right)\varphi_i(x, 0) \tag{10}$$

Through the lateral component $|E_x(x, y)| = \frac{\partial\varphi(x,y)}{\partial x}$ and vertical component $|E_y(x, y)| = \frac{\partial\varphi(x,y)}{\partial y}$ of the electric field, the electric field expression at any point of the device can be expressed as (11).

$$|E(x, y)| = \sqrt{E_x^2(x, y) + E_y^2(x, y)} \tag{11}$$

Substituting $y = 0$ into equation (11), then simplifying equation (11) in combination with boundary condition (3), after that, solving the first-order partial derivative in x direction for equation (9), and substituting the result into the simplified equation (11), the expression of surface electric field in each region can be described as (12).

$$\begin{aligned} E_i(x, 0) = &\left(V_i - \frac{qN_{di}t_i^2}{\varepsilon_s}\right)\frac{\cosh\left(\frac{x-L_{i-1}}{t_i}\right)}{t_i\sinh\left(\frac{L_i-L_{i-1}}{t_i}\right)} \\ &- \left(V_{i-1} - \frac{qN_{di}t_i^2}{\varepsilon_s}\right)\frac{\cosh\left(\frac{L_i-x}{t_i}\right)}{t_i\sinh\left(\frac{L_i-L_{i-1}}{t_i}\right)}, \\ &L_{i-1} \le x \le L_i \end{aligned} \tag{12}$$

Meanwhile, through equations (10) and (11), the expression of buried layer electric field is given by (13).

$$E_{li}(x, t_{si}) = \sqrt{\left[\left(1 - \frac{t_{si}^2}{2t_i^2}\right)E_i(x, 0)\right]^2 + \left[\left(-\frac{t_{si}}{t_i^2}\right)\varphi_i(x, 0)\right]^2} \tag{13}$$

On this basis, the expression describing the electric field modulation mechanism can be expressed as (14) by mathematical transformation.

$$\begin{aligned} &|E_i(x, 0)| \\ &= \sqrt{\left(\frac{2t_i^2}{2t_i^2 - t_{si}^2}\right)^2\left\{[E_{li}(x, t_{si})]^2 - \left[\left(-\frac{t_{si}}{t_i^2}\right)\varphi_i(x, 0)\right]^2\right\}} \end{aligned} \tag{14}$$

It can be seen from equation (14) that the electric field of the buried layer has a positive correlation with the surface electric field and the change of the buried electric field affects the distribution of the surface electric field. When a new electric field peak is generated in the buried layer electric field, a new electric field peak is also generated in the surface electric field. When the electric field of the buried layer increases, the surface electric field also increases and so on. That is to say, the surface electric field can be optimized by the buried electric field to further optimize the device performance.

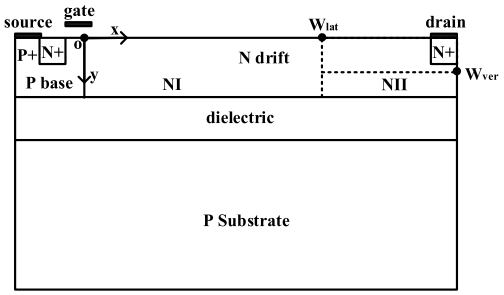

FIGURE 2. Cross-sectional view of electric field modulated SOI LDMOS under incomplete depletion.

Theoretically, when the breakdown occurs simultaneously in the PN and N^+N junctions, i.e., $E(0, 0) = E(L_n, 0) = E_C$, the BV of the device is highest. Substituting this equation into equation (12) with (6), (7) and (9), the RESURF condition [23]–[24] of SOI LDMOS device should be satisfied as (15).

$$N_d \times t_{eff} \le \varepsilon_s E_C/q \tag{15}$$

where t_{eff} is the equivalent characteristic thickness of the device [20], [21], [28], [30] and the E_C is the critical breakdown electric field of the silicon.

When the device is not completely depleted, the cross-section view of the depletion region is shown in Fig. 2, which is divided into NI and NII, and the W_{lat} is the lateral depletion width. And when W_{lat} satisfies $L_{m-1} = W_{lat} = L_m (m = 1, 2 \ldots n, i = 1, 2 \ldots m)$, the surface electric field of NI will be obtained as (16).

The W_{lat} can be obtained according to equation (16) based on the fact that the electric field in the edge of depletion region is 0. Especially when $W_{lat} = L_n$, drift region in the x direction completely depleted, the lateral depletion voltage V_{lat} at this time is just the V_d.

$$\begin{aligned} &E(x, 0) \\ &= \begin{cases} \left(V_i - \frac{qN_{di}t_i^2}{\varepsilon_s}\right)\frac{\cosh\left(\frac{x-L_{i-1}}{t_i}\right)}{t_i\sinh\left(\frac{L_i-L_{i-1}}{t_i}\right)} - \left(V_{i-1} - \frac{qN_{di}t_i^2}{\varepsilon_s}\right) \\ \quad \frac{\cosh\left(\frac{L_i-x}{t_i}\right)}{t_i\sinh\left(\frac{L_i-L_{i-1}}{t_i}\right)}, \qquad L_{i-1} \le x \le L_i \\ \left(V_m - \frac{qN_{dm}t_m^2}{\varepsilon_s}\right)\frac{\cosh\left(\frac{x-L_{m-1}}{t_m}\right)}{t_m\sinh\left(\frac{W_{lat}-L_{m-1}}{t_m}\right)} - \left(V_{m-1} - \frac{qN_{dm}t_m^2}{\varepsilon_s}\right) \\ \quad \frac{\cosh\left(\frac{W_{lat}-x}{t_m}\right)}{t_m\sinh\left(\frac{W_{lat}-L_{m-1}}{t_m}\right)}, \qquad L_{m-1} \le x \le L_m \end{cases} \end{aligned} \tag{16}$$

Ignoring the effect of lateral depletion region in device depletion region NII, the electric field and potential distributions among the N^+ drain and the buried layer can be approximated by a one-dimensional abrupt junction [21]. Let the width of its vertical depletion region be W_{ver}, then the

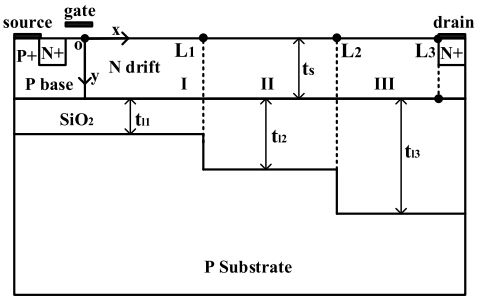

FIGURE 3. Cross-sectional view of SBOSOI LDMOS.

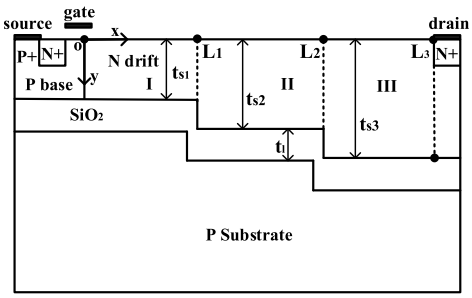

FIGURE 4. Cross-sectional view of BODSSOI LDMOS.

distribution of electric field and potential in NII is expressed as (17)-(18).

$$E(L_{\mathrm{n}}, y) = \begin{cases} 00 \le y \le t_{\mathrm{sn}} - W_{\mathrm{ver}} \\ qN_{\mathrm{dn}}(y + W_{\mathrm{ver}} - t_{\mathrm{sn}})/\varepsilon_{\mathrm{s}} t_{\mathrm{sn}} - W_{\mathrm{ver}} \le x \le t_{\mathrm{sn}} \end{cases} \tag{17}$$

$$\varphi(L_{\mathrm{n}}, y) = \begin{cases} V_{\mathrm{d}} 0 \le y \le t_{\mathrm{sn}} - W_{\mathrm{ver}} \\ V_{\mathrm{d}} - qN_{\mathrm{dn}}(y + W_{\mathrm{ver}} - t_{\mathrm{sn}})^2/(2\varepsilon_{\mathrm{s}}), \\ \quad t_{\mathrm{sn}} - W_{\mathrm{ver}} \le x \le t_{\mathrm{sn}} \end{cases} \tag{18}$$

An expression for the W_{ver} can be obtained as (19).

$$W_{\mathrm{ver}} = \sqrt{\left(\frac{t_{\mathrm{ln}}\varepsilon_{\mathrm{s}}}{\varepsilon_{\mathrm{ln}}}\right)^2 + \frac{2\varepsilon_{\mathrm{s}} V_{\mathrm{d}}}{qN_{\mathrm{dn}}}} - \frac{t_{\mathrm{ln}}\varepsilon_{\mathrm{s}}}{\varepsilon_{\mathrm{ln}}} \tag{19}$$

When $W_{\mathrm{ver}} = t_{\mathrm{sn}}$, the vertical depletion voltage is given by (20).

$$V_{\mathrm{ver}} = \frac{qN_{\mathrm{dn}} t_{\mathrm{n}}^2}{\varepsilon_{\mathrm{s}}} = V_{\mathrm{d}} \tag{20}$$

At the points of potential breakdown, $E(x, y) = E_{\mathrm{C}}$ is substituted into equation (12), (13) and (17) to obtain the BV at each point, and the actual BV of the device is determined by the minimum of these values.

A. MODEL FOR SBOSOI FROM THE UNIFIED ELECTRIC FIELD MODULATION MODEL WITH THREE REGIONS

As shown in the Fig. 3, the drift is divided into three regions because of the difference in the thickness of the buried layer. The SBOSOI structure has a discontinuous charge distribution at the step position, which causes a new electric field peak at the stepped position on the surface of the drift region, so that the electric field distribution on the surface of the drift region is more uniform, and the BV is increased, which is the modulation result of the step buried layer electric field on the surface electric field [25].

When modeling the SBOSOI structure according to the unified numerical model, due to the difference in the thickness of the buried layer, the drift is divided into three regions based on the difference, as shown in Fig. 3, the buried layer thickness in region I is t_{l1}, in II is t_{l2}, in III is t_{l3}. Substituting n = 3 into the unified model. The main parameters are the thickness of the drift region t_s, the length of the drift region L_3, and the length of I, II, III region L_1, $(L_2 - L_1)$, and $(L_3 - L_2)$. Based on the unified model, getting the boundary conditions that meet the SBOSOI structure, and other related conditions, which are substituted into the unified model. Through empirical calculations, the detailed 2-D numerical model of the SBOSOI structure is obtained.

B. MODEL FOR BODSSOI FROM THE UNIFIED ELECTRIC FIELD MODULATION MODEL WITH THREE REGIONS

As shown in the Fig. 4, due to the difference in thickness of the drift region and the charge accumulation effect at the step, the drift is divided into three regions. The positive charge accumulation at the upper step and the negative charge accumulation at the lower step can further enhance the electric field of the step part. At the same time, the accumulation of the positive charge also acts as a shielding effect of the electric field against the local field. The BODSSOI structure obtained in this case can simultaneously optimize the lateral and vertical electric field distribution [26].

When modeling the BODSSOI structure based on the unified numerical model, the thickness of the drift region is different due to the change in the step of the buried layer, and the effect of charge accumulation at the step is also considered. Based on this, the drift is divided into three regions. As shown in Fig. 4, the thickness of the drift region in region I is t_{s1}, and the thickness of the drift region in regions II and III is t_{s2} and t_{s3}. In addition, its other main parameters are the thickness of the buried layer t_l, the length of the drift region is L_3, and the length of the I, II and III regions is L_1, $(L_2 - L_1)$ and $(L_3 - L_2)$. Substituting n = 3 into the unified model, and then based on the continuity of electrical displacement, electric field and electric potential at the boundary of different regions, the boundary conditions that meet the BODSSOI structure and other related conditions can be obtained. Through empirical calculation, the effective 2-D numerical model of BODSSOI detailed structure is got.

C. MODEL FOR BPSOI FROM THE UNIFIED ELECTRIC FIELD MODULATION MODEL WITH THREE REGIONS

As shown in the Fig. 5, a p-type buried layer with N_{p} doping concentration is buried in the substrate near the source, the middle part is a p-type substrate, and an SiO_2 layer is buried in the substrate near the drain end. According to the different buried layers, the drift is divided into three areas. This structure makes use of the additional electric field modulation

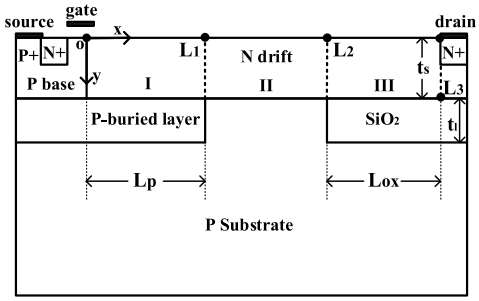

FIGURE 5. Cross-sectional view of BPSOI LDMOS.

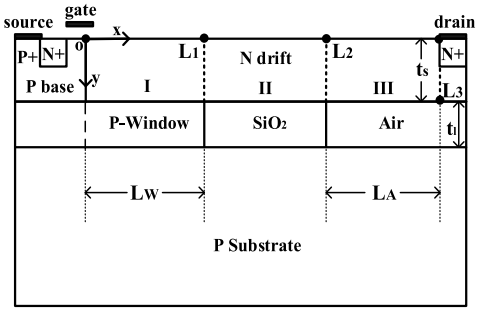

FIGURE 6. Cross-sectional view of APSOI LDMOS.

effect generated by the charge of the p-type buried layer, so that a new electric field peak appears in the surface electric field and tends to be uniform. Moreover, due to the electrical neutrality of the p-type buried layer, the drift region meets the RESURF condition at a higher concentration, ensuring a low specific on-resistance [27].

When modeling the BPSOI structure based on the unified numerical model, the drift region is divided into three regions according to the different materials at the buried layer. Substituting n = 3 into the unified model, the thickness of the drift region is t_s, the thickness of the buried layer is t_l. It should be noted that in the region of $0 \leq x \leq L_1$, we can understand that the substrate concentration in this region is N_p, and in the region of $L_1 \leq x \leq L_3$, the substrate concentration is N_t [28]. On this basis, according to the continuity of electrical displacement, electric field and electric potential at the boundary of different regions, the boundary conditions that meet the structural characteristics of BPSOI can be obtained, which can be substituted into the unified model to obtain the detailed 2-D analytical model of BPSOI structure.

D. MODEL FOR APSOI FROM THE UNIFIED ELECTRIC FIELD MODULATION MODEL WITH THREE REGIONS

As shown in the Fig. 6, the buried layer below the source is a silicon window and its same doped as doping concentration of the p-type substrate. The presence of silicon window provides a thermal conduction channel for the structure, which effectively alleviates the self-heating effect of the general SOI structure, reduces the temperature in the active region of the device, and improves the stability of the device [29]. The buried layer below the drain is the air gap with a dielectric constant of 1. Due to its low dielectric constant, the breakdown characteristic of the structure is optimized. In addition, with the buried SiO_2 layer under the drift region, the APSOI LDMOS is modulated by the buried layer with different dielectric constants to optimize the surface electric field distribution and improve the device performance.

When modeling the APSOI structure based on the unified numerical model, the drift region is divided into three regions according to the different materials at the buried layer. Substituting n = 3 into the unified model, with the thickness of drift region t_s and the thickness of buried layer t_1, and the boundary conditions and t_i conforming to the structural characteristics of the APSOI are combined to obtain a detailed 2-D analytical model of the APSOI structure [30].

III. RESULTS AND DISCUSSION

Through the MATLAB software, the SOI structure based on electric field modulation is modeled and analyzed, and the specific analytical results are obtained, and the simulation results obtained by simulating the same structural parameters in ISE TCAD software are compared and fitted. It is important to note that the analysis results in this section are all conducted under the conditions of $V_g = 0$ and $V_d = BV$. It can be seen that the fitting results of the two are highly consistent, which fully indicates that the unified model established for the SOI structure based on electric field modulation has extremely high universal adaptability and accuracy, and has great reference significance for the research and optimization of the SOI structure. Of course, what needs to be declared here is that the analytical model in this paper ignores the curvature of the electric field at the boundary during the calculation process, so the fitting results will have some slight errors in these places. In the following, the specific SOI structure based on electric field modulation in combination with the changes of key parameters is verified and analyzed.

A. MODEL VERIFICATION OF SBOSOI

From Fig. 7(a), it can be seen that the buried electric field distribution of the SBOSOI device has two electric field peaks at the position of the single-sided step compared with the conventional SOI structure. At the same time, modulated by the buried layer through the electric field modulation effect, as shown in Fig. 7(b), the electric field distribution on the surface of the drift region at the corresponding position also inspired new electric field peaks, and the peaks obvious. It effectively balances the surface electric field distribution, makes the surface electric field distribution of the device more uniform. Therefore, in Fig. 7(c), the BV is also improved. The BV of SBOSOI LDMOS is about 75% higher than that of traditional SOI LDMOS. These are all consistent with the analytical model.

It can be seen from the Fig. 8(a) that the position of the new electric field peak in the buried layer changes with the

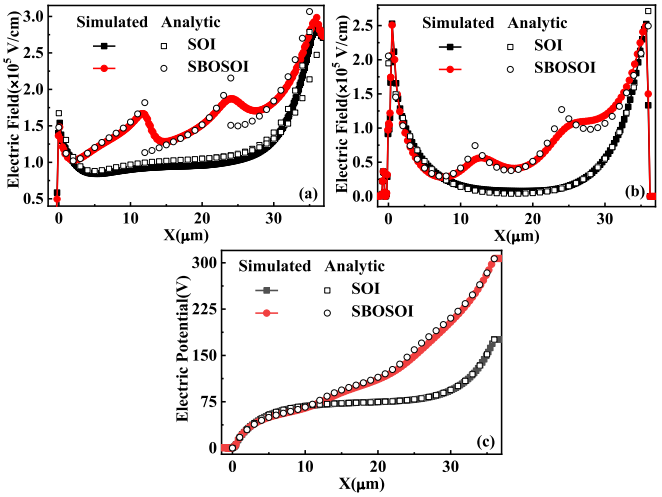

FIGURE 7. (a) Buried layer electric field distribution (b) Surface electric field distribution (c) Surface electric potential distribution (SOI: $N_d = 3.4 \times 10^{15}\text{cm}^{-3}$, $t_s = 2\mu\text{m}$, $t_1 = 2\mu\text{m}$, $L_3 = 36\mu\text{m}$, $BV = 175\text{V}$; SBOSOI: $N_d = 4.7 \times 10^{15}\text{cm}^{-3}$, $t_s = 2\mu\text{m}$, $t_{11} = 1\mu\text{m}$, $t_{12} = 2\mu\text{m}$, $t_{13} = 4\mu\text{m}$, $L_1 = 12\mu\text{m}$, $L_2 = 24\mu\text{m}$, $L_3 = 36\mu\text{m}$, $BV = 306\text{V}$).

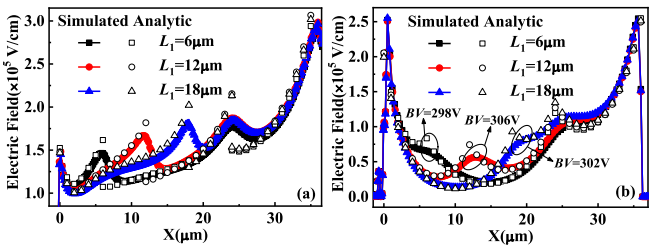

FIGURE 8. The performances of SBOSOI LDMOS under different L_1 (a) Buried layer electric field distribution (b) Surface electric field distribution.

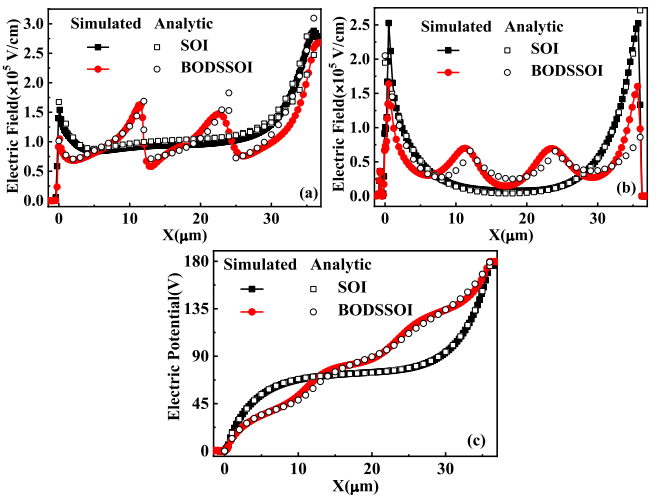

FIGURE 9. (a) Buried layer electric field distribution (b) Surface electric field distribution (c) Surface electric potential distribution (SOI: $N_d = 3.4 \times 10^{15}\text{cm}^{-3}$, $t_s = 2\mu\text{m}$, $t_1 = 2\mu\text{m}$, $L_3 = 36\mu\text{m}$, $BV = 175\text{V}$; BODSSOI: $N_d = 3.05 \times 10^{15}\text{cm}^{-3}$, $t_{s1} = 2\mu\text{m}$, $t_{s2} = 3\mu\text{m}$, $t_{s3} = 4\mu\text{m}$, $t_1 = 1\mu\text{m}$, $L_1 = 12\mu\text{m}$, $L_2 = 24\mu\text{m}$, $L_3 = 36\mu\text{m}$, $BV = 179\text{V}$).

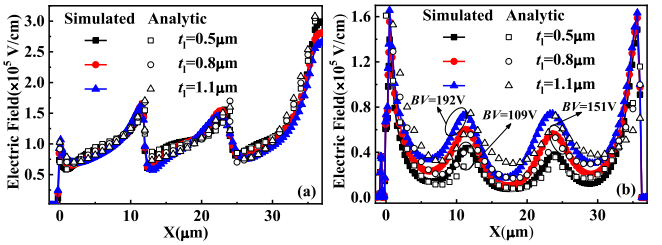

FIGURE 10. The performances of BODSSOI LDMOS under different t_1 (a) Buried layer electric field distribution (b) Surface electric field distribution.

step position, which is consistent with the expected results of the model. The position of the new electric field peak introduced by the electric field modulation of the buried layer electric field on the surface electric field of the drift region also moves with the step position of the buried layer, as shown in Fig. 8(b), which clearly demonstrates the role of electric field modulation effect. Also, in this set of data, when $L_1 = 12\mu\text{m}$, that is $L_1 = (L_2 - L_1) = 1/3L_3 = 12\mu\text{m}$, the BV of the device is the largest. Therefore, considering that the optimization effect of the electric field modulation effect on surface electric field is weakened when the step position is too close to the edge of the gate or the step on the right, the buried layer step position should keep a proper distance from the gate or the step on the right to fully reflect the advantage of the electric field modulation effect of the SBOSOI device.

B. MODEL VERIFICATION OF BODSSOI

In the BODSSOI, a large amount of positive charge accumulated at the step positions causes the space charge concentration to have high peaks at the position of the buried layer step, and leads to the change of electric field distribution in the position of the step, which affects the surface electric field with the effect of electric field modulation. Compared with the traditional SOI structure, as shown in Fig. 9(a), the buried layer electric field of BODSSOI device generates new electric field peaks at the position where the thickness of the drift region is abrupt. Under the modulation of the buried layer electric field, the new electric field peaks appear at the corresponding position in the surface electric field, as shown in Fig. 9(b), and the electric field modulation effect is enhanced at this point due to the large accumulation of charge at the stepped buried layer. As shown in Fig. 9(c), the BV of BODSSOI device is also increased due to more evenly surface electric field distribution. These are consistent with the model results.

As the model results show, it can be seen from the Fig. 10(a) that when the thickness of the buried layer is gradually increased, that is, the difference in the thickness of the drift region of the adjacent area is gradually increased, the electric field of the buried layer of the device does not change significantly, but the peaks of two new electric field peaks in the surface electric field at the step position of the buried layer increase gradually in the Fig. 10(b), making

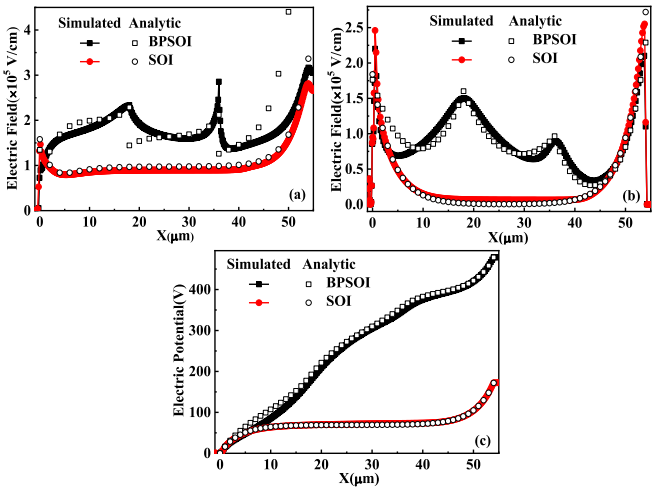

FIGURE 11. **(a) Buried layer electric field distribution (b) Surface electric field distribution (c) Surface electric potential distribution (BPSOI: $N_d = 5.3 \times 10^{15}cm^{-3}$, $t_s = 2\mu m$, $t_1 = 2\mu m$, $L_1 = 18\mu m$, $L_2 = 36\mu m$, $L_3 = 54\mu m$, $BV = 478V$; SOI: $N_d = 3.21 \times 10^{15}cm^{-3}$, $t_s = 2\mu m$, $t_1 = 2\mu m$, $L_1 = 18\mu m$, $L_2 = 36\mu m$, $L_3 = 54\mu m$, $BV = 171V$).**

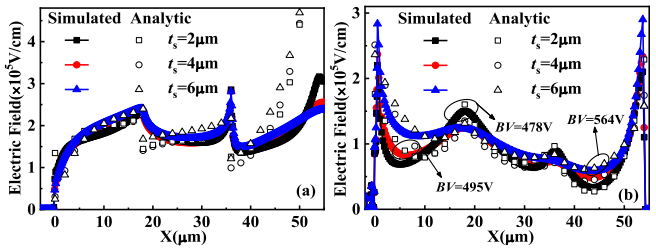

FIGURE 12. **The performances of BPSOI LDMOS under different t_s (a) Buried layer electric field distribution (b) Surface electric field distribution.**

the drift area more evenly distributed, and the breakdown voltage also increases.

C. MODEL VERIFICATION OF BPSOI

Fig. 11 shows the electric field and potential distributions for BPSOI and traditional SOI structures. The simulation results fit well with the model. As can be clearly seen from Fig. 11(a), the buried layer electric field of the BPSOI structure has new electric field peaks at the interface of different types of buried layer compared to the SOI structure. Meanwhile, as shown in Fig. 11(b), under the modulation effect of buried layer electric field, the surface electric field of BPSOI structure introduces new electric field peak in the corresponding position, so that the surface electric field distribution is more uniform than that of the traditional SOI structure, which leads to the increase of *BV*. As shown in Fig. 11(c), the *BV* increases from 171V of the conventional SOI to 478V of the BPSOI.

When $L_{ox} = L_p = 1/3L_3$, the influence of t_s on the electric field distribution of BPSOI structure can be seen in Fig. 12. From the expression of buried layer electric field of the Fig. 12(a), it can be seen that the peak changes of buried layer electric field are small during the gradual increase

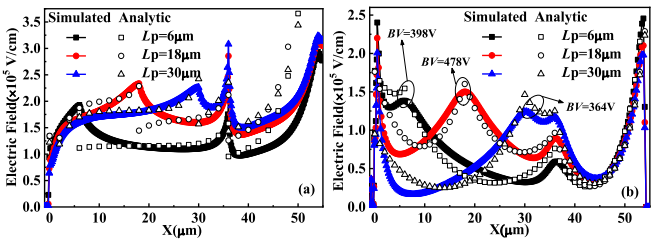

FIGURE 13. **The performances of BPSOI LDMOS under different L_p (a) Buried layer electric field distribution (b) Surface electric field distribution.**

of t_s. However, in the surface electric field, the peak values of the new electric field peaks at the different buried layer interface gradually becomes lower and less obvious, as shown in Fig. 12(b). This is because with the increase of t_s, under the influence of shielding effect, the electric field modulation is gradually weakened. The breakdown voltage increases with the increase of the valley value of the surface electric field in Fig. 12(b). However, it can also be seen from the Fig. 12 that an appropriate thinner drift region thickness is required in the application of electric field modulation technology.

When $L_{ox} = 1/3L_3$, the effect of changes in L_p on the electric field distribution of BPSOI can be seen in Fig. 13. It can be seen from Fig. 13(a) that in the process of L_p increasing gradually, the position of the new electric field peak in the buried layer electric field at the interface of p-type buried layer/substrate varies from left to right. Based on the electric field modulation effect, the position of the new electric field peak in the corresponding position of the surface electric field is also changing from left to right, as shown in Fig. 13(b). We can also see from the Figure that in this case, when L_{ox} and L_p are 1/3 L_3 respectively, the *BV* of the BPSOI structure is the largest with 478V.

D. MODEL VERIFICATION OF APSOI

As shown is the electric field and electric potential distribution of the APSOI structure in the Fig. 14. Compared with the traditional SOI, the APSOI surface electric field distribution is more evenly, the *BV* is higher, and the device performance is better. This is because of the different buried layer of APSOI structure causes new electric field peaks to appear in the buried electric field in Fig. 14(a). At the same time, under the electric field modulation of the buried electric field, the drift region surface electric field also introduces new electric field peaks at the corresponding position, which causes the overall distribution more evenly in Fig. 14(b). In addition, due to the presence of silicon window and air gap buried layer, the self-heating effect can be further alleviated and the *BV* of the structure can be increased, so that the device performance can be further optimized. The *BV* increased from 172V of conventional SOI to 458V of APSOI in Fig. 14(c). And the simulation results are in good agreement with the analytical model in the Fig. 14.

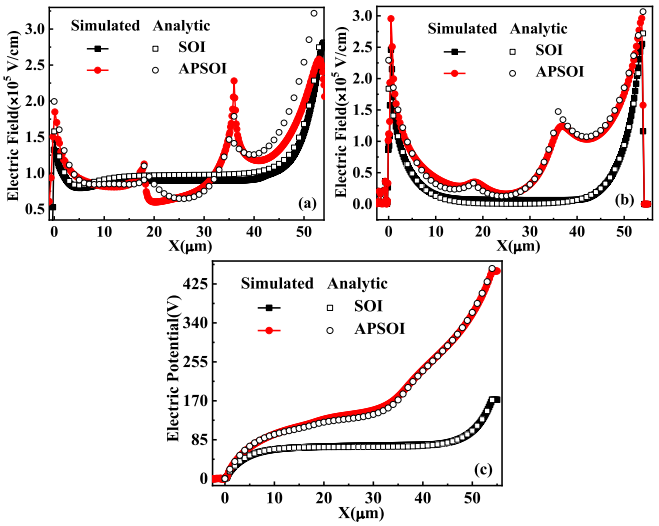

FIGURE 14. **(a) Buried layer electric field distribution (b) Surface electric field distribution (c) Surface electric potential distribution (SOI: $N_d = 3.2 \times 10^{15}cm^{-3}$, $t_s = 2\mu m$, $t_1 = 2\mu m$, $L_3 = 54\mu m$, $BV = 172V$; APSOI: $N_d = 2.4 \times 10^{15}cm^{-3}$, $t_s = 2\mu m$, $t_f = 2\mu m$, $L_1 = 18\mu m$, $L_2 = 36\mu m$, $L_3 = 54\mu m$, $BV = 458V$).**

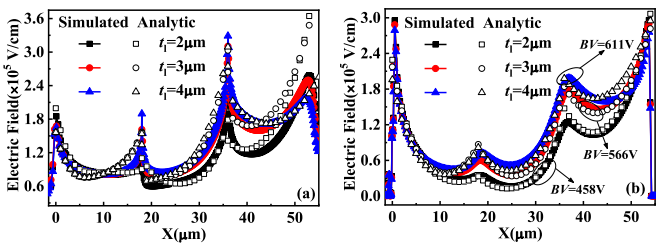

FIGURE 15. **The performances of APSOI LDMOS under different t_f (a) Buried layer electric field distribution (b) Surface electric field distribution.**

As shown in Fig. 15(a), the peak values of buried layer electric field increase with the increase of t_f. Meanwhile, under the effect of electric field modulation technology, as can be seen from the Fig. 15(b), the new peak values of surface electric field at the corresponding position also increase in the Figure, which further improves the valley value of surface electric field distribution, presents the overall uniformity, and increases the breakdown voltage. Also, as can be seen from the Figures, the analytical model is accurate, and its fitting effect with simulation results is excellent.

IV. CONCLUSION

Based on the existing research, this paper proposes a unified analytical model of SOI LDMOS based on electric field modulation. The electric field and potential distribution based on the electric field modulated SOI LDMOS are studied systematically, and the electric field modulation formula is proposed. The mechanism of surface electric field modulated and optimized by buried layer electric field is explained. Taking SBOSOI, BODSSOI, BPSOI, and APSOI as examples, combined with the characteristics of their respective structures, the analytical solutions of each structure is obtained by using the unified analytical model method. And in the case of ignoring the error caused by junction curvature, comparing the analytical solutions with the simulation results, the conclusion with good consistency is obtained. This verifies the feasibility of the electric field modulation theory, and also illustrates the universality of the unified analytical model. On this basis, the performance of the device is analyzed and optimized by changing the parameters, which once again demonstrates the effectiveness of the unified model, and the proposed unified analytical model has an important guiding significance for the design and optimization of the SOI LDMOS based on electric field modulation. When it is necessary to establish a 2-D numerical model for the electric field modulation SOI LDMOS, and if this buried layer of the structure has different doping concentrations, different thicknesses, different shapes or different materials, etc., the unified model proposed in this paper can provide strong support.

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BAOXING DUAN was born in Shaanxi, China, in 1977. He received the B.S. and M.S. degrees in material physics and chemistry from the Harbin University of Science and Technology, in 2000 and 2004, respectively, and the Ph.D. degree in microelectronics and solid-state electronics from the University of Electronic Science and Technology of China, in 2007.

He has been a Professor with the School of Microelectronics, Xidian University, Xi'an, China, since 2009. He has authored more than 50 papers. His research interests include new power semiconductor devices design and semiconductor devices physics.

JINGYU XING was born in Shanxi, China, in 1994. She received the B.S. degree from the North University of China in 2017. She is currently pursuing the M.S. degree in microelectronics and solid state electronics with Xidian University.

Her research interests include semiconductor devices physics and new power devices design based on Si materials.

ZIMING DONG received the B.S. degree from the North University of China in 2014, and the M.S. degree from Xidian University in 2017, where he is currently pursuing the Ph.D. degree in microelectronics and solid-state electronics.

His research interests include the new power devices design and power integration technology based on Si materials.

YINTANG YANG (Senior Member, IEEE) was born in Hebei, China, in 1962. He received the B.S. and M.S. degrees in microelectronics and solid-state electronics from Xidian University, Xi'an, China, in 1982 and 1984, respectively, and the Ph.D. degree in electronic science and technology from Xi'an Jiaotong University, in 1987.

He has been a Professor with the School of Microelectronics, Xidian University since 1997. He has authored more than 180 scientific papers in the related fields. His research interests include semiconductor materials, devices, and systems.

Prof. Yang is a winner of the National Science Foundation for Distinguished Young Scholars of China. In 2010, he has been invited as a General Chair for the International Conference on Electronic Packaging Technology and High-Density Packaging.