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28-nm FD-SOI CMOS RF Figures of Merit Down to 4.2 K

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ABSTRACT This work presents a detailed RF characterization of 28-nm FD-SOI nMOSFETs at cryogenic temperatures down to 4.2 K. Two main RF Figures of Merit (FoMs), i.e., current-gain cutoff frequency (f_t) and maximum oscillation frequency (f_{max}), as well as parasitic elements of the small-signal equivalent circuit, are extracted from the measured S-parameters. An improvement of up to ∼130 GHz in f_t and ∼75 GHz in f_{max} is observed for the shortest device (25 nm) at low temperature. The behavior of RF FoMs versus temperature is discussed in terms of small-signal equivalent circuit elements, both intrinsic and extrinsic (parasitics). This study suggests 28-nm FD-SOI nMOSFETs as a good candidate for future cryogenic applications down to 4.2 K and clarifies the origin and limitations of the performance.

INDEX TERMS 28-nm FD-SOI, UTBB MOSFET, cryogenic CMOS, RF figures of merit, small-signal modeling, liquid helium temperature.

I. INTRODUCTION

Numerous studies focused on the cryogenic behavior of advanced CMOS technologies are mainly driven by the perspective of quantum computing applications [1]-[12]. Quantum computer operations are realized by quantum bits (or "qubits"), working at extremely low temperature, presently down to the mK range, while the control and read-out circuitry is to be placed in a close proximity to the qubits, typically at liquid-helium temperatures [2]. Bringing the front-end electronics and the qubits closer has several advantages in terms of scalability and latency [3]. However, the degree of scalability is limited by the total dissipated power that can be removed by the cooling system. The co-integration of the qubits and the peripheral electronics on the same substrate, the so-called quantum-integrated circuits, would be the following step in the quantum computing roadmap. Recent studies have already demonstrated silicon qubit operating above 1 K [4], [5]. With further engineering of qubits, it might be possible to increase the operating temperature of qubits to ∼4.2 K, therefore having the whole system operating at that temperature. This relatively higher operation temperature enables the use of a different and more efficient cooling system, therefore removing more heating power from the system. As more dissipated power would be allowed, it would boost scalability and ease the co-integration of qubits and the front-end electronics.

The ultra-thin body and buried oxide (UTBB) fully-depleted silicon-on-insulator (FD-SOI) CMOS platform is an outstanding platform for cryo-CMOS, thanks to its very low power consumption feature, large integration and very good analog and radiofrequency (RF) performances [13], [14], as required for qubit write and read operations. Furthermore, the back-gate bias is a useful knob in its ability to tune the power consumption, and adjust for process or temperature variations [15]. 28-nm FD-SOI CMOS is also a viable solution for quantum-integrated circuits as the implementation of qubits is compatible with this platform and just additionally requires a few non-standard process steps, like e-beam lithography [10], [11].

To enable cryo-CMOS, it is therefore essential to embed digital, analog and RF models in a process design kit in order to predict the MOSFETs performances and power dissipation at cryogenic temperatures as required for reliable circuit designs. This motivated several works [6]–[9] and [16]–[19] towards the analysis of advanced MOSFETs behavior at cryogenic temperatures. Those works widely addressed static parameters, such as short-channel effects, threshold voltage, subthreshold swing, etc. The influence of cryogenic temperature on 28-nm bulk and FD-SOI CMOS technologies with a main focus on analog parameters and modeling has been discussed in [7] and [9]. In [16] and [17], the above studies were completed by investigating the analog and RF figures of merit (FoMs) in 28-nm FD-SOI CMOS technology at temperatures down to 77 K. A strong improvement of both analog and RF FoMs was demonstrated [16], [17].

The present paper extends our previous work [18]. It is the continuation of our previous study [17] on the RF performances of 28-nm FD-SOI transistors down to 4.2 K, the liquid-helium temperature. The paper is organized as follow. First the experimental setup is detailed in Section II. A brief description of the measured FETs is given and the extraction procedure is explained. Then, in Section III, the extraction of the full small-signal equivalent circuit of UTBB MOSFETs, including both intrinsic and extrinsic parasitic elements, is presented. The temperature dependence of these parameters is discussed in details. Finally, an analysis on the RF FoMs of the FETs is provided.

II. EXPERIMENTAL DETAILS

Devices studied in this work originate from 28-nm FD-SOI CMOS process of ST Microelectronics [13]. N-channel MOSFETs under study feature a high-K metal gate stack and gate lengths (L_g) from 25 to 150 nm. The Si film, buried oxide (BOX) and the equivalent gate oxide thicknesses are 7, 25 and 1.3 nm, respectively. Studied nMOSFETs incorporate 60 fingers of 2 µm width, embedded in Ground-Signal-Ground (GSG) pads for RF characterization.

The FETs are measured from DC up to 67 GHz under saturation (V_{ds} = 0.6 and 1 V) and "cold" (V_{ds} = 0 V) conditions for different applied gate voltages (V_{gs}) down to liquid-helium temperature (4.2 K). The on-wafer setup consists of a LakeShore cryogenic probe station with a pair of GSG Picoprobe probes with 100 µm pitch and a 67 GHz PNA-X vector network analyzer. Several dies with the FETs and an impedance standard substrate (ISS) are placed inside the probe station. Liquid-helium or liquid-nitrogen is used to cool down the chuck and the inner part of the probe station. At each temperature, an off-wafer Short-Open-Load-Thru (SOLT) calibration is first performed with the ISS calkit that is at the same temperature as the samples. Then, the access parasitics are de-embedded by a dedicated open structure for each device that reproduces the interconnects upto the first metal layer. Therefore, the reference plane after de-embedding in this paper is at the first metal layer of the FETs. The Load standard resistance is measured at each temperature and its variation is found to be comparable to the variation of one Load standard (not necessarily a precision Load) to another. Its variation has therefore not been taken into account. By neglecting its variation during the calibration process, the worst deviation in the Load resistance measured with respect to the expected value of 50Ω leads to an error of maximum 5% in the extracted values of the small-signal equivalent circuit elements. Therefore, this simplification has a small impact on the extractions.

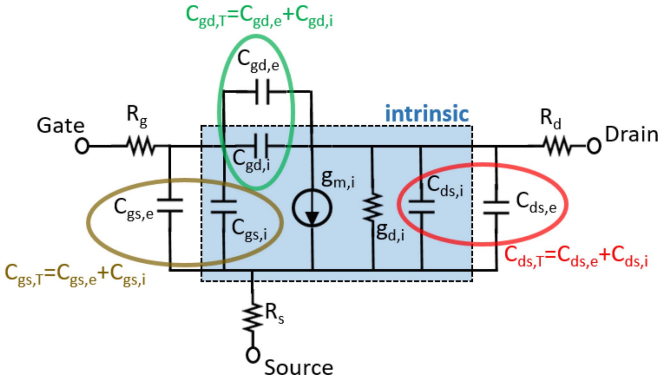

FIGURE 1. Small-signal equivalent circuit of the MOSFETs for this paper.

From the "cold" FET measurements, the extrinsic resistances are extracted employing the method from [20]. The extrinsic capacitances are also obtained from the "cold" FET condition in accumulation. Then, the intrinsic parameters are extracted at each bias point from the measurements in saturation, from which the effect of the extrinsic elements has already been subtracted. More details about the extraction methodology can be found in [14]. The small-signal equivalent circuit used in this paper is displayed in Fig. 1. The S-parameters measurements presented here are extracted for a bias condition of V_{ds} = 0.6 and 1 V and a V_{gs} corresponding to the peak transconductance ($g_{m,max}$). The back-gate is kept grounded. Each element of the small-signal equivalent circuit is extracted from an average over a frequency range, specific to the element, for a best fit of the S-parameters across all *relevant* frequencies. Almost all the elements are extracted below 5 GHz, except the gate resistance (R_g) and maximum oscillation frequency (f_{max}), which are extracted above 10 GHz. These two elements are therefore more sensitive to calibration accuracy. A more detailed description of the variation with frequency of different parameters is available in the Appendix. The upper bound of the *relevant* frequency range for the model fitting is determined by the calibration and de-embedding procedure. The lack of de-embedding structures and/or of on-wafer calibration structures limits the whole de-embedding accuracy over ∼20 GHz [21].

Another difficulty to be overcome is the quality of probing contacts at low temperature. A mediocre contact quality at the drain side mainly leads to inaccuracy in the source and drain resistances (R_{ds}) and $g_{m,i}$ extraction, while a bad contact quality at the gate side leads to wrong values of g_m, R_g,

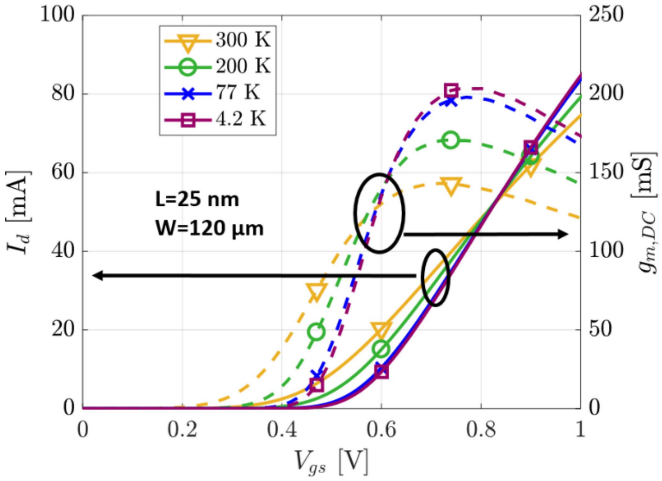

FIGURE 2. I_d (left) and $g_{m,DC}$ (right) for different V_{gs} from 300 K down to 4.2 K (V_{ds} = 1 V).

current-gain cutoff frequency (f_t) and f_{max}. Measurements were repeated several times, changing the probe position on the pad, to detect and if necessary replace outliers.

III. RESULTS AND DISCUSSION

This section presents the extracted small-signal equivalent circuit parameters and RF FoMs at different temperatures and for different devices. First, the effect of cryogenic temperatures on each parameter is discussed, then the behavior of f_t and f_{max} versus temperature is explained in terms of these observations.

A. DRAIN CURRENT AND TRANSCONDUCTANCE

Fig. 2 shows the drain current (I_d) and DC transconductance ($g_{m,DC}$) versus gate voltage (V_{gs}) for the shortest device (25 nm) for V_{ds} = 1 V. As expected, one can observe an increase of the threshold voltage, I_d and maximum $g_{m,DC}$ with temperature reduction. Furthermore, the zero temperature coefficient (ZTC) point at which I_d stays invariable with temperature (T) clearly appears at ~0.83 V. It is also interesting to notice that the V_{gs} yielding $g_{m,max}$ follows the threshold voltage (V_{th}) dependence with temperature, such that the overdrive voltage remains constant across temperature for each device.

Due to the power dissipated in the MOSFET, the channel temperature of the measured devices is not as low as the ambient temperature of its surroundings. Therefore, the curves showing small-signal parameters varying with temperature are referenced to the ambient temperature. Their study referenced to the channel temperature of the device would require a systematic study of self-heating effect [22] and is out of scope of this paper. Nevertheless, an estimation of the channel temperature for different devices is provided in Table 1, along with the dissipated power (P_{dc}), at an ambient temperature of 4.2 K. These estimations are computed based on the thermal resistance extracted at an ambient temperature of 77 K from [22]. The thermal resistivity of

TABLE 1. Dissipated power (P_{dc}) and estimated channel temperature at the two studied bias points: V_{ds} = 0.6 and 1 V and V_{gs} yielding $g_{m,max}$ at an ambient temperature of 4.2 K.

Gate length [nm]	P_{dc} [mW]		Channel temperature [K]	
	V_{ds} = 0.6 V	V_{ds} = 1 V	V_{ds} = 0.6 V	V_{ds} = 1 V
25	20.7	41.2	34.2	63.9
30	19.5	38.4	36.9	68.5
35	20.04	38.4	30.9	55.4
45	20.34	37.7	37.4	65.8

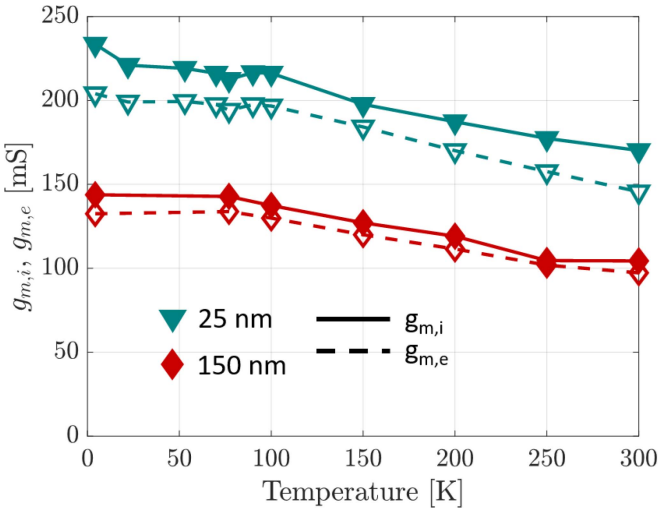

FIGURE 3. Maximum $g_{m,i}$ and $g_{m,e}$ extracted from RF measurements (V_{ds} = 1 V).

doped silicon and dielectrics are known to increase with temperature reduction below 77 K [23], [24]. Therefore, those estimations represent a lower boundary of the actual channel temperature in each device.

The maximum g_m (from S-parameters) versus temperature behavior is further detailed in Fig. 3. Both the "extrinsic" transconductance, $g_{m,e}$ (i.e., as measured) and the "intrinsic" one, $g_{m,i}$ (i.e., when parasitics are withdrawn using RF extraction) are shown. For all device lengths, g_m increases by ~40% with temperature lowering down to 4.2 K (see Fig. 4), mainly thanks to an increased mobility. As observed in Fig. 3, below 100 K, the increase in g_m is attenuated. A small local drop is observed at 77 K and a larger increase at 4.2 K in $g_{m,i}$ for the 25 nm-long FET. Those two local singularities are relatively small and might fall within the measurement uncertainty, despite being repeatedly observed. This needs more investigation in the 4.2 to 90 K temperature range.

From 300 K to ~100 K, the strong enhancement in mobility (μ) is due to a reduced phonon scattering, dominant in this temperature range. Then, as T decreases below 100 K, a concurrent μ mechanism, associated with impurity scattering (in the source and drain junctions and extension regions) and known to feature a μ reduction with T lowering, comes into a play [17]. Remarkably, the maximum $g_{m,e}$ and $g_{m,DC}$ are very close. The difference between $g_{m,i}$ and $g_{m,e}$ is mainly due to the source and drain resistances. The stronger discrepancy observed for the shortest device compared to

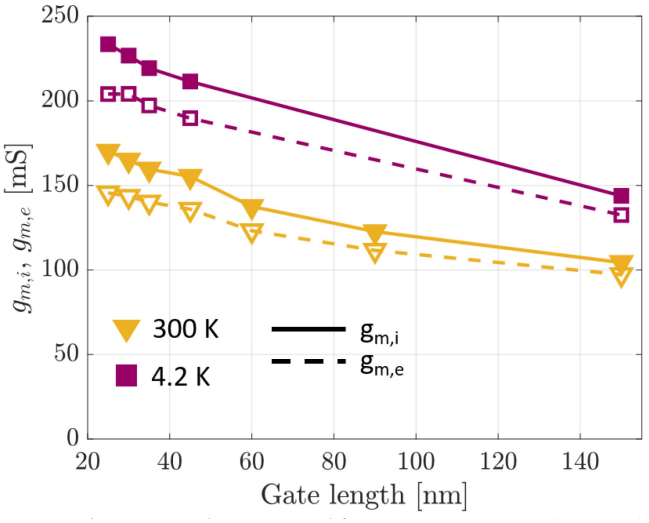

FIGURE 4. Maximum $g_{m,i}$ and $g_{m,e}$ extracted from RF measurements (V_{ds} = 1 V).

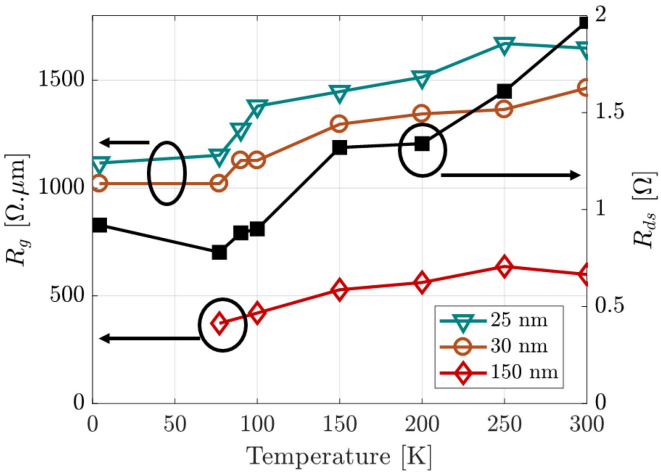

FIGURE 5. Extrinsic R_g (left) at different T for three gate lengths (25 nm in 'v', 30 nm in 'o' and 150 nm in 'd'). Extrinsic R_{ds} (right) at different T for the 30 nm-long FET in black line ('s').

the longest one is explained by a larger drive current in the 25 nm-long FET implying a larger voltage drop across similar R_{ds} and hence a slightly different bias point for the intrinsic device part.

B. EXTRINSIC RESISTANCES

Fig. 5 shows the total source and drain resistance behavior versus T for the 30 nm-long FET. R_{ds} accounts for the resistive behavior of the source and drain regions across materials with different properties (S/D extensions, heavily doped regions, silicidation) having different temperature dependences. Indeed, in doped silicon, the mobility degradation due to Coulomb effect is related to the doping level [25]. Therefore, the extensions and the highly-doped Source/Drain (S/D) regions can have a very different behavior versus temperature due to significantly different doping levels. Furthermore, the resistivity of NiSi (present in the silicidation) is known to decrease at lower temperature and to stabilize below 50 K [26].

Therefore, as all these effects come into a play together, it is difficult to identify the separate contribution of each device region to the total R_{ds} behavior versus T from the measured transistors. The global trend in R_{ds} displayed in Fig. 5 is observed for all the FETs. The strong decrease down to 77 K can be explained by the reduced phonon scattering in the Si S/D and extensions regions and decreased resistivity of the silicided contacts. Below 77 K, the apparent increase could be related to a stronger Coulomb scattering in the highly-doped S/D regions.

Fig. 5 also shows the R_g behavior versus T for different device lengths. A monotonic decrease of ∼30% with temperature lowering is observed down to 70 K, then the value stabilizes. Such a trend is in agreement with the TiN resistivity behavior at cryogenic temperatures reported in [27]. Therefore, this decrease in R_g is explained by two phenomena: (i) a lowered resistivity of the metal gate and (ii) an enhanced mobility in the polysilicon due to reduced phonon scattering. The value of R_g at 4.2 K of the longest device (150 nm) is not shown, because the accuracy of the S-parameters of that measurement was degraded above 10 GHz.

C. EXTRINSIC AND INTRINSIC CAPACITANCES

Figs. 6 and 7 display the extrinsic ($C_{gg,e}$) and intrinsic ($C_{gg,i}$) gate capacitances for different device lengths. The capacitances are extracted from an average over the 1.5 – 5 GHz frequency range. From repeated measurements of the same devices at the same temperatures, the error on the extrinsic gate capacitance extraction is estimated to be about ±1 fF. For the total gate capacitance ($C_{gg,T} = C_{gd,e} + C_{gs,e} + C_{gd,i} + C_{gs,i}$, including both extrinsic and intrinsic contributions), the error is estimated to be as large as ±7 fF. For the intrinsic capacitance extraction, the error is therefore about ±8 fF, since it is computed as the difference between $C_{gg,T}$ and $C_{gg,e}$. This surprisingly large difference between the error on $C_{gg,e}$ and $C_{gg,T}$ might be related to a stronger sensitivity of measured S-parameters to the probing contact quality when the FET is working in strong inversion and saturation rather than in cold and accumulation regime.

Despite the extraction uncertainty, Fig. 6 shows a decreasing trend of the extrinsic gate capacitance as the temperature goes down for all devices. The general trend of the intrinsic capacitance is less obvious as displayed in Fig. 7. $C_{gg,i}$ remains globally constant with a larger variation compared to the extrinsic capacitance. Fig. 8 shows the total gate capacitance variation with respect to temperature. A slight decrease of a few fF is observed at cryogenic T for the shortest devices in which the extrinsic capacitance dominates. Fig. 9 shows the extrinsic and intrinsic contributions of the gate capacitance versus gate length at room (300 K) and cryogenic (4.2 K) temperatures. As the device dimensions shrink, the extrinsic contribution dominates and does

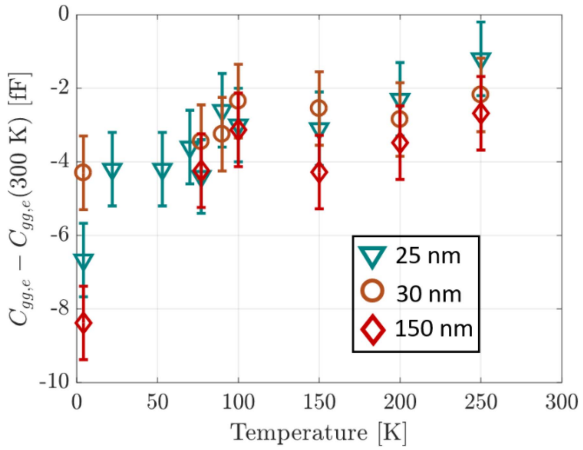

FIGURE 6. Extrinsic gate capacitance ($C_{gg,e} = C_{gd,e} + C_{gs,e}$) versus temperature normalized at 300 K, for three gate lengths (25 nm in 'v', 30 nm in 'o' and 150 nm in 'd') from measurements (symbols) and the error bars with an estimated uncertainty of ±1 fF. The extrinsic capacitances are extracted in "cold" FET operation, in accumulation ($V_{ds} = 0$ V, $V_{gs} = -0.2$ V).

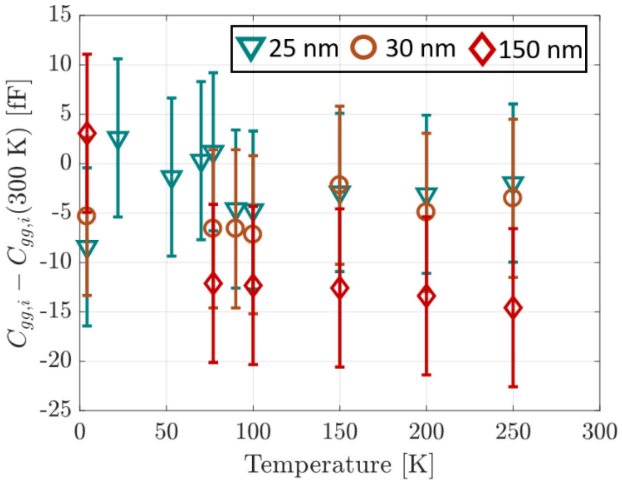

FIGURE 7. Intrinsic gate capacitance ($C_{gg,i} = C_{gd,i} + C_{gs,i}$) versus temperature normalized at 300 K, for three gate lengths (25 nm in 'v', 30 nm in 'o' and 150 nm in 'd') and the error bars with an estimated uncertainty of ±8 fF, at $V_{ds} = 1$ V and V_{gs} corresponding to $g_{m,max}$.

not scale as well as L_g. This effect partially explains the slower increase or even saturation of f_t with respect to the gate length independently from temperature (see Fig. 13).

D. OUTPUT CONDUCTANCE AND VOLTAGE GAIN

Fig. 10 and 11 shows the variation of the intrinsic ($g_{d,i}$) and extrinsic ($g_{d,e}$) output conductance and the voltage gain (A_v) versus temperature. The voltage gain A_v is an analog FoM of transistors and is computed as the ratio of the extrinsic g_m and g_d (i.e., $g_{m,e}/g_{d,e}$), both taken from S-parameters measurements and including the effect of the series resistances. Both $g_{d,i}$ and $g_{d,e}$ are stable above 150 K, then exhibit a steadily increase down to 4.2 K. They follow the same trend with an offset that depends on R_{ds}, similarly to the transconductance. A_v, dominated by $g_{m,e}$, follows the opposite trend with a slight increase in the temperature range from 300 K

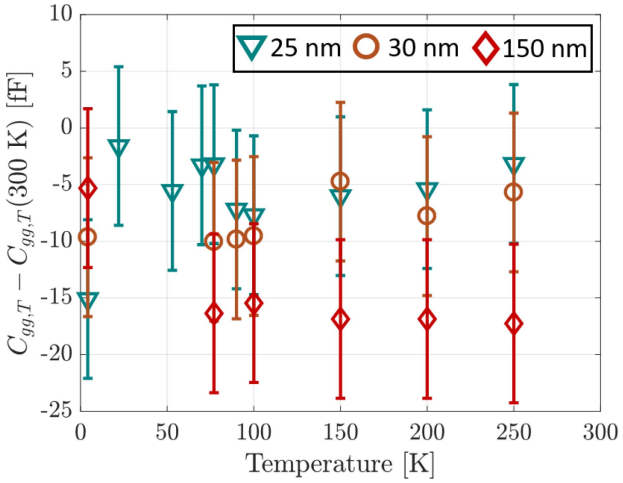

FIGURE 8. Total gate capacitances ($C_{gg,T} = C_{gg,i} + C_{gg,e}$) versus temperature normalized to the values at 300 K, for three gate lengths (25 nm in 'v', 30 nm in 'o' and 150 nm in 'd') and the error bars with an estimated uncertainty of ±7 fF, at $V_{ds} = 1$ V and V_{gs} corresponding to $g_{m,max}$.

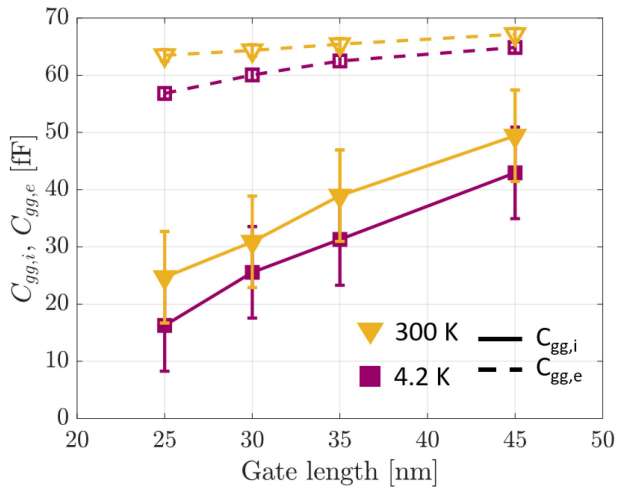

FIGURE 9. Extrinsic (dashed lines) and intrinsic (solid lines) C_{gg} versus gate length at 4.2 ('v') and 300 K ('s'). The intrinsic capacitances are extracted at $V_{ds} = 1$ V and V_{gs} corresponding to $g_{m,max}$. The error bars for both the intrinsic and extrinsic components are present too. The uncertainty in $C_{gg,i}$ is about ±8 fF, while for $C_{gg,e}$ it is about ±1 fF, which is too small to be visible in the figure.

down to 150 K and then stabilizes. Fig. 12 displays $g_{d,e}$ and A_v versus gate length at room (300 K, yellow) and cryogenic temperatures (4.2 K, purple). As expected, $g_{d,e}$ increases dramatically in shorter devices compared to the longest ones due to short-channel effect. $g_{d,e}$ increases by 20-25% for the shortest devices and only by ∼10% in the longest one as the temperature moves from 300 K to 4.2 K. Nevertheless, the voltage gain is still improved by 1-1.7 dB (depending on the length), because the $g_{m,e}$ increase is much stronger than the $g_{d,e}$ degradation.

E. RF FoMS

The cutoff frequency and maximum oscillation frequency, the two main RF figures of merit, are extracted from the

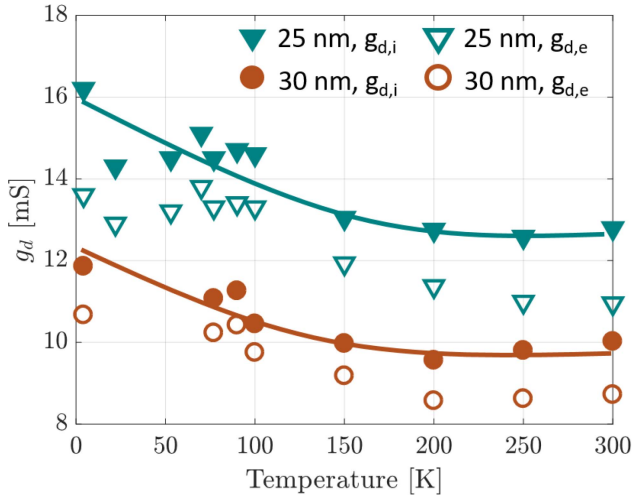

FIGURE 10. $g_{d,i}$ (solid line, filled markers) and $g_{d,e}$ (empty markers) versus temperature for 25 ('v') and 30 nm-long devices ('o'), at V_{ds} = 1 V and V_{gs} corresponding to $g_{m,max}$.

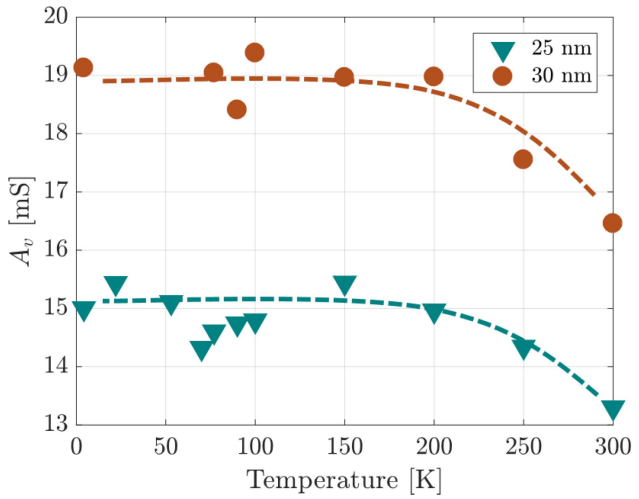

FIGURE 11. A_v versus temperature for 25 ('v') and 30 nm-long devices ('o'), at V_{ds} = 1 V and V_{gs} corresponding to $g_{m,max}$.

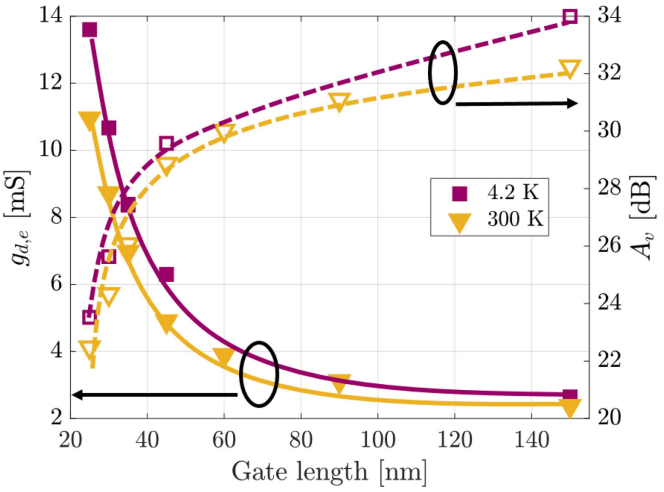

FIGURE 12. $g_{d,e}$ (solid lines, left) and A_v (dashed lines, right) versus gate length at 4.2 K ('s') and 300 K ('v'), at V_{ds} = 1 V and V_{gs} corresponding to $g_{m,max}$.

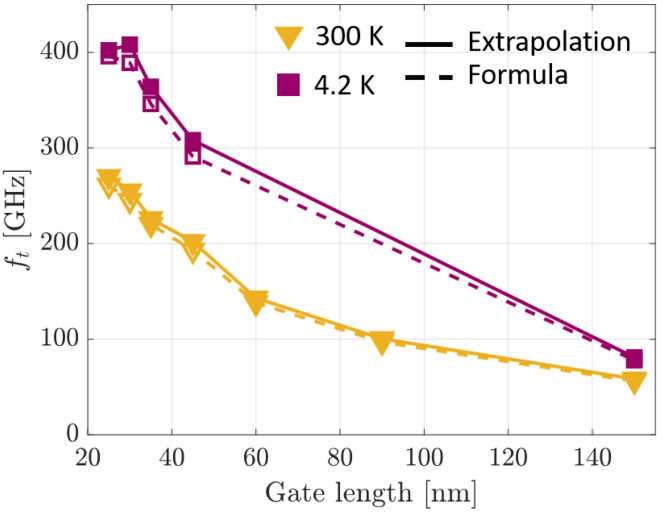

FIGURE 13. f_t extracted from extrapolation (solid lines) and (1) in dashed lines at 300 K ('s') and 4.2 K ('v') for different device lengths, at V_{ds} = 1 V and V_{gs} corresponding to $g_{m,max}$.

extrapolation to unity of the H_{21} (short circuit current-gain) and the U (Mason's gain or unilateral power gain), respectively. The extrapolation uses a −20 dB/dec slope, which interpolates either H_{21} or U from 1 to 20 GHz. Knowing the small-signal equivalent circuit elements, analytical expressions of f_t and f_{max} are used to assess the consistency of the extraction procedure. The variation of these two FoMs with respect to temperature and device length is displayed in Figs. 13-16 at a bias point of V_{ds} = 1 V and V_{gs} corresponding to $g_{m,max}$. The data resulting from the gains extrapolation are in solid line while the dashed lines show the values obtained from the analytical expressions in (1) and (2), using the extracted parameters that were discussed in the previous section [14], [28].

$$f_t \approx \frac{g_{m,e}}{2\pi C_{gs,T}\left[1+\frac{C_{gd,T}}{C_{gs,T}}+R_{ds}\left(\frac{C_{gd,T}}{C_{gs,T}}\left(g_{m,e}+g_{d,e}\right)+g_{d,e}\right)\right]} \tag{1}$$

$$f_{max} \approx \frac{g_{m,e}\sqrt{1+g_{m,e}R_s+g_{d,e}R_{ds}}}{4\pi\left[\begin{array}{c} C_{gs,T}^2\left(R_g+R_s\right)g_{d,e}\left(1+g_{m,e}R_s\right)+C_{gd,T}^2 \\ \times\left[\left(R_g+R_d\right)\left(g_{m,e}+g_{d,e}\right)+\left(g_{m,e}+g_{d,e}\right)^2\left(2R_gR_s+R_gR_d+2R_sR_d\right)\right] \\ +C_{gs,T}C_{gd,T}\left[R_g\left(g_{m,e}+2g_{d,e}\right)+g_{m,e}g_{d,e}\left(5R_gR_s+3R_gR_d+2R_sR_d\right)\right. \\ \left.+g_{m,e}^2R_gR_s\right] \end{array}\right]} \tag{2}$$

Although more accurate, these expressions are a bit too complex to understand the separate contribution of each parameter to the f_t and f_{max}. Simplified, but commonly used expressions [14] are

$$f_t \approx \frac{g_{m,e}}{2\pi\left(C_{gs,T}+C_{gd,T}\right)}, \tag{3}$$

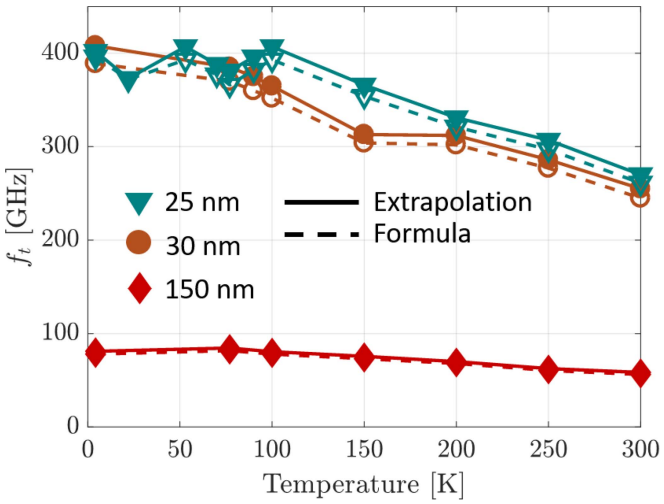

FIGURE 14. f_t extracted from extrapolation (solid lines) and (1) in dashed lines for the 25 nm-long ('v'), 30 nm-long ('o') and 150 nm-long ('d') devices at different temperatures, at $V_{ds} = 1$ V and V_{gs} corresponding to $g_{m,max}$.

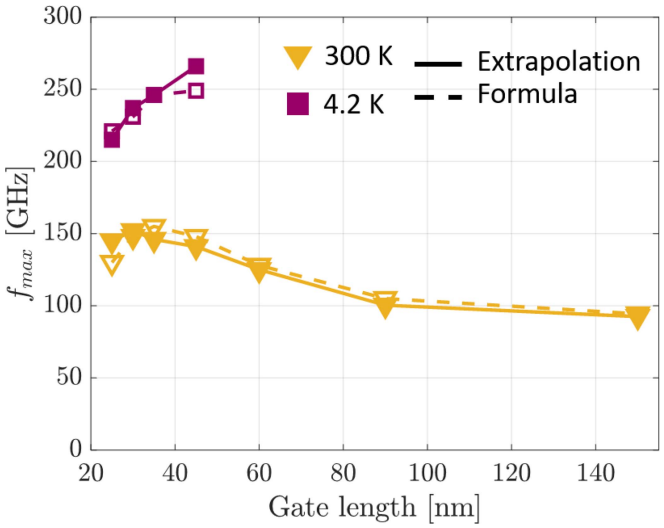

FIGURE 15. f_{max} extracted from extrapolation (solid lines) and (2) in dashed lines at 300 K ('s') and 4.2 K ('v') for different device lengths, at $V_{ds} = 1$ V and V_{gs} corresponding to $g_{m,max}$.

$$f_{max} \approx \frac{f_t}{2\sqrt{2\pi f_t R_g C_{gd,T} + (R_s + R_g) g_{d,e}}}. \quad (4)$$

As shown in Figs 13-16, the extrapolated data agree well with (1) and (2), which validates the extraction of the small-signal equivalent circuit elements. Furthermore, they are both affected by the same measurement errors as the small-signal equivalent circuit is extracted for each device at every temperature. This technology (28-nm FD-SOI CMOS) is known to have excellent RF performance with f_t and f_{max} of several hundreds GHz at room temperature. Overall, both f_t and f_{max} are improved at cryogenic temperatures. An increase by approximately 50% is observed in f_t for all the measured devices while f_{max} increases by more than 50% depending on the device length. The main reason for the f_t

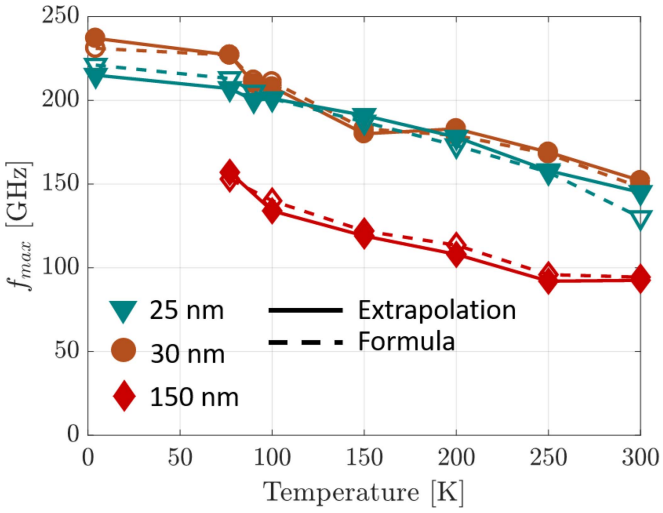

FIGURE 16. f_{max} extracted from extrapolation (solid lines) and (2) in dashed lines for the 25 nm-long ('v'), 30 nm-long ('o') and 150 nm-long ('d') devices at different temperatures, at $V_{ds} = 1$ V and V_{gs} corresponding to $g_{m,max}$.

improvement is related to the transconductance increase by 40% thanks to an enhanced mobility in the channel, whereas f_{max} benefits from both a higher g_m and a lower R_g (30%) at cryogenic T. The slight decrease in $C_{gg,T}$ for the shortest devices also contributes in a lesser extent to the larger f_t and f_{max}. Similarly to the g_m(T) trends observed in Fig. 3, the f_t increase slows down below 100 K and even saturates for the shortest device. The value of f_{max} at 4.2 K of the longest device (150 nm) is not shown in Fig. 15-17, because the accuracy of the S-parameters of that measurement was degraded above 10 GHz.

Fig. 17 shows the f_t and f_{max} of the different devices at room (300 K) and cryogenic (4.2 K) temperatures at a lower V_{ds} bias. $I_d - V_{ds}$ curves measured at different temperatures ensure that the devices are operating in saturation at $V_{ds} = 0.6$ V. Operating at lower V_{ds} reduces power dissipation (see Table 1) and thereby self-heating, which is a key concern for circuits aiming quantum computing as explained in the Introduction. Despite lesser performances (13-20% lower f_t and f_{max} according to the device length) compared to the nominal V_{ds} of 1 V, the devices still exhibit excellent RF FoMs, well above the values needed for quantum readout circuits [29], for a ~50% reduced power dissipation. All the trends discussed above about the small-signal equivalent circuit elements and RF FoMs behavior at cryogenic temperatures are also observed at $V_{ds} = 0.6$ V and will therefore not be further discussed here. Nevertheless, for a fair comparison of transistor operation at different bias conditions under cryogenic temperatures, it is of uppermost importance to take into account self-heating. As displayed in Table 1, working at a lower V_{ds} implies a reduced self-heating and thus channel temperature. It might therefore affect the intrinsic properties of the transistor and this effect is particularly pronounced at cryogenic temperatures, where the difference

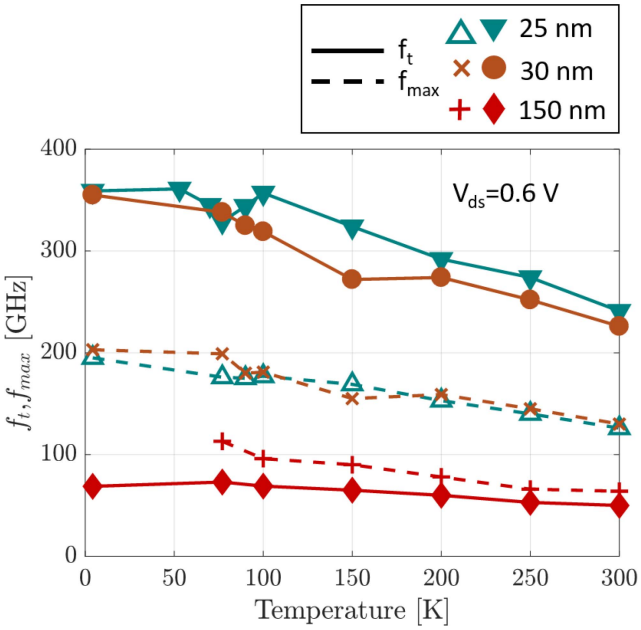

FIGURE 17. f_t (solid lines) and f_{max} (dashed lines) extracted from extrapolation from 300 K down to 4.2 K for the 25 nm (blue), 30 nm (brown) and 150 nm-long (red) devices at $V_{ds} = 0.6$ V and V_{gs} corresponding to $g_{m,max}$. The devices are still operating in saturation at $V_{ds} = 0.6$ V.

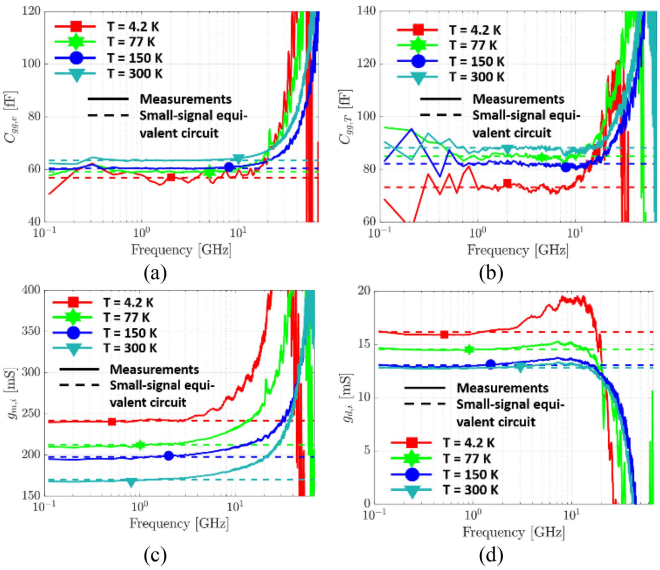

FIGURE A.1. Some parameters of the small-signal equivalent circuit versus frequency at different temperatures (4.2 K in 's', 77 K in 'h', 150 K in 'o', 300 K in 'v') for the shortest device (L = 25 nm) and at $V_{ds} = 1$ V and V_{gs} corresponding to the peak transconductance (except for the extrinsic gate capacitance in Fig. A.1(a) for which $V_{ds} = 0$ V and $V_{gs} = -0.2$ V). The extrinsic gate capacitance (a), total gate capacitance (b), intrinsic transconductance (c), intrinsic output conductance (d). In solid lines: measurements. In dashed lines: S-parameters reproduced by the small-signal equivalent circuit extracted from the model of Fig. 1.

in channel temperature for different bias conditions is in the same order of magnitude as the ambient temperature.

IV. CONCLUSION

In this work, the prospects of 28-nm FD-SOI CMOS for future cryogenic RF applications have been assessed by the analysis of RF FoMs and complete small-signal equivalent circuit elements in the cryogenic temperature range down to 4.2 K. The temperature reduction has been shown to result in a strong improvement of f_t (up to ∼130 GHz for 25 nm–long device) and f_{max} (∼75 GHz). The temperature evolution of the RF FoMs is mainly explained in terms of mobility enhancement (improvement of 40% in $g_{m,i}$) and gate resistance reduction (∼30%). This was supported by the fact that the reconstructed f_t and f_{max} based on the MOSFET small-signal equivalent circuit model agree well with those extracted by the extrapolation of current and unilateral power gains in the temperature range down to 4.2 K. A steady decrease in the extrinsic gate capacitance $C_{gg,e}$ is also observed, which leads to a reduced total gate capacitance that is more important in the shortest devices where the extrinsic contribution dominates. Finally, the RF FoMs for a lower V_{ds} of 0.6 V are also presented. Despite an overall reduction of approximately 13-20 % in f_t and f_{max}, compared to the nominal V_{ds} of 1 V, the devices are still operating incredibly well, exhibiting RF FoMs enabling their low-voltage low-power operation at RF and mm-wave frequencies.

APPENDIX
SMALL-SIGNAL PARAMETERS VERSUS FREQUENCY

As specified in Section II, each element of the small-signal equivalent circuit is extracted from an average over a frequency range, specific to the element, for a best fit of the S-parameters across all relevant frequencies. The different frequency ranges are explained by the fact that different phenomena affect each parameter in different ways. This is illustrated in Figs. A.1 and A.2 that show some parameters ($C_{gg,e}$, $C_{gg,T}$, $g_{m,i}$, $g_{d,i}$, H_{21} and U) of the small-signal equivalent circuit versus frequency. Both the measurements (solid lines) and the extractions (dashed lines) are shown. The curves from Figs. A.2(c) and (d) are common ways of calculating f_t and f_{max}, respectively, that are valid if H_{21} and U exhibit a −20 dB/dec slope as predicted by the small-signal equivalent circuit of Fig. 1. Deviations from this theoretical slope lead to non-flat curves in Figs. A.2(c) and (d).

The strong increases in $g_{m,i}$ and $g_{d,i}$ above several GHz are due to two phenomena: (i) the series inductances are not taken into account in the small-signal equivalent circuit (see Fig. 1), because their main contribution comes from the accesses, and (ii) a lack of de-embedding or on-wafer calibration (due to limitations in available de-embedding structures). That is why these parameters are extracted at lower frequencies (up to 3 GHz). On the contrary, U has a −20 dB/dec slope only at higher frequencies (above 10 GHz). The low frequency data is unsuited to the f_{max} extraction, because U is affected by dynamic self-heating effect and substrate effect.

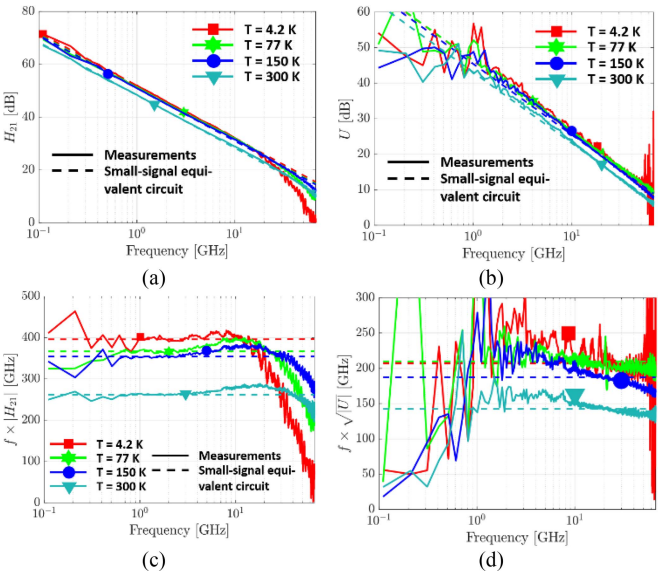

FIGURE A.2. RF FoMs versus frequency at different temperatures (4.2 K in 's', 77 K in 'h', 150 K in 'o', 300 K in 'v') for the shortest device (L = 25 nm) and at V_{ds} = 1 V and V_{gs} corresponding to the peak transconductance. The H_{21} (a), U (b). Figs. A.2(c) and (d) represent a common way f_t and f_{max} are respectively calculated. Flat curves in Figs. A.2(c) and (d) correspond to −20 dB/dec slopes in H_{21} and U, respectively, and is expected by the small-signal equivalent circuit. In solid lines: measurements. In dashed lines: S-parameters reproduced by the small-signal equivalent circuit extracted from the model of Fig. 1.

The gate capacitances (mainly $C_{gg,e}$) and H_{21} (from Fig. A.2(c)) curves give a good estimation of the calibration/de-embedding consistency at higher frequencies. A strong deviation from the theoretical curves (in dashed lines) is related to an unreliable calibration, which determines the upper bound of the relevant frequency range in which the model fitting is valid. As observed in Figs. A.1 and A.2, this upper bound lies around 20 GHz.

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