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SiC Planar MOSFETs With Built-In Reverse MOS-Channel Diode for Enhanced Performance

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ABSTRACT In this paper, the SiC planar MOSFET with built-in reverse MOS-channel diode (SiC MCD-MOSFET) is investigated utilizing TCAD simulation tools. When the device is working as a freewheeling diode, the operation of the parasitic body diode is suppressed effectively due to the lower threshold voltage of the MCD. Therefore, the bipolar degradation issue can be completely solved. In addition, the SiC MCD-MOSFET is featuring superior dynamic characteristics. The input capacitance (C_{ISS}), reverse transfer capacitance (C_{RSS}), gate charge (Q_{G}) and gate-to-drain charge (Q_{GD}) are reduced by a factor of $\sim$2, $\sim$7, $\sim$2 and $\sim$10, respectively, as compared to the conventional SiC MOSFET (SiC C-MOSFET). Combined with the slightly increased on-resistance (R_{ON}), tremendously enhanced figures of merit ($R_{\mathrm{ON}} \times Q_{\mathrm{G}}$ and $R_{\mathrm{ON}} \times Q_{\mathrm{GD}}$ are decreased by a factor of 1.8 and 9, respectively) are obtained in the SiC MCD-MOSFET. The outstanding performance and easy-to-implement feature make the SiC MCD-MOSFET more attractive for further power electronic applications.

INDEX TERMS SiC planar MOSFETs, bipolar degradation, dynamic performance.

I. INTRODUCTION

SiC MOSFETs are generally treated as a replacement of Si counterparts in power electronic applications, owing to the superior material properties [1]–[5]. In many applications, the source-drain diode inherently provided by the MOSFET, also referred to as the body diode, is always utilized as a freewheeling diode, such as in a voltage source inverter [6]. This is attractive since it enables the engineer to cut the number of power semiconductor components to half, thus significantly reducing the cost of the system. However, the parasitic body diode of a conventional SiC MOSFET (SiC C-MOSFET) is not suitable for use because of the following two reasons: one is the large knee voltage (nearly 3 V) due to the wide band gap property of SiC material [7], which would lead to a high conduction loss; the other is the bipolar degradation issue induced by the electron-hole recombination [8]. The basal plane dislocation (BPD) could gain energy from this recombination process. Consequently, the stacking faults grow into the N-drift region, resulting in a higher on-resistance (R_{ON}).

Some approaches have been reported to handle this problem so far. An external SiC Schottky barrier diode (SBD) anti-paralleled with the SiC MOSFET is a popular method [9], whereas the resulting introduction of extra capacitance and inductance is unexpected [10]. A SiC MOSFET with embedded SBD has been put forward to solve this issue [11], [12], which shows a better performance in terms of the switching characteristics and the bipolar degradation suppression. The DioMOS structure [13], [14], which enables the forward and reverse current to flow through the same accumulation channel, is another effective design. Lately, it comes to our attention that a Si-based power MOSFET with built-in channel diode has been proposed to enhance the reverse recovery performance of the device [15]. The channel diode is turned on in competition with the body diode under reverse operation mode, thus reducing the injected minority carriers in the drift region. However, the cut-in voltage of the body diode in Si devices is still small ($\sim$0.7 V), so it is difficult to prevent it from operating thoroughly, which may weaken the advantage of this design

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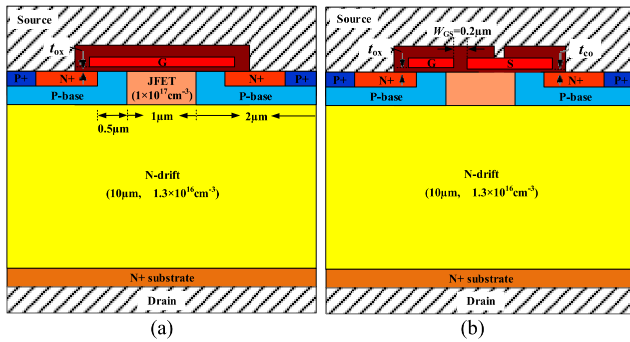

FIGURE 1. Schematic cross-sectional views of (a) SiC C-MOSFET and (b) SiC MCD-MOSFET.

concept. By comparison, this top cell design is more attractive in SiC devices, since the built-in voltage of PN junction is raised to about 3 V due to the wider band gap of SiC material. Our previous work has demonstrated its feasibility based on a double-trench MOSFET structure proposed by Rohm [16]. However, the process implementation of this device architecture is too complex and demanding, making it difficult to be introduced into the market.

In this paper, the easily achievable SiC planar MOSFET with built-in reverse MOS-channel diode (SiC MCD-MOSFET) is studied systematically by TCAD simulations. The dummy gate oxide thickness is thinned for a required turn-on voltage, so as to confine the injection level of the minority carriers from the body diode. As a result, the bipolar degradation can be removed completely when the device acts as a freewheeling diode. The superior performance with remarkably improved figures of merit can be obtained with respect to the SiC MCD-MOSFET, showing a significant advantage in high-frequency applications when compared to the SiC C-MOSFET. What's more, the influence of parameters variation on the device characteristics is addressed as well.

II. DEVICE STRUCTURES AND SIMULATION RESULTS

The schematic cross sections of the SiC C-MOSFET and MCD-MOSFET are illustrated in Fig. 1, respectively. The doping and dimension parameters used in the simulation refer to the design rules and already published research [17]. The thickness of the epitaxial layer is 10 μm with a doping concentration of 1.3×10^{16} cm^{-3} to achieve a breakdown voltage (BV) higher than 1200 V. The gate oxide thickness (t_{ox}) is 50 nm and the channel mobility is assumed to be 50 cm^2/V-s [18]. The doping concentration of the P-base and JFET area are both 1×10^{17} cm^{-3}. For the SiC MCD-MOSFET, the dummy gate oxide thickness (t_{co}) is thinner than t_{ox} to modulate the knee voltage of the MCD, and the distance between the true and dummy gate (W_{GS}) is set to be 0.2 μm. The SiC MCD-MOSFET can be realized in a similar fashion as the conventional one, with an additional lithography process to form a stepped oxide profile by dry etch after the oxidation procedure. The true gate and dummy

TABLE 1. Parameters of the impact ionization coefficients of 4H-SiC.

	Perpendicular to c-axis[19]	Parallel to c-axis[20]	Unit
a_e	2.1×10^7	8.19×10^9	cm^{-1}
b_e	1.7×10^7	3.94×10^7	V/cm
a_h	2.96×10^7	4.48×10^6	cm^{-1}
b_h	1.6×10^7	1.28×10^7	V/cm

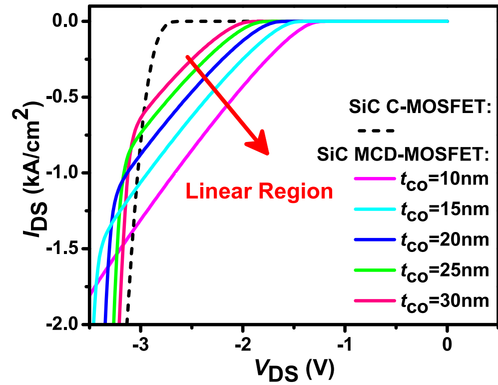

FIGURE 2. Conduction characteristics in the third quadrant for the studied MOSFETs.

gate can be separated incidentally in the subsequent etch process after the polysilicon deposition. Likewise, the contact via hole between the source metal and the dummy gate can be formed along with the formation of the source contact hole.

To simulate SiC-based power devices, the following models are essential: anisotropic avalanche model based on the Chynoweth law [19], [20] used only for breakdown voltage simulations, incomplete ionization of dopants in SiC material, Shockley-Read-Hall (SRH) recombination with doping dependency, bandgap narrowing [21]–[23]. The parameters of the electron- and hole-impact ionization coefficients of 4H-SiC used in the simulations are given in Table 1. The interface charge traps at SiC-SiO_2 interface are not considered in the simulations. It should also be noted that this simulation work is aimed at comparing the performance of two different structures on the same terms instead of revealing their features as physical devices. So the default model parameters for 4H-SiC material given by the simulation tool are employed, and the results are obtained based on rather idealistic assumptions.

The third quadrant characteristics of SiC C-MOSFET and MCD-MOSFET at $V_{GS} = -5$ V are plotted in Fig. 2, respectively. A steep on-state curve in the SiC C-MOSFET can be observed, indicating the turn-on of the parasitic body diode, whose knee voltage and voltage drop at $I_{SD} = 100$ A/cm^2 (V_F) are 2.7 V and 2.82 V, respectively. While in the SiC MCD-MOSFET, although the dummy gate and the P-base region both short-circuit the source metal, the potential of the P-base region is still lower than that of the dummy gate, as shown in Fig. 3 (a). Fig. 3 (b) presents the vertical potential profile along the dotted line. The perpendicular flow of the majority carriers (the holes) results in the abrupt

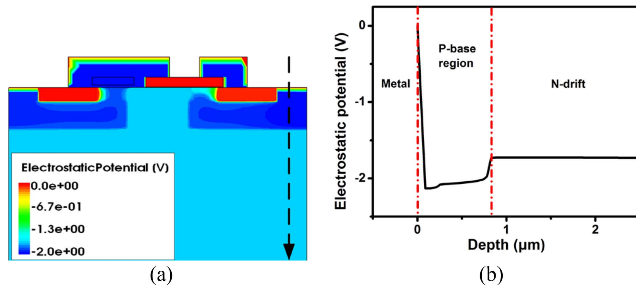

FIGURE 3. (a) Potential distribution of SiC MCD-MOSFET with t_{co} of 15 nm at I_{SD} = 100 A/cm^2. (b) Potential profile along the dotted line.

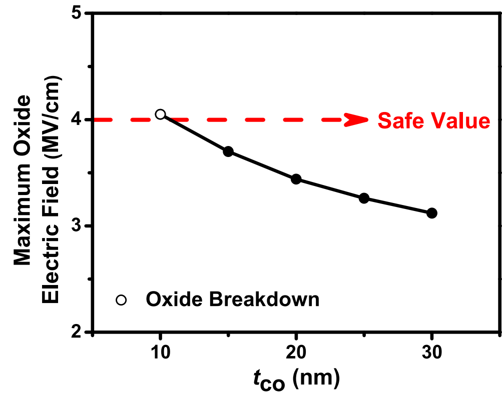

FIGURE 4. Maximum oxide field versus t_{co} at V_{DS} = 1200 V.

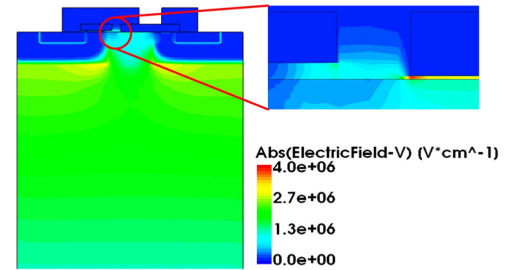

FIGURE 5. Electric field distribution at t_{co} = 10 nm and V_{DS} = 1200 V. The field strength around the left corner of the dummy gate is beyond 4 MV/cm.

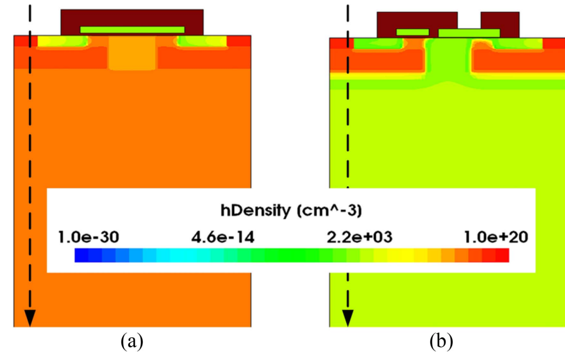

FIGURE 6. Hole density distributions at I_{SD} = 100 A/cm^2 for the (a) SiC C-MOSFET and (b) SiC MCD-MOSFET, respectively.

decrease of the potential near the surface of the semiconductor, thus bringing down the potential of the P-base region. Consequently, a strong inversion layer beneath the oxide can be formed to create a path for the current flowing from the source to the drain. In Fig. 2, a linear region can be found in regard to the SiC MCD-MOSFET with an I_{SD} lower than 500 A/cm^2, demonstrating the unipolar conduction of the MCD. The characteristic curves with certain values of t_{co} begin to steepen when I_{SD} is higher than 500 A/cm^2. It means that the body diode starts to conduct the reverse current together with the MCD, due to that the on-state voltage drop has already reached the threshold voltage of the body diode at this time. Moreover, it is shown that t_{co} plays a crucial role in adjusting the cut-in voltage of MCD. A lower cut-in voltage can be obtained with a smaller t_{co}, thus further restraining the operation of the body diode when carrying high-density current. However, this can also aggravate the electric field crowding in off-state. As shown in Fig. 4, when t_{co} = 10 nm, the maximum electric field in the oxide has already exceeded the safety limit 4 MV/cm at V_{DS} = 1200 V [24]. The corresponding electric field distribution plot can be found in Fig. 5, and the electric field crowing around the bottom corner of the dummy gate is clearly visible. It means that the oxide breakdown occurs, which may influence the long-term reliability of the device. As a result, unless otherwise specified, t_{co} = 15 nm is employed in the following discussions, and thus V_F = 1.75 V is obtained in the SiC MCD-MOSFET. The smaller V_F with comparison to that of the SiC C-MOSFET enables the device to save much more conduction losses when serving as a freewheeling diode.

Fig. 6 shows the hole density distributions at I_{SD} = 100 A/cm^2 for the SiC C-MOSFET and MCD-MOSFET, respectively. The profiles of minority carrier concentration along the dotted lines are exhibited in Fig. 7. The extremely low hole density in the N-drift region of the SiC MCD-MOSFET indicates that the turn-on of the body diode is restrained effectively. Therefore, the bipolar degradation can be completely eliminated when the device is acting as a freewheeling diode.

The reverse recovery characteristics of the studied MOSFETs are tested using the circuit in Fig. 8(a), and the reverse recovery performance at different turn-off current is reported in Fig. 8(b) for both cases, respectively. The reverse recovery charges Q_{RR} are nearly the same with respect to the SiC C-MOSFET and MCD-MOSFET at a turn-off current of 100 A/cm^2, although the bipolar conduction takes place in the former while unipolar conduction in the latter. This is because the injection level of the minority carriers is still not high enough at this moment, which is clearly visible from the hole density profile of the SiC C-MOSFET in Fig. 7. The hole concentration does not even reach the background doping of the N-drift region at I_{SD} = 100 A/cm^2. It seems that the Q_{RR} could not be reduced so much in the SiC MCD-MOSFET under that circumstance. However, the advantage of this MCD design becomes appreciable at

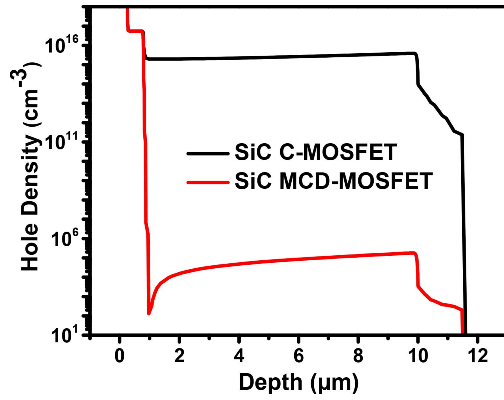

FIGURE 7. Hole density profiles along the depth of the studied MOSFETs at I_{SD} = 100 A/cm^2.

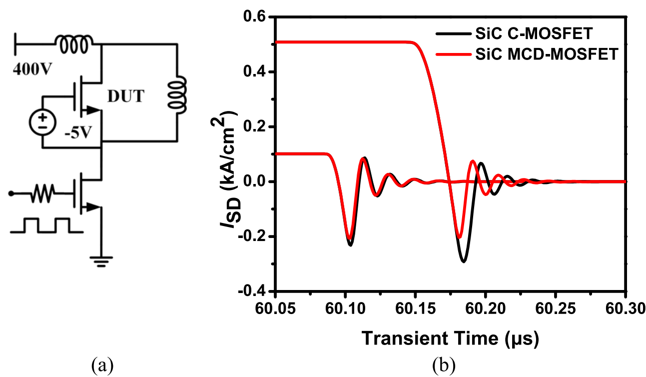

FIGURE 8. (a) Test circuit used for simulating the reverse recovery characteristics. (b) Reverse recovery performance at different turn-off current.

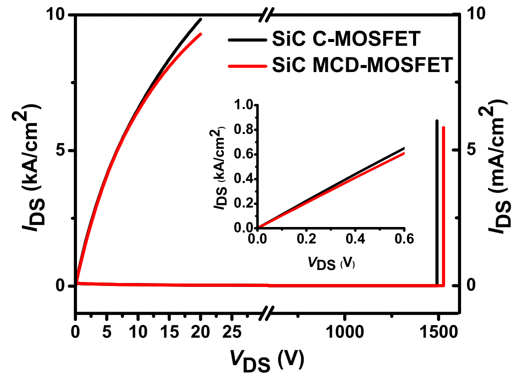

FIGURE 9. On-state and breakdown characteristics for the SiC C-MOSFET and SiC MCD-MOSFET, respectively.

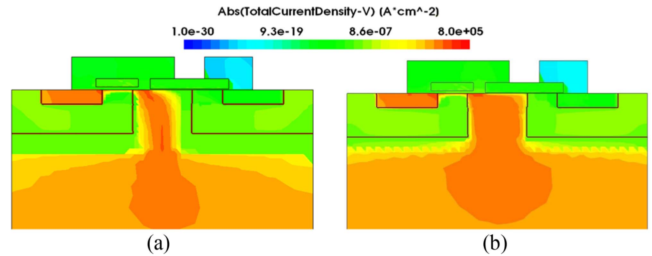

FIGURE 10. Total current density distributions at I_{DS} = 100 A/cm^2 for the SiC MCD-MOSFET (a) without JFET region and (b) with JFET region, respectively.

a high turn-off current, such as at I_{SD} = 500 A/cm^2 in Fig. 8(b). The epitaxial layer of the SiC C-MOSFET now is flooded with plasma, and more charges need to be removed when it is turned off, resulting in a higher Q_{RR} [25]. While in the case of SiC MCD-MOSFET, its Q_{RR} is not changed with that turn-off current, which is a unique feature for the unipolar devices. By calculation, the Q_{RR} of 3.28 μC/cm^2 is obtained in the SiC C-MOSFET, while 1.56 μC/cm^2 in the SiC MCD-MOSFET at a turn-off current of 500 A/cm^2, showing nearly a 50% improvement.

The performance of the SiC MCD-MOSFET working as a switching device is also studied. The on-state and breakdown characteristics for the SiC C-MOSFET and MCD-MOSFET are depicted in Fig. 9, respectively. The current carrying capability in the saturation regime is weakened in the SiC MCD-MOSFET because of the decreased channel density, which would help improving the short-circuit ruggedness of the devices [26]. However, no serious degradation can be observed in the linear region with comparison of the conventional one, as shown in the inner plot of Fig. 9. Consequently, the R_{ON} of the SiC C-MOSFET at I_{DS} = 100 A/cm^2 is 0.89 mΩ·cm^2 while 0.96 mΩ·cm^2 for the SiC MCD-MOSFET, only an 8% increase. On the one hand, the highly doped JFET region could help spread the current more evenly into the drift region, thus reducing the JFET resistance for both cases. According to our simulation results, if without the JFET region, the R_{ON} of SiC C-MOSFET is 2.5 mΩ·cm^2 while 90.7 mΩ·cm^2 for the SiC MCD-MOSFET, and the degradation becomes great. Obviously, the improvement on R_{ON} brought by the JFET area is more significant for the SiC MCD-MOSFET by comparison, since the dummy gate does not contribute to the current flow, as presented in Fig. 10. The other factor affecting the total on-resistance is the channel resistance, which is an important component of R_{ON}, especially in SiC-based MOSFET. The R_{ON} of the SiC C-MOSFET and MCD-MOSFET can grow to 1.1 mΩ·cm^2 and 1.3 mΩ·cm^2, respectively, thus in contrast a 20% increase, if a conservative value 10 cm^2/V-s of channel mobility is used. In brief, the introduction of JFET region and a high channel mobility both promote the on-state characteristic of SiC MCD-MOSFET. Furthermore, the SiC MCD-MOSFET has the same reverse blocking capability as that of the SiC C-MOSFET. It means that the segmented gate does not give rise to an electric crowding at the bottom of the oxide layer, which would be a threat to the long-term reliability of the devices.

Fig. 11 shows the *C-V* characteristics of the SiC C-MOSFET and MCD-MOSFET, respectively. The SiC MCD-MOSFET boasts a smaller input capacitance (C_{ISS}) and a much lower reverse transfer capacitance (C_{RSS}) as compared to the conventional one (C_{ISS} is reduced by half, while

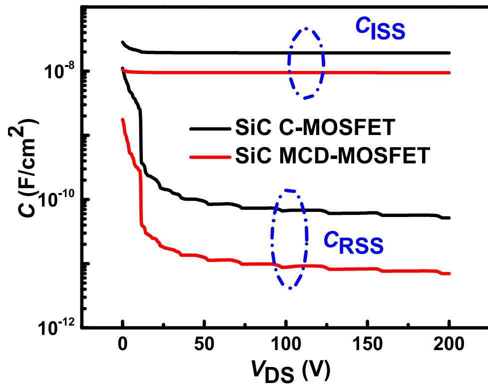

FIGURE 11. C-V characteristics of the SiC C-MOSFET and MCD-MOSFET, respectively.

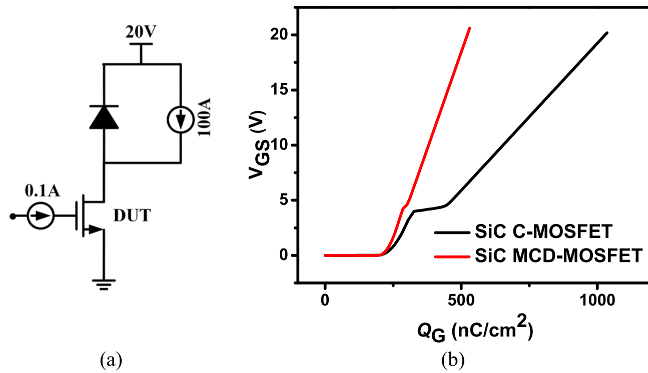

FIGURE 12. (a) Test circuit used for simulating the gate charge characteristics. (b) Gate charge characteristics for the studied MOSFETs.

C_{RSS} is lowered by up to 87%). It means that this top cell design could weaken the capacitive coupling between electrodes effectively due to the reduced area where the gate electrode overlaps the JFET region.

Fig. 12(a) shows the test circuit used to simulate the gate charge characteristics and the simulation results of both cases can be found in Fig. 12(b). The extracted gate charge Q_G at $V_{GS} = 20$ V and gate-to-drain charge Q_{GD} for the SiC C-MOSFET is 1037 nC/cm^2 and 121 nC/cm^2, respectively. While in the SiC MCD-MOSFET, $Q_G = 531$ nC/cm^2 and $Q_{GD} = 12$ nC/cm^2 are obtained. As a consequence, the figures of merit $R_{ON} \times Q_G$ and $R_{ON} \times Q_{GD}$ are enhanced by a factor of 1.8 and 9, respectively. This is a remarkable promotion, making the SiC MCD-MOSFET more suitable for higher frequency applications. The main characteristics of the devices are summarized in Table 2.

III. PARAMETERS VARIATION

The superior performance of SiC MCD-MOSFET is demonstrated in the previous section. In this section, the influence of parameters variation on the device characteristics will be explored.

As SiC-based switching devices, the high electric field in the gate oxide under reverse bias is always the major concern on account of the large critical field strength of SiC material. Fig. 13 shows the lateral dimension of the studied SiC MCD-MOSFET, and the maximum oxide field versus W_{GS} as a function of t_{co} is illustrated in Fig. 14. The hollow symbols represent the occurrence of the oxide breakdown. It is shown that a thicker t_{co} is favourable for electric field suppression as previously described. What's more, we obtain a type of "arch" shaped curve at a specified t_{co}, and the peak of electric field occurs at $W_{GS} = 0.5$ μm. This is reasonable since the gate oxide in the middle of the neck area is the weakest point due to the absence of protection by the depletion layer of P-base/N-drift junction where the drain voltage is mainly sustained. The electric field crowding is very likely to happen therein at the corner of the dummy gate, especially with a smaller t_{co}. Therefore, W_{GS} and t_{co} require to be carefully designed to ensure the ruggedness of the device and avoid the premature breakdown of the gate oxide.

TABLE 2. Performance comparison.

	SiC C-MOSFET	SiC MCD-MOSFET	Unit
V_F	2.82	1.75	V
BD	Yes	No	-
BV	1480	1515	V
R_{ON}	0.89	0.96	mΩ·cm^2
Q_{RR}	3.28	1.56	μC/cm^2
C_{ISS}	20	9	nF/cm^2
C_{RSS}	52	7	pF/cm^2
Q_G	1037	531	nC/cm^2
Q_{GD}	121	12	nC/cm^2
$R_{ON}\times Q_G$	923	510	mΩ·nC
$R_{ON}\times Q_{GD}$	108	12	mΩ·nC

BD: bipolar degradation;
Q_{RR} is measured at I_{SD}=500 A/cm^2;
C_{ISS} and C_{RSS} are measured at V_{DS}=200 V.

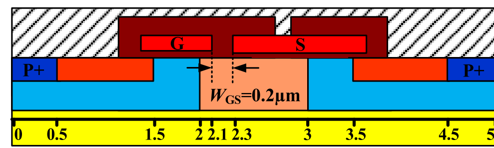

FIGURE 13. Lateral dimension of the SiC MCD-MOSFET.

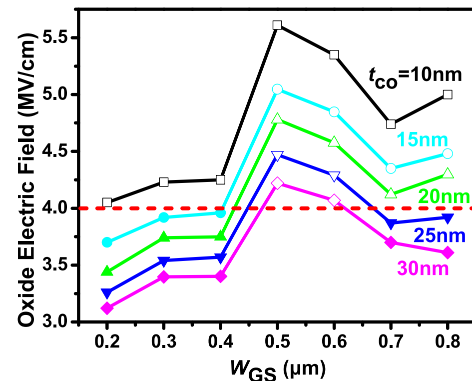

FIGURE 14. Variations of the maximum electric field in the oxide with W_{GS} as a function of t_{co}.

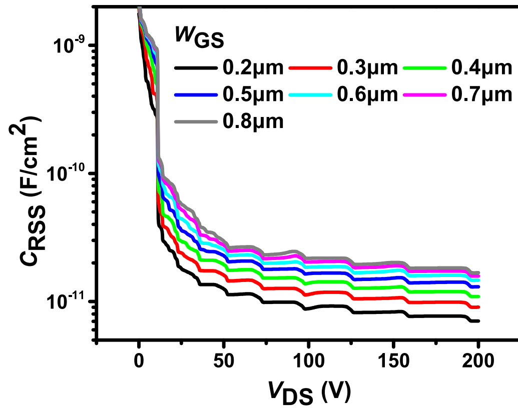

FIGURE 15. Variations of C_{RSS} with V_{DS} as a function of W_{GS}.

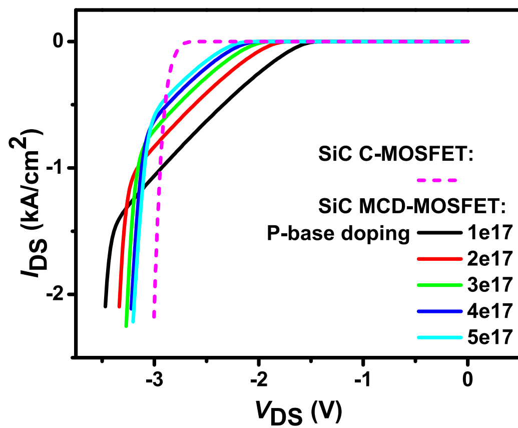

FIGURE 16. Conduction characteristics in the third quadrant for the SiC MCD-MOSFET versus P-base doping at t_{co} = 15 nm.

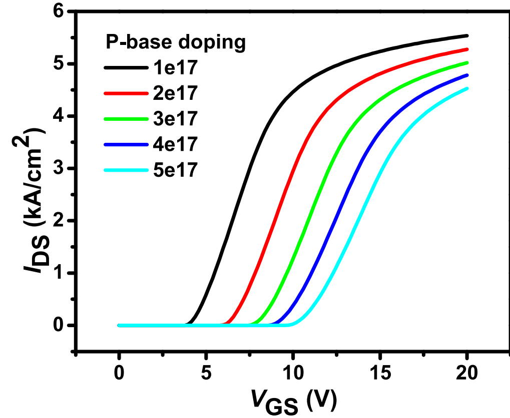

FIGURE 17. Variations of the transfer characteristics of SiC MCD-MOSFET as a function of P-base doping at t_{co} = 15 nm.

It should be noted that no significant changes of the device performance are found in our simulations except that of V_F just by modifying t_{co}, and W_{GS} has little effect on the first and third quadrant of *I-V* features for the SiC MCD-MOSFET due to the highly doped JFET region. Therefore, we only talk about the influence of W_{GS} on the reverse transfer capacitance herein, and the consequent variation of gate-to-drain charge characteristics is easy to reason out due to the proportional relationship between them. Note that W_{GS} is just adjusted by changing the dummy gate length, and the true gate length keeps constant. Fig. 15 presents the C_{RSS} versus V_{DS} as a function of W_{GS}. It is discerned that a smaller W_{GS} will result in a lower C_{RSS}. As we know, C_{RSS} is determined by the series combination of C_{OX} (the electrostatic capacitance of the oxide layer) and C_{SM} (the semiconductor capacitance under the gate oxide). Meanwhile, it is proportional to the width of the JFET area where the gate electrode overlaps the epitaxy. C_{OX} is constant for a particular architecture, while C_{SM} decreases with the increase of drain voltage due to the formation of the depletion region at the P-base/N-drift junction. In other word, a deeper bulk depletion will lead to a smaller C_{SM} [27]. In the SiC MCD-MOSFET with a larger W_{GS}, there is no depletion region formed in the JFET area under the gate oxide. Hence, a higher C_{SM} is obtained due to the lack of pinch-off effect at a lower drain voltage. In a word, a smaller W_{GS} and a thicker t_{co} is preferred. Of course, the tradeoff between the electric field suppression and V_F should also be taken into account.

The P-base doping is a parameter which can significantly influence the threshold voltage of the device, while it is also a key factor affecting both of the forward and reverse conduction performance of the SiC MCD-MOSFET. As shown in Fig. 16, a larger knee voltage is obtained with higher P-base doping. However, the unipolar feature can be still observed at I_{SD} lower than 500 A/cm^2 even with P-base doping of up to 5×10^{17} cm^{-3}. In that case, besides, the threshold voltage of the device would reach to 10 V, as exhibited in Fig. 17. That is to say, the increased doping concentration of P-base region will not degrade too much the conduction characteristic of the SiC MCD-MOSFET in the third quadrant with a threshold voltage in a reasonable range. What's more, a high threshold voltage always results in a large R_{ON}, namely a performance degradation in the first quadrant(not reported here for brevity). However, a lightly doped P-base region, conversely, could induce reach-through breakdown, which would weaken the blocking capability of the device. As a result, the P-base region with proper design should be carefully considered according to different device applications.

IV. CONCLUSION

The easy-to-implement SiC MCD-MOSFET is studied in this paper utilizing TCAD simulations. The turn-on of the parasitic body diode can be restrained effectively when operating as a freewheeling diode, thus completely eliminating the bipolar degradation. Moreover, for the SiC MCD-MOSFET working as a switching device, the superior characteristics can be observed, such as a rather small C_{ISS} and C_{RSS} and a lower Q_G and Q_{GD}, when compared to the SiC C-MOSFET. Nevertheless, there is only a slight increase in R_{ON} (8%), leading to a notably increased figures of merit

in the SiC MCD-MOSFET. At last, the effect of parameters variation on the device characteristics is discussed as well. These remarkable attributes make the SiC MCD-MOSFET an excellent choice for high-frequency power electronic applications.

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