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Germanium Twin-Transistor Nonvolatile Memory With FinFET Structure

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ABSTRACT Germanium is a promising alternative material for use in advanced technology nodes because it exhibits symmetrical mobility of holes and electrons. Embedded nonvolatile memory (NVM) is essential in electronic devices with integrated circuit (IC) technology, including future Ge-based technology. In this paper, we demonstrate Ge twin-transistor NVM with a fin field-effect transistor (FinFET) structure. This Ge twin-transistor NVM exhibits high programming and erasing speeds and satisfactory reliability. Moreover, the masks and fabrication process of this Ge twin-transistor NVM are identical to those of Ge-channel FinFETs. Thus, Ge twin-transistor NVM is a promising candidate for embedded NVM applications in future high-performance Ge complementary metal–oxide–semiconductor technology (CMOS).

INDEX TERMS Germanium, non-volatile memory, FinFET, embedded memory.

I. INTRODUCTION

In conventional planar CMOS technology, short-channel effects (SCEs) cannot easily be suppressed. As per Moore's law, FinFET was proposed and was mass produced below the 16-nm technology node. The whole channel is close to the gate electrode in a FinFET. Therefore, the FinFET structure enhances gate controllability because of the absence of leakage paths in the channel [1]–[3]. In NVM applications, the FinFET structure enhances the electric field in tunneling oxide. Accordingly, the FinFET structure improves the program/erase (P/E) efficiency of NVM because of the corner effect [4]. Ge is a promising alternative channel material that can be used for improving transistor performance because Ge exhibits high, symmetric carrier mobility for holes and electrons. In addition, p-type and n-type Ge FinFETs with improved channel surface roughness have been successfully used in the past few years [5]–[8]. Most mass storage flash memory devices such as solid-state drives (SSD) are based on the NAND array architecture. The bit cells are series-connected in the NAND array architecture for NVM applications. Thus, high-series resistances in NAND arrays result in low read currents. High-mobility Ge-channel NVM can be used to enhance the read current for NAND array architecture.

Information can be sustained in NVM even without a power supply. IC chips require embedded NVM to store basic information, such as program codes and identification codes. Embedded NVM can be fabricated with few or no additional masks. Therefore, embedded NVM is an essential element in current IC technology. NVM using a Si-channel twin-transistor structure was proposed for embedded NVM applications [8]–[9]: NVM with a similar structure has been mass produced in many Si-based platforms. According to the relevant literature, Ge-based conventional planar NVM with a thermal SiO2–Si3N4–SiO2 gate dielectric stack exhibits excellent P/E performance and reliability [10]–[11]. This paper presents Ge-channel twin-transistor NVM with a FinFET structure (Ge Twin NVM). The fabrication process of this Ge twin NVM is identical to that of a Ge-channel FinFET. The Ge-channel

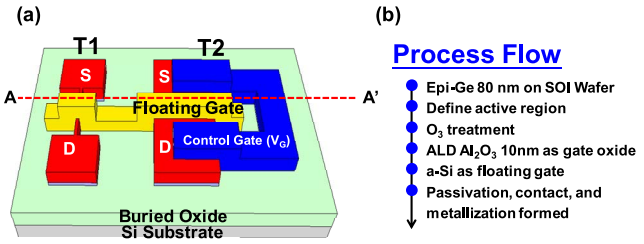

FIGURE 1. **(a) Schematic top view of the Ge Twin NVM with one fin, and (b) process flow of the Ge Twin NVM.**

device has a limited thermal budget [12]. This Ge Twin NVM does not require the deposition of multiple gate dielectric layers. Thus, the transistor characteristics of this Ge Twin NVM are superior to those of other Ge-channel NVM in the literature [10]–[11], and in this Ge Twin NVM, more thermal budget is preserved for the remaining IC chip fabrication processes.

II. DEVICE FABRICATION

The key fabrication steps of the Ge twin-transistor NVM are summarized in Fig. 1 and Fig. 2. Fig. 1(b) displays the structure and process flow of the Ge Twin NVM. An 80-nm epitaxial Ge layer was grown on an SOI wafer through remote plasma chemical vapor deposition. In-situ post annealing was performed at 825°C for 5 min to reduce lattice-mismatch-induced dislocations in the Ge layer. Two transistors are present in the Ge Twin NVM shown in Fig. 1(a), namely T1 and T2. The active regions of T1 and T2 were patterned using electron beam (e-beam) direct writing and transferred through transmission coupled plasma (TCP) etching.

After hydrofluoric acid chemical cleaning, O_3 treatment generated GeO_2 to improve channel surface roughness and the Al_2O_3 layer was grown by atomic layer deposition (ALD) to reduce the interface defect density (D_{it}). A 10-nm-thick Al_2O_3 was deposited in the ALD chamber as the tunneling oxide and the blocking oxide. Subsequently, a 110-nm amorphous-Si (a-Si) layer was deposited through high-density plasma chemical vapor deposition as a floating gate. After the gate deposition, the gate regions were patterned by e-beam direct writing and TCP etching [13]–[15]. The active layer was implanted using boron ions to form a p-type device (1×10^{15} cm^{-2} at 10keV), then activated by a microwave annealing (MWA) at 2.75p for 100 secs [16]. A 200-nm-thick SiO_2 passivation layer was deposited by low-pressure chemical vapor deposition (LPCVD) as a passivation layer, and metal contacts were patterned through e-beam direct writing and transferred through TCP etching. Finally, Al–Si–Cu metallization was performed to a thickness of 300 nm.

III. RESULTS AND DISCUSSION

Fig. 3 illustrates the top view of the Ge Twin NVM which is composed of T1 and T2. The gate electrodes of T1 and T2 are

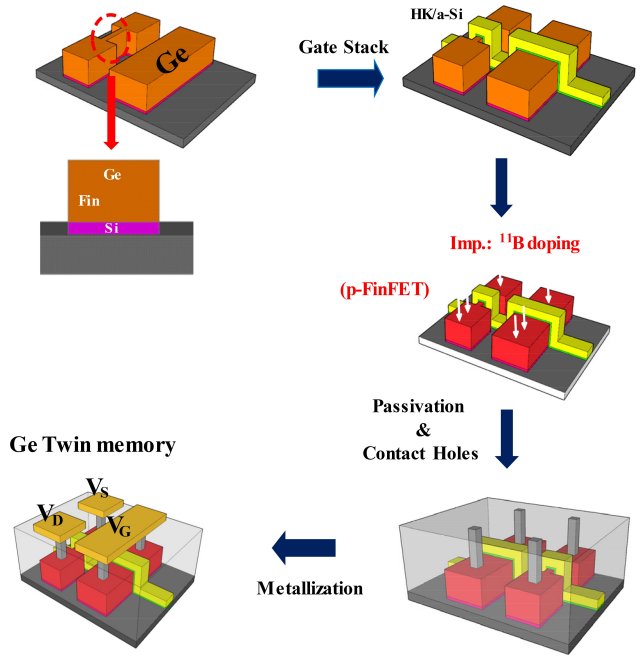

FIGURE 2. **Process flowcharts for fabrication of the Ge twin-transistor NVM.**

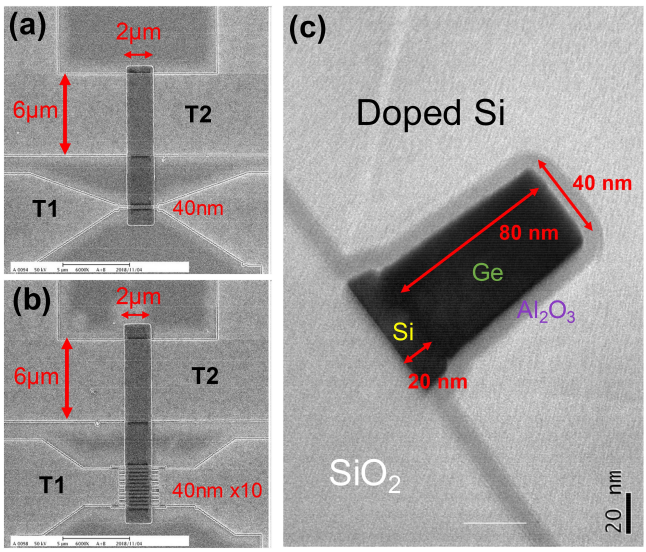

FIGURE 3. **Top-view SEM image of the Ge Twin NVM with (a) one fin and (b) ten fins. (c) The TEM image of the cross-section of the Ge Twin NVM.**

connected as a floating gate for charge storage. The source and the drain of T2 are connected and used as a control gate to control the channel of T1. The charges can be stored in the floating gate of T1 and T2, and the stored charges can affect the threshold voltage of T1. The electrons in the channel of T1 or in the floating gate can tunnel through the gate oxide of T1 using the Fowerler–Nordheim (FN) method in the P/E operations. The gate voltage is biased at the source/drain of T2 for both read and P/E operations. The gate length and the gate width of T2 are 2 and 6 μm, respectively. T1 is

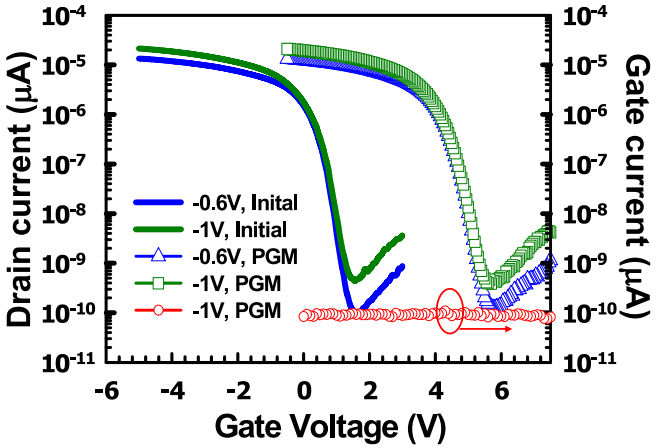

FIGURE 4. $I_D - V_G$ transfer characteristic of the fresh Ge Twin NVM with one fin at $V_D = -1$ V and −0.6 V. The programming bias is $V_G = 17$ V, $V_D = V_S = 0$ V for 0.1s from the fresh state to the programmed state (PGM). Open circle curve shows the gate current at $V_D = -1$ V after programming (PGM).

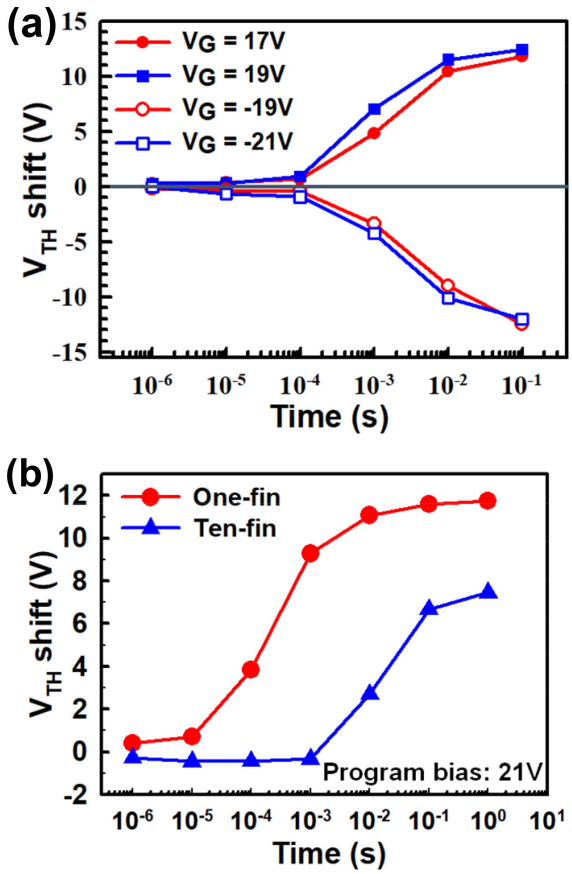

FIGURE 5. (a) FN programming and FN erasing characteristics of the Ge Twin NVMs with one fin. (b) Programming speeds of the one-fin and the ten-fin devices.

a FinFET which has one fin with a width = 40 nm, as shown in Fig. 3(a). A Ge Twin NVM with ten fins (ten-fin device) was fabricated for comparison in Fig. 3(b). Fig. 3(c) is the transmission electron microscopy (TEM) image of the fin of T1. The fin height of the Ge Twin NVM is 80 nm, as shown in Fig. 3 (c). The gate electrodes of T1 and T2 were connected to form the floating gate, and, thus, the total charges of T1 and T2 are identical in the channel. However, the gate area of T1 was smaller than that of T2. Therefore, the charge density of T1 was higher than that of T2. More charge density can generate more electric flux density in the gate oxide of T1, and the electric field of T1 was higher than that of T2 in the gate oxide. Accordingly, the carrier exchange between the floating gate and the channel was in T1 in the P/E operations.

Fig. 4 illustrates the $I_D - V_G$, $I_G - V_G$ curve and the programming characteristics of the Ge Twin NVM with one fin (one-fin device). The programming mechanism involves FN tunneling method at $V_G = 17$ V, $V_D = V_S = 0$ V for 0.1 s. The gate bias was supplied from the S/D of T2 in the read operation. Thus, the effective gate oxide thickness was 20 nm in the read operation. The read bias in Fig. 4 is $V_D = -0.6$ V and −1V with $V_S = 0$ V, and the subthreshold slope is 291 mV/dec. The off current of the Ge Twin NVM is sensitive to the gate bias. Gate-induced barrier lowering (GIDL) is an intrinsic drawback of Ge-channel because of the narrow bandgap of Ge. The gate leakage of the one fin device is very small to ignore and it shows although the electric field in programming state is high, the Al_2O_3 layer is still not breakdown. The Ge-channel FET has high potential for low-voltage applications because of the high both electron and hole mobility. However, the Ge-channel FET also is required to operate at low voltage to suppress the GIDL leakage current.

The P/E characteristics of the one fin device using FN method are plotted in Fig. 5(a). The start point for the programming speed was at $V_{TH} = -5.4$ V, and the start point for the erasing speed was at $V_{TH} = 7.5$ V. The V_{TH} shifts (ΔV_{TH}) for programming operations were more than 4 V in 1ms. This high P/E efficiency occurred because the corner region in the gate oxide had a high electric field to enhance the FN tunneling current in a FinFET [4]. Furthermore, the 10-nm-thick Al_2O_3 can avoid electron leakage from a-Si charge trapping layer and maintain good retention and endurance. Thus, the Al_2O_3 film is thick, the P/E performance are satisfied. Fig. 5(b) displays the programming speeds of the one-fin device and the ten-fin device. The maximum ΔV_{TH} for one fin and ten fins device are 8V and 12V, respectively. Although there has trap of the GeO_2/Al_2O_3 interface, the D_{it} and hysteresis can be ignored under such high ΔV_{TH}. The coupling ratio from the control gate of the one-fin device is higher than that of the ten-fin device. Therefore, the electric field in the T1 gate oxide of the one-fin device was higher than that of the ten-fin device. As the result, the programming speed of the one-fin device was markedly faster than that of the ten-fin device in the FN tunneling operation.

Fig. 6(a) depicts the endurance characteristics of the one-fin and the ten-fin devices using the FN programming and the FN erasing methods. In this study, the best programming

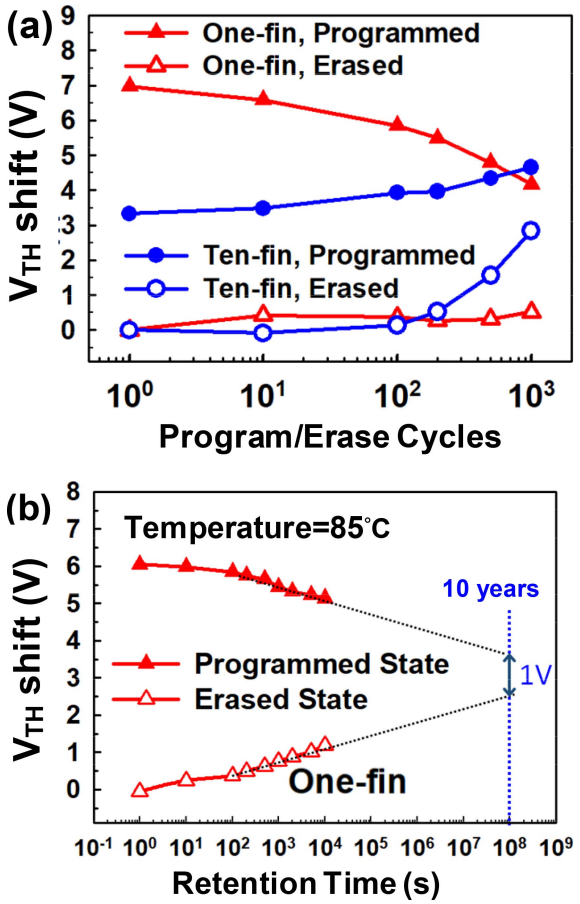

FIGURE 6. (a) Programming/erasing cycling characteristics of the one-fin and the ten-fin devices. (b) Retention characteristics of one-fin device at 85°C.

condition after 1000 P/E cycles of the one-fin device was $V_G = 15$ V, $V_D = V_S = 0$ V for 10ms, and the erasing condition was $V_G = -17$ V, $V_D = V_S = 0$ V for 10ms. The best programming condition of the ten-fin device was $V_G = 17$ V, $V_D = V_S = 0$ V for 10ms, and the erasing condition was $V_G = -20$ V, $V_D = V_S = 0$ V for 10ms. The V_{TH} of the one-fin device and ten-fin device were −3.1V and −1.5V, respectively, in the erased state. After 1000 P/E cycles, the memory window of the one-fin device sustained 3.65V, which is satisfactory for consumer-grade applications. The ten-fin device requires high bias for P/E operations. More deep-trap sites in the gate oxide were generated because of the high electric field in the P/E operations. Removal of the charges in the deep-trap sits is difficult. Thus, the ten-fin device exhibited degraded erasing efficiency after 1000 P/E cycles for the ten-fin device. Fig. 6(b) illustrates the retention characteristics of the one-fin device at 85°C using the FN P/E methods. The programming condition was $V_G = 15$ V, $V_D = V_S = 0$ V for 10ms, and the erasing condition was $V_G = -18$ V, $V_D = V_S = 0$ V for 10ms. The charges of the one-fin device were stored in the floating gate after the programming operation. The charges escaped from the floating gate with time. The barrier height of electrons and holes were 2.66 and 3.17 eV in the floating gate [17], and the energy barrier was sufficient high to sustain the charges in the floating gate. The memory window sustained 1V after 10 years at high temperature. The read current ratio of the programmed and the erased states are over three orders after ten years. The ALD Al_2O_3 gate oxide in this Ge Twin NVM has higher defect density than the thermal SiO_2 tunneling oxide in a conventional NVM [18]. However, the dielectric constant of an Al_2O_3 layer is much higher than that of a thermal SiO_2 layer. Therefore, the thicker Al_2O_3 gate oxide can be used in the Ge Twin NVM to further improve endurance and retention characteristics.

IV. CONCLUSION

This study investigated the feasibility of Ge Twin NVM in embedded NVM applications for use in future high-performance Ge CMOS technology. Ge Twin NVM exhibits good transistor characteristics and high P/E efficiency for memory applications [19]–[20]. For Ge Twin NVM, the number of P/E cycles can reach 1000, and the data retention exceeds 10 years. Moreover, the masks and fabrication processes for Ge Twin NVM are identical to those for Ge CMOS technology.

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