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Self-Heating in FDSOI UTBB MOSFETs at Cryogenic Temperatures and Its Effect on Analog Figures of Merit

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ABSTRACT This work studies the self-heating (SH) effect in ultra-thin body ultra-thin buried oxide (UTBB) FDSOI MOSFETs at cryogenic temperatures down to 77 K. S-parameter measurements in a wide frequency range, with the so-called RF technique, are employed to assess SH parameters and related variation of analog figures of merit (FoMs) at different temperatures. Contrary to the expectations, the effect of self-heating on analog FoMs is slightly weaker at cryogenic temperatures with respect to room-temperature case. The extracted thermal resistance and channel temperature rise at 300 K and 77 K in short-channel devices are of the same order of magnitude. The observed increase in SH characteristic frequency with temperature reduction emphasizes the advantage of the RF technique for the fair analysis of SH-related features in advanced technologies at cryogenic temperatures.

INDEX TERMS UTBB, FDSOI, MOSFET, self-heating, S-parameters, analog figures of merit.

I. INTRODUCTION

Ultra-thin body and buried oxide (UTBB) fully depleted (FD) silicon on insulator (SOI) technology is widely considered as one of the main contenders for the technology downscaling to 20 nm and beyond [1]–[4]. Outstanding electrostatic and variability control, excellent performance in terms of low-power, high-speed, as well as attractive analog and RF figures of merit (FoMs) offered by this technology were demonstrated in numerous publications [1]–[8]. This technology was also largely investigated at cryogenic temperatures showing promising improvement of device performance [9]–[12]. Apart from space applications, cryogenic studies are nowadays strongly motivated by a breakthrough in silicon-based quantum bits (qubit) which requires their co-integration with the control blocks and read-out electronics for the realization of quantum computers [13]–[16]. Device self-heating (SH) and related power dissipation is particularly crucial for such applications because it can disturb the spin state.

Self-heating effect in SOI-based technologies at cryogenic temperatures was previously studied in "older technology generations" [17], [18] showing SH intensification both in terms of channel temperature rise, thermal resistance and related parameters degradation at cryogenic temperatures A more recent study [19] analysed self-heating in a wide variety of FDSOI transistors (including UTBB) down to 4.2 K using gate resistance technique and showed a strongly non-linear dependence of the channel temperature rise with dissipated power at low temperatures. Our group has studied SH effect in FDSOI technology and its impact on analog FoMs at room temperature and shown that in spite of strong SH with the channel temperature rise reaching ∼85 °C, its effect on parameters degradation is limited allowing FDSOI devices to outperform bulk counterparts [5], [20].

This paper is an extended version of our work [21], in which the variation of analog FoMs due to self-heating in 28nm FDSOI UTBB CMOS technology is evaluated down

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to 77 K. In [21], it also shown how the thermal resistance and channel temperature rise are modified at 77 K compared to 300 K. The present paper extends [21] by providing a critical analysis of the assumptions made by the extraction technique and their impact on the self-heating related results. The present extended paper also discusses the observed variations of the FETs thermal resistance from 300 to 77 K according to the devices length in terms of the thermal resistivity of different materials (Si, SiO_2, metal) behavior with temperature. Section II describes the experimental setup. In Section III, the impact of SH on analog FoMs such as transconductance (g_m), output conductance (g_d) and intrinsic voltage gain (A_v) is assessed using S-parameter measurements in a wide frequency range. In Section IV, the change of g_d with frequency (f) complemented by the drain current (I_d) versus temperature (T) variation (also called RF technique [5], [22]) is used to monitor device self-heating and extract related parameters. First, SH parameters, such as thermal resistance (R_{th}), channel temperature rise (ΔT) and characteristic frequency (f_c), are extracted in a temperature range from 300 to 77 K and devices length spanning from 25 nm to 90 nm. Then, the impact of different sources of uncertainty inherent to the method on the thermal resistance extraction is discussed.

II. EXPERIMENTAL DETAILS

The devices studied in this work originate from ST-Microelectronics 28nm FDSOI process [1]. The Si film, BOX and the equivalent gate oxide thicknesses are 7, 25 and 1.3 nm, respectively. The ground plane (GP) doping is of the same type as the channel. More process details can be found in [1]. The n-channel MOSFETs under study feature 60 fingers of 2 µm width, embedded in ground-signal-ground (GSG) pads for RF characterization. The gate lengths (L) of the studied devices range from 25 to 90 nm. The back gate and source terminals are grounded. LakeShore cryogenic probe station is used to extend DC I-V and RF S-parameter measurements temperature range from 300 K down to liquid nitrogen temperature of 77 K. The devices are measured from 50 kHz up to 3 GHz with an ENA Vector Network Analyzer and a pair of GSG Picoprobes. At each temperature, a short-open-load-thru (SOLT) calibration is performed on an ISS calkit (off-chip), which is at the same temperature as the devices.

III. IMPACT OF SELF-HEATING ON ANALOG FIGURES OF MERIT

The output conductance, transconductance and intrinsic voltage gain are extracted as the real part of Y_{dd}, Y_{dg} and g_m/g_d, respectively. Y-parameters are extracted from measured S-parameters followed by a dedicated open de-embedding for each device (and at every temperature). An example of g_d, g_m and A_v versus frequency curves at different temperatures is given in Fig. 1 for the 30 nm-long device in strong inversion and saturation. With temperature reduction from 300 K to 77 K, the g_m improvement of 30 % is larger than the g_d degradation of only 12 %, resulting in an overall improvement of A_v by about 15% at a fixed bias condition of $V_g = V_d = 1$ V. The transconductance

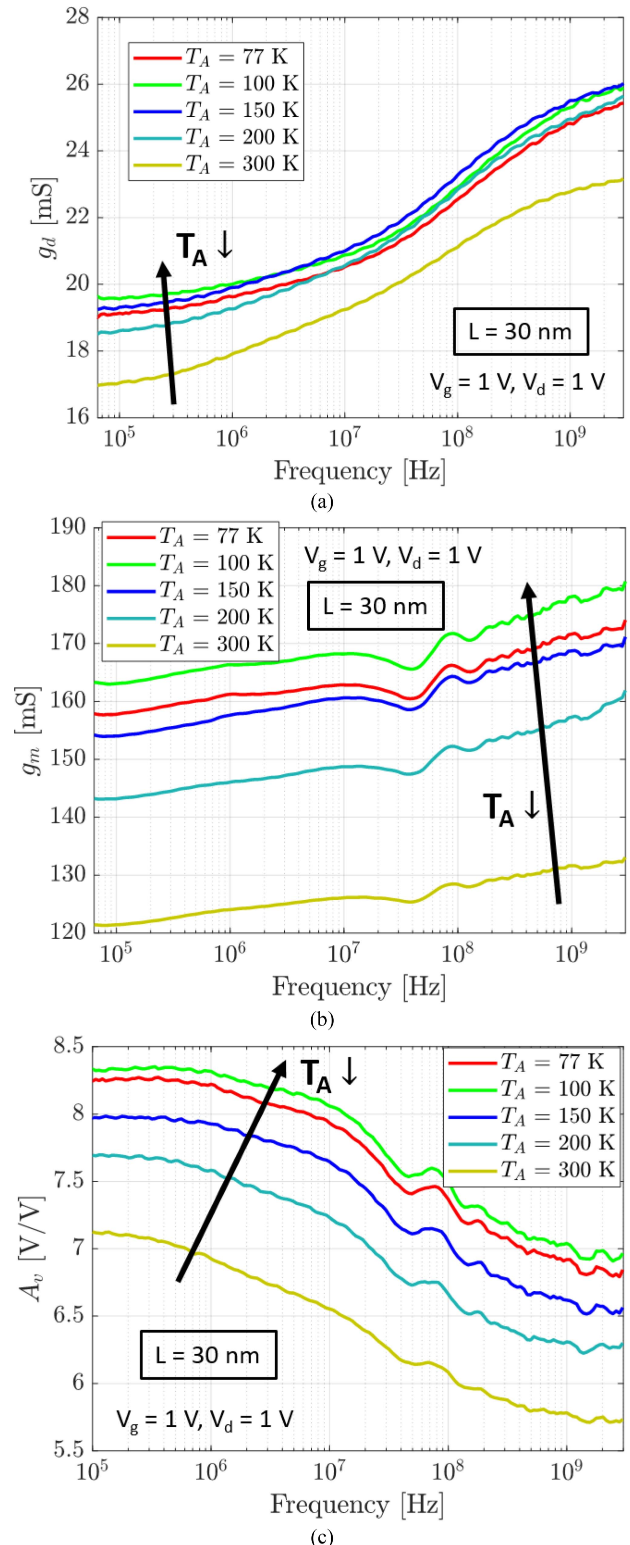
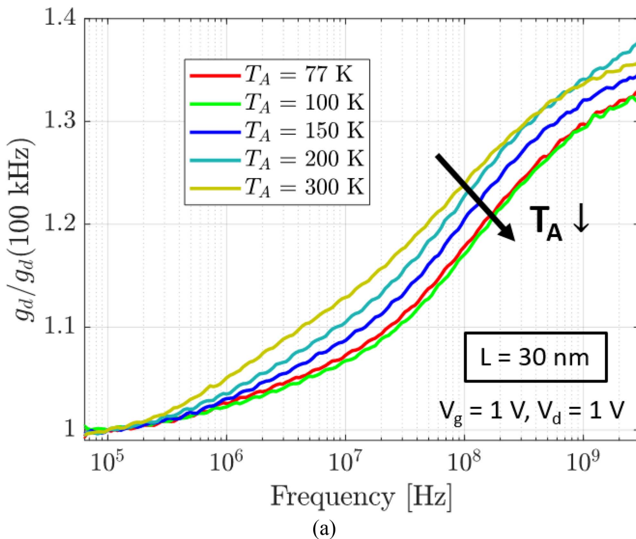
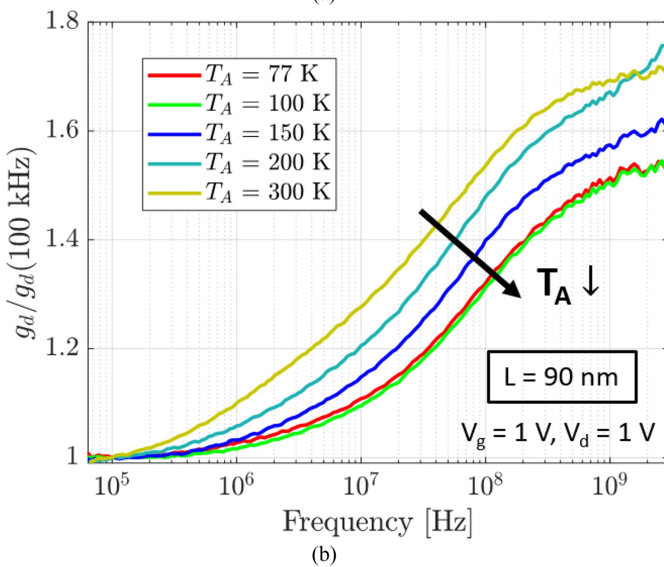


FIGURE 1. g_d (a), g_m (b) and A_v (c) versus frequency of the 30 nm-long UTBB n-MOSFET for different temperatures, at $V_d = V_g = 1$ V.

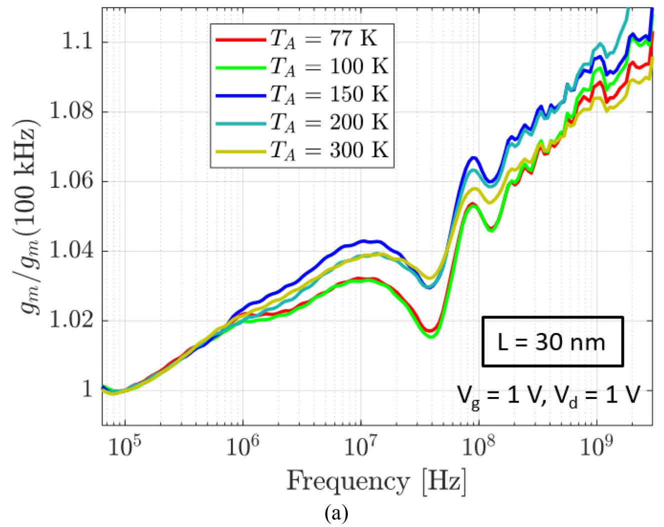


(a)

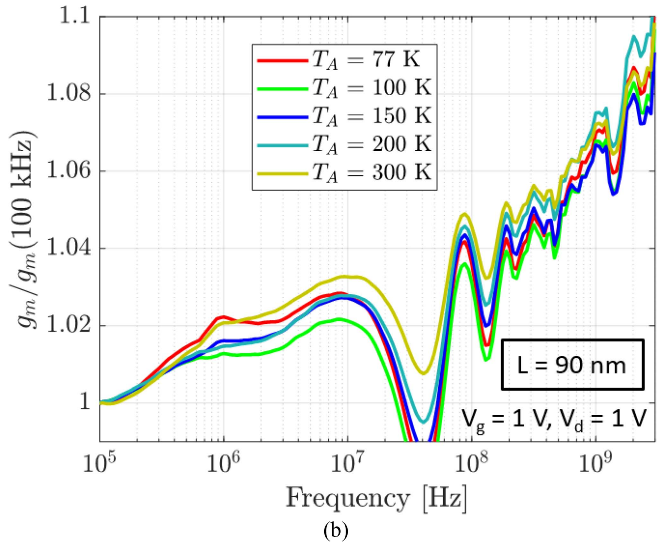


(b)

FIGURE 2. Normalized g_d variation with frequency for different temperatures of the 30 (a) and 90 (b) nm-long UTBB MOSFETs, at $V_d = V_g = 1$ V.



(a)



(b)

FIGURE 3. Normalized g_m versus frequency for different temperatures of the 30 (a) and 90 (b) nm-long UTBB MOSFETs, at $V_d = V_g = 1$ V. The resonance around 50 MHz is present in all measurements and attributed to the measurement setup.

variation with temperature is mainly related to the mobility dependence on temperature. As temperature decreases, two concurrent mechanisms dictate the mobility behavior: (i) Coulomb scattering (featuring a mobility reduction with decreasing temperature) on the defects of the source/drain and extensions regions and (ii) phonon scattering (featuring a mobility improvement with decreasing temperature) [10], [12]. The impact of Coulomb scattering on the mobility is more important in shorter channels [23]. The small reduction in g_m from 100 K to 77 K was already reported in [10], [12] and explained by a mobility saturating at 100 K and slightly deteriorating at 77 K due to a dominant Coulomb scattering effect.

It is commonly accepted [24], [25] that the frequency responses of g_d and g_m feature a transition related to SH. As the frequency increases, the lattice temperature ceases to follow the small-signal AC electrical excitation, such that the values of g_d and g_m at low frequency are affected by the dynamic and static SH, while their values at high frequency are "dynamic-SH free". Indeed, the analog FoMs are flat below 100 kHz and then tend to a plateau above 1 GHz. It is worth noting that the substrate-related transition in g_d frequency response is greatly reduced in our devices thanks to the use of ground planes in these devices as discussed previously in [5].

Figs. 2-4 show normalized values of analog FoMs with respect to the low frequency ones at several temperatures. One can note in Fig. 2 that g_d increases with frequency and tends to a plateau at 1-3 GHz, where the dynamic self-heating effect is removed. SH is seen to result in a very strong reduction of g_d at low frequency (i.e., ∼35 % to 70% of g_d increase is observed at the "dynamic-SH-free" point for the short and long-channel transistors resp. in the room temperature case, Fig. 2). At the same time, the g_m improvement

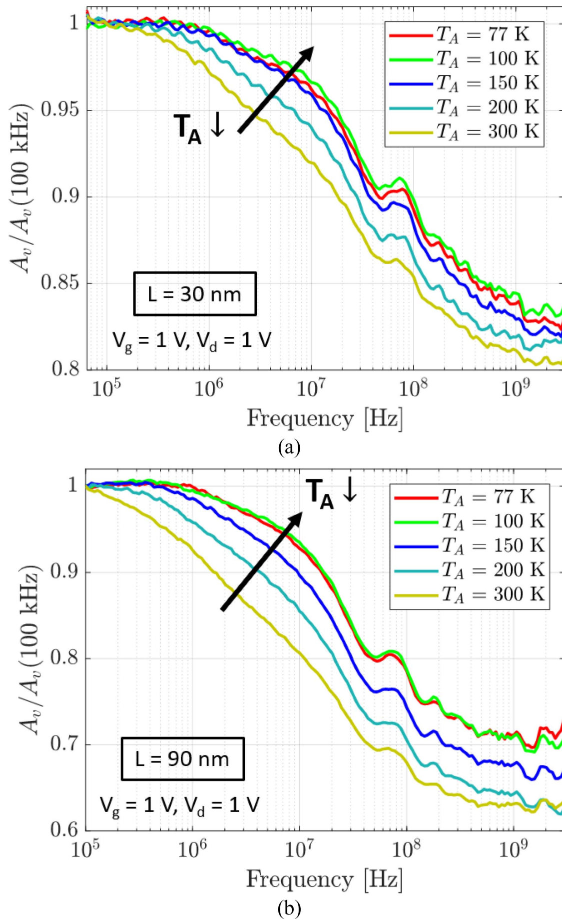


FIGURE 4. Normalized A_v versus frequency for different temperatures of the 30 (a) and 90 (b) nm-long UTBB MOSFETs, at $V_d = V_g = 1$ V.

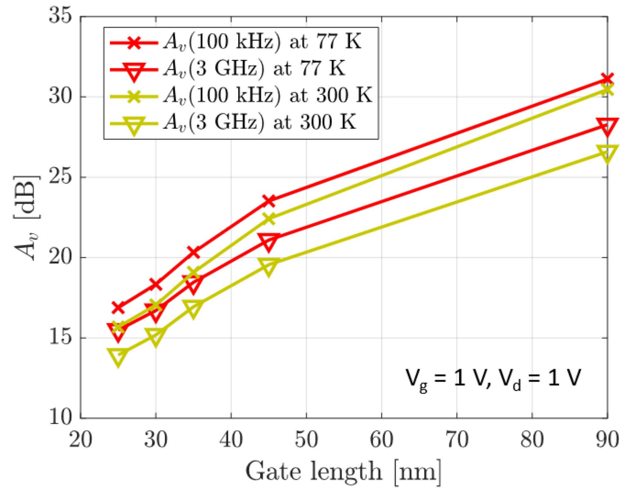


FIGURE 5. Voltage gain, A_v in dB at 100 kHz and 3 GHz at 77 (red) and 300 K (yellow) for different device lengths, at $V_d = V_g = 1$ V.

observed at "dynamic-SH-free" point is relatively smaller (∼9 % for 2 devices in the room temperature case, Fig. 3). Because of the stronger variation of g_d compared to g_m (Figs. 2-3), a degradation of the intrinsic voltage gain at "dynamic-SH-free" frequencies is observed (Fig. 4). A_v features a degradation of ∼20 to 37 % at room temperature for the 30 and 90 nm channel lengths respectively.

The relative effect of self-heating on the output conductance is attenuated at lower temperatures for all the devices (though only the 30 nm- and 90 nm-long ones are shown here, Fig. 2). The effect of self-heating on the transconductance does not vary much (by less than 2 %) with temperatures and lengths (Fig. 3). The A_v variations related to dynamic self-heating follow the g_d trends as the difference between the low- and high-frequency values is reduced at lower temperatures (Fig. 4). Furthermore, as can be noticed from Figs. 4(a) and 4(b), the reduction of SH-related A_v variation (from low to high frequencies) at low temperature is more pronounced for the longest device, but still present for all measured devices.

This trend is further detailed in Fig. 5, which shows A_v at low and high frequencies (i.e., with SH and dynamic-SH free, respectively) at 77 K and 300 K for devices of different gate lengths. The voltage gain decreases in short devices due to an increased g_d that dominates the larger g_m. As mentioned above, the increase in g_m with temperature reduction is more important than g_d increase, implying a larger gain at low temperature. The effect of self-heating is seen in the difference between the low- and high-frequency curves. One can see that SH-related A_v variation is slightly (∼1 dB) smaller at 77 K with respect to room temperature. This slight variation over temperature is larger than the experimental error. Indeed, the decreased A_v variation at lower temperatures is consistently observed from 300 K down to 77-100 K from Figs. 4(a) and 4(b).

Fig. 6 shows the transconductance as a function of the intrinsic voltage gain taken at 100 kHz and 3 GHz (i.e., affected by SH and "dynamic-SH free", respectively) for 77 K and 300 K (data for devices with various lengths are used to realize such plot). The g_m versus A_v plot is a well-known metric allowing to benchmark devices originating from different processes or operating at different temperatures and bias conditions in terms of their potential for further analog applications [5]. The g_m value as well as its increase due to dynamic SH removal is larger at cryogenic temperatures. The same observation is valid for A_v, i.e., it is slightly higher at cryogenic temperatures. However, A_v lowering due to SH is smaller at cryogenic temperatures.

Understanding all these observations raises questions about the thermal resistance and channel temperature rise variations with device length and ambient temperature.

IV. THERMAL PARAMETERS EXTRACTION

The thermal resistance R_{th} and channel temperature rise (ΔT) are extracted using the RF technique in a way similar to [24] initially developed for the AC g_d technique:

$$R_{th} = \frac{\Delta g_d}{\left(I_d + V_d g_{d,LF}\right)\partial I_d/\partial T}, \quad \Delta T = R_{th} I_d V_d \qquad (1)$$

where Δg_d is the difference between $g_{d,LF}$, the output conductance at 100 kHz where dynamic SH is present and g_d at

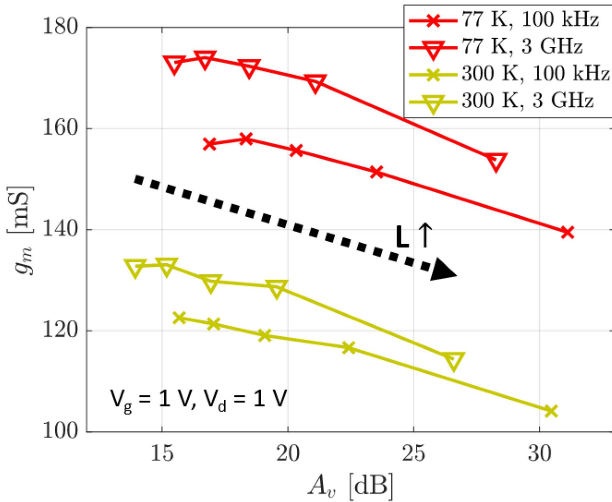


FIGURE 6. g_m versus A_v at 100 kHz ('x') and 3 GHz ('v') at 77 K (red) and 300 K (yellow), at $V_d = V_g = 1$ V, for UTBB MOSFETs featuring channel lengths of 25, 30, 35, 45 and 90 nm from left to right.

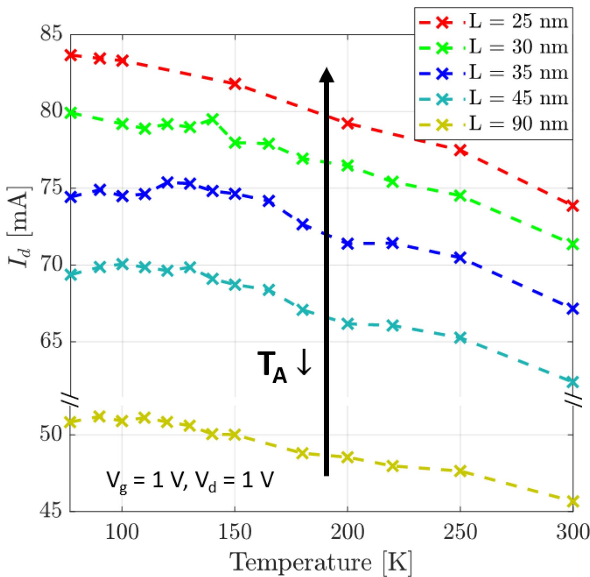


FIGURE 7. DC I_d versus temperature dependence for UTBB MOSFETs of different lengths, at $V_d = V_g = 1$ V.

3 GHz after the transition, where dynamic SH is removed. I_d is the DC drain current and $\partial I_d/\partial T$ its derivative with ambient temperature.

Fig. 7 shows I_d(T) curves measured on the devices with different lengths, at the same bias conditions as used for RF measurements. These curves are then used to compute the $\partial I_d/\partial T$ values to be used in Eq. (1). The extracted values of normalized thermal resistance (R_{thn}) and the associated channel temperature rise are presented in Table 1.

However, these values need to be discussed in the face of assumptions or limitations of the RF extraction technique.

a) Firstly, it is worth to point out that presently there is no consensus in literature about the point at which the $\partial I_d/\partial T$ term is evaluated, i.e., either at the "expected" channel temperature or at the chuck (ambient) temperature. The AC conductance in [25] and RF techniques in [22] explicitly specify that it should be evaluated at the channel temperature. Nevertheless, this detail is usually omitted in room temperature measurements, since the I_d dependence with temperature is approximately linear from 300 K to ~> 500 K. The difference in these approaches becomes crucial at cryogenic temperatures, since I_d tends to saturate as temperature goes down to 77-100 K. This either (i) leads to unphysically large values of R_{th} and ΔT if $\partial I_d/\partial T$ is evaluated at ambient/chuck temperature or (ii) means that (1) requires an iteration method to be solved and does not necessarily imply a unique solution, since $\partial I_d/\partial T$ is not constant and must be evaluated at the unknown channel temperature. $\partial I_d/\partial T$ in this work is first computed in the temperature range of 130-250 K, which corresponds to the expected channel temperature range (according to the extracted R_{th} at room temperature). Then, a first estimation of R_{thn} (noted R^1_{thn}) and device temperature is obtained. Based on the latter, $\partial I_d/\partial T$ is computed iteratively with the 3 closest temperature points and then R_{thn} and the device temperature are recomputed until convergence. The converged solution (noted R^n_{thn}) and corresponding temperature rise, are reported in Table 1 along with R^1_{thn} for all measured device lengths. It is observed that the first iteration already gives values close to the final ones, therefore validating the convergence of this method or the simplification to this linearization. However, the necessity of a good initial guess complexifies its application to low power levels, for which the I_d(T) curve is far from being linear.

b) Another assumption of this technique worth of further discussion is that the isothermal frequency (i.e., the frequency at which dynamic self-heating is removed) is achieved at 3 GHz. Indeed, during the analysis of the g_d (and g_m) frequency response, one should keep in mind that electrical effects, such as related to the substrate node or the gate resistance, are also known [26]

TABLE 1. Normalized R_{th} and temperature rise for different gate lengths and ambient temperatures. Room temperature extractions used additional DC I_d measurements up to 400 K.

Gate length	Normalized R_{th} [Kµm/mW]			Channel temperature rise [K]	
	77 K (R_{thn}^1)	*77 K (R_{thn}^n)*	*300 K*	*77 K*	*300 K*
25 nm	187	174	173	121	106
30 nm	201	201	167	134	99
35 nm	181	160	128	99	71
45 nm	195	196	135	113	70
90 nm	154	163	94	69	36

to induce an increase in g_d and g_m in a similar frequency range, such that their effect becomes hardly differentiable from self-heating effect. Overestimating the isothermal frequency could directly lead to an overestimation of R_{th}. Karim *et al.* proposed in [26] a way to physically extract the isothermal frequency from measurements at two different but very close biases. The isothermal frequency is then taken as the frequency at which the imaginary part of Y_{dd} (normalized to a constant) "significantly" deviates between those two biases. Fig. 8 illustrates the application of this method to our 30 nm-long UTBB MOSFET at $V_g = 1$ V and 1.1 V for a fixed $V_d = 1$ V and ambient temperatures of 300 K and 77 K. The black dashed lines are the curves of $Im(Y_{dd})$ at $V_g = 1$ V multiplied by a constant to have the same values as at 1.1 V at low frequency, such that the frequency at which the dashed and solid lines split is the isothermal frequency according to [26]. Using this method, the isothermal frequencies would lie above 20 MHz at 300 K and 10 MHz at 77 K for the L = 30 nm FET. However, [26] does not give a strict criterion concerning to which extent the two curves must deviate in order to achieve isothermal conditions. Therefore, the only thing that can be confidently estimated here is a lower bound of the isothermal frequency. Furthermore, the method from [26] assumes the isothermal frequency to be power-independent, which would make sense if R_{th} is also power-independent. However, a recent self-heating study [19] on similar UTBB devices down to 4.2 K using the DC gate resistance extraction approach shows that the thermal resistance is a strong function of power, particularly at low device temperatures. We thus consider the method from [26] as inappropriate in our case. Considering the isothermal frequency equal to 20 and 10 MHz at 300 K and 77 K, respectively, would imply a ~57% decrease in R_{thn} at 300 K and a ~78% decrease in R^1_{thn} at 77 K with respect to our extractions shown in Table 1. The latter reduction yields a non-physical value of R^1_{thn} that is one order of magnitude lower than what has been published in [19] and found in this work.

c) An envisaged method to avoid a strict determination of the isothermal frequency is then the simultaneous thermal and electrical (compact) modeling of the transistors as was done in [27] and [28]. In that case, the extracted thermal resistance would not be so sensitive to the isothermal frequency. Due to the lack of a cryogenic compact model, the application of this method is beyond the scope of this paper based on measurements.

Another important parameter that characterizes device thermal properties is the characteristic frequency of SH effect, f_c. Fig. 9 shows the characteristic frequency of the SH effect, determined to first order as in [24], i.e., $g_d(f_c) = g_d(100 \text{ kHz}) + \Delta g_d/3$. With this definition, f_c corresponds to the pole of a first-order thermal RC network describing the complex thermal impedance, such that $f_c = 1/(2\pi R_{th} C_{th})$, where C_{th} is the thermal capacitance. One can see that f_c moves toward higher frequencies as temperature decreases for all devices. An increase by approximately 4 times is observed for each device length from 300 K to 77 K. f_c is known to be inversely proportional to the thermal resistance and thermal capacitance. As we do not observe an important reduction of R_{th} down to 77 K, the f_c shift to higher frequencies suggests a reduction of the thermal capacitance with temperature reduction. Indeed, this is in agreement with other works that report a thermal capacitance reduction with temperature lowering [29], [30]. Furthermore, this f_c shift toward higher frequencies as temperature decreases justifies the need of the RF method for self-heating features extraction instead of the pulsed I-V method, especially for cryogenic temperatures. Indeed, the required pulse width for the latter method becomes further shorter than the minimum pulse duration of available commercial instruments for on-wafer measurement, which would lead to a wrong extraction of R_{th} [22].

To further discuss and analyze the results summarized in Table 1, one can see that at 300 K, the observed R_{th} and ΔT increase with the gate length reduction is in agreement with [20]. As displayed in Table 1, from room to cryogenic temperature, the increase in the extracted R_{th} is fairly small for the shortest devices, but becomes more important for the longest devices (up to 70% larger). A similar behaviour is observed for the channel temperature rise. The observed dependence of the R_{th} increase with respect to gate length may suggest different dominant heat evacuation paths according to the device structure. Several paths may indeed exist: (i) through the BOX and substrate, (ii) through the source and drain contacts and (iii) through the gate contact. The drain ($R_{th,d}$) and source ($R_{th,s}$) thermal impedances are composed of a contribution coming from the metal accesses and from the Si raised highly-doped source/drain regions. The thermal resistivity of metals is known to decrease with decreasing temperature (down to 10-20 K) [31]. The thermal resistivity of doped silicon layers slightly decreases with temperature down to 77 K [32]. The thermal impedance through the BOX and the bulk substrate is dominated by the dielectric thermal impedance ($R_{th,BOX}$). The thermal resistivity of dielectrics increases with decreasing temperature [33]. Since the source and drain thermal impedances do not scale with the gate length contrary to the BOX thermal impedance, the contribution of $R_{th,d}$ and $R_{th,s}$ to the total R_{th} of the device is more important for shorter channels [34]. Therefore, in agreement with Table 1, an increase in $R_{th,BOX}$ with decreasing temperature implies a larger increase in R_{th} for the longest devices whereas it is counterbalanced by the $R_{th,d}$ and $R_{th,s}$ reduction in the shortest ones.

The increases in R_{th} and ΔT in our devices are smaller than those reported in previous studies of SH effect in "older generation" SOI MOSFETs at cryogenic temperatures [17], [18]. Indeed, they demonstrated an R_{th} increase by more than 2 times and ΔT increase by more than

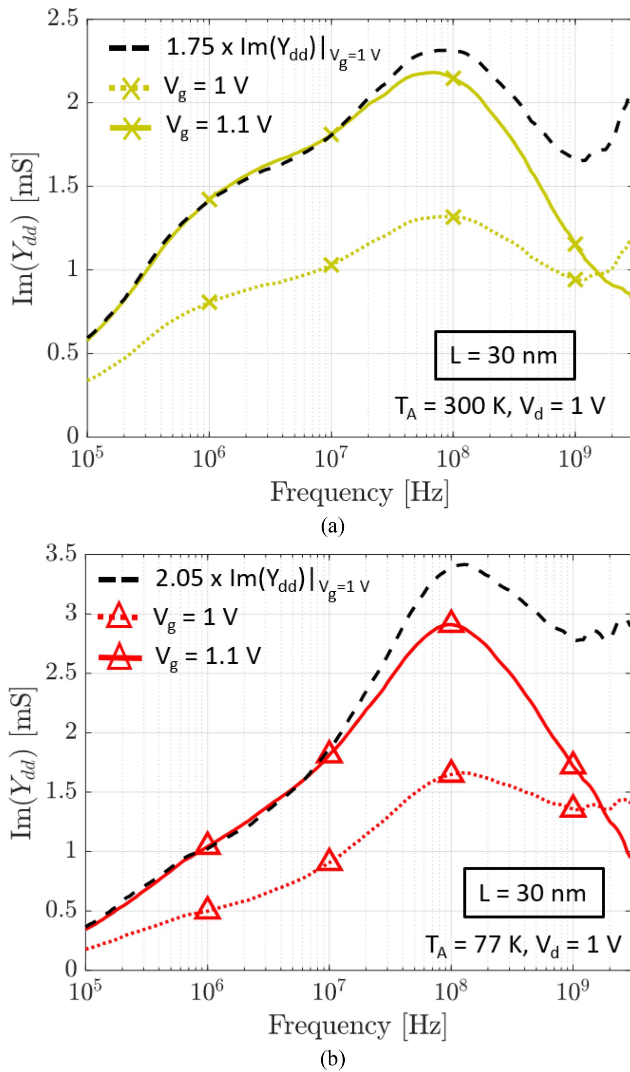


FIGURE 8. **Imaginary part of Y_{dd} as a function of frequency at an ambient temperature of 300 K (a) and 77 K (b) for the 30 nm-long FET, at $V_g = 1$ V in dotted lines and $V_g = 1.1$ V in solid lines. $V_d = 1$ V. The black dashed lines are the curves of Im(Y_{dd}) at $V_g = 1$ V multiplied by a constant to have the same value as at 1.1 V at low frequency.**

3 times at cryogenic temperatures [17], [18]. Considering the discussion of the previous paragraph, the possible reason of the improvement we observe in UTBB FDSOI technology involves a different dominant heat evacuation path due to different geometries (L, Si film and BOX thicknesses), bias conditions and doping levels in our study w.r.t. previous works.

It is interesting to note that, despite the increased R_{th}, the impact of SH on the analog FoMs is reduced at cryogenic temperatures, as discussed in the previous section. This phenomenon is well described by Eq. (1) and is caused by a flatter $I_d(T)$ curve that tends towards saturation below 100 K. Furthermore, our results agree qualitatively well with the ones obtained on similar devices but with a very different extraction approach (using gate resistance) [19]. Indeed, the authors observed that the differential thermal resistance does

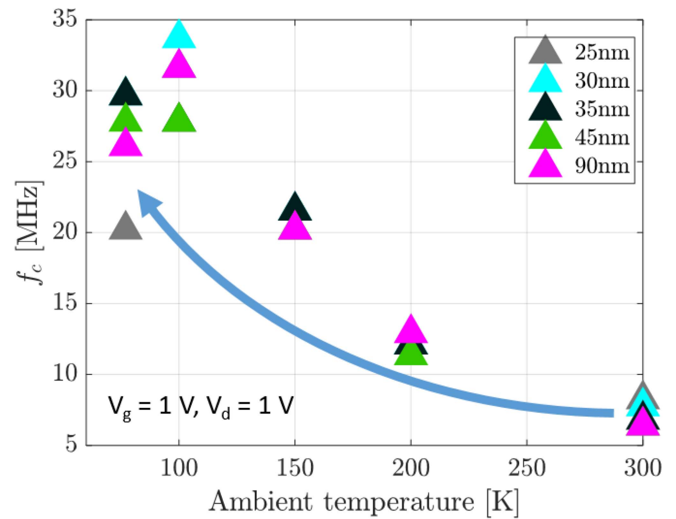


FIGURE 9. **Characteristic frequency of SH effect versus ambient temperature for different device lengths, at $V_d = V_g = 1$ V. f_c is extracted as in [24], such that $g_d(f_c) = g_d$(100 kHz) $+\Delta g_d/3$. The drawn arrow suggests a trend based on the data.**

not increase significantly for channel temperatures down to ~150 K on the UTBB MOSFETs.

V. CONCLUSION

A detailed analysis of the impact of self-heating on the output conductance, transconductance and intrinsic voltage gain of 25-to-90nm-long UTBB n-MOSFETs was carried out at cryogenic temperatures. It is shown that the performances of these analog FoMs are less degraded by self-heating at 77 K compared to 300 K. The voltage gain reduction due to SH is attenuated by 2 to 8%, depending on the gate length, when the ambient temperature goes to 77 K. Moreover, the dynamic-SH-free voltage gain is increased by 1-2 dB from 300 to 77 K, thanks to mobility enhancement and gate voltage overdrive decrease.

With temperature reduction down to 77 K, the SH characteristic frequency increases about four-fold, motivating the necessity of using the RF extraction method for SH effect over other conventional methods particularly at cryogenic temperatures.

Finally, the thermal resistance and channel temperature rise are extracted with the RF method at different ambient temperatures and gate lengths. Possible sources of uncertainty in the RF method are discussed and the determination of the isothermal frequency is identified as being the most sensitive parameter. However, our measurements and analyses agree well with other results of literature and extend them by studying the effect of dynamic self-heating and subsequently by including information about the complex thermal impedance. It is shown that the increase in R_{th} when temperature is reduced down to 77 K is more important for the longest devices than for the shortest ones, suggesting different dominant heat evacuation paths according to the gate length. Furthermore, neither R_{th} nor the temperature

rise vary much when temperature goes down to cryogenic temperatures for the shortest device lengths, demonstrating the ability of UTBB FDSOI MOSFETs for use at cryogenic temperatures for space applications or quantum computing.

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