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Comprehensive n- and pMOSFET Channel Material Benchmarking and Analysis of CMOS Performance Metrics Considering Quantum Transport and Carrier Scattering Effects

RASEONG KIM (Member, IEEE), UYGAR E. AVCI (Member, IEEE), AND IAN A. YOUNG (Life Fellow, IEEE)

Components Research, Intel Corporation, Hillsboro, OR 97124, USA

CORRESPONDING AUTHOR: R. KIM (e-mail: raseong.kim@intel.com)

ABSTRACT Comprehensive channel material benchmarking for n- and pMOS are performed considering effects of quantum transport and carrier scattering. Various channel material options (Si, InAs, $In_{0.7}Ga_{0.3}As$, $In_{0.53}Ga_{0.47}As$, GaAs, and Ge for nMOS, Si and Ge for pMOS) are covered using hybrid simulation of quantum ballistic transport and semi-classical Monte Carlo. Current-voltage characteristics and performance metrics such as the capacitance and effective drive current (I_{eff}) are explored considering device parasitic components. For low power operation, III-V nMOS may deliver good performance while Ge n- and pMOS with different source/drain tip designs may give performance advantage over Si from low power to high performance operations. CMOS benchmarking results for I_{eff}, capacitance, and switching energy vs. delay (for gate capacitance loading vs. interconnect wire capacitance loading) are also presented for various homogeneous and hybrid combinations of n- and pMOS (Si CMOS, III-V hybrid CMOS, Ge hybrid CMOS, and Ge CMOS). Finally, sensitivity analysis is performed for I_{eff} on the parasitic resistance (R_{SD}) and contact resistivity (ρ_c). Novel channel materials may relax the R_{SD} and ρ_c requirements to match the I_{eff} performance of Si reference. Comprehensive literature reviews of experimental ρ_c's of novel materials are also presented to discuss the effect of material-dependent R_{SD}.

INDEX TERMS III-V semiconductor materials, germanium, MOSFET, semiconductor device modeling, silicon.

I. INTRODUCTION

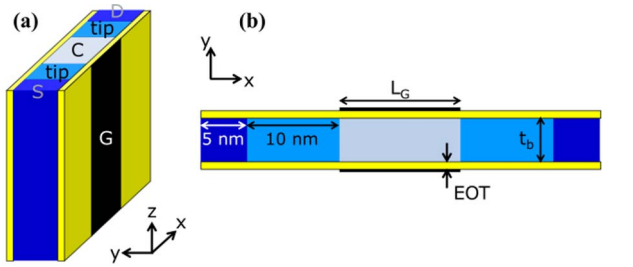
To continue the scaling of metal-oxide-semiconductor field-effect transistor (MOSFET) and satisfy performance metric requirements [1], novel channel materials such as III-V's and Ge are being actively explored [2]–[4]. The main motivation for such non-Si materials has been the high carrier mobility [5], which is expected to deliver high drive current in the classical point of view. For nanoscale MOSFETs, however, it is critical to treat all relevant physical effects (beyond the simple mobility-based model) such as quantum capacitance [6], tunneling [7], and ballistic transport [8] to correctly project the performance. For alternative materials such as III-V's and Ge, it is especially important to take a rigorous and comprehensive approach because the lighter electron or hole effective mass (m^*) makes those materials more susceptible to such novel physical effects (e.g., smaller quantum capacitance, larger tunneling current, and more ballistic carriers) [9]–[11].

There have been many previous theoretical studies on the performance projection of nanoscale MOSFETs with novel materials [12]–[25]. Those studies can be categorized into three groups depending on their simulation approach, i) semi-classical ballistic model [12]–[14], ii) semi-classical model including scattering effects [15]–[20], and iii) quantum transport model [21]–[25]. The semi-classical ballistic model [8], [26] provides an efficient way to quickly explore new channel materials while it does not capture advanced physical effects such as quantum tunneling and carrier scattering. The semi-classical model including scattering effects (such as Monte Carlo (MC) simulation [27]–[29]) has been

widely used to study MOSFETs considering various carrier scattering mechanisms such as electron-phonon (e-ph), impurity, and surface roughness scattering. While it provides quantum correction models to capture some of quantum mechanical effects (e.g., threshold voltage (V_{th}) shift due to quantum confinement), it is still challenging to treat quantum effects rigorously within this framework. For example, conventional MC simulation cannot treat tunneling effects, which can be critical to the OFF-state leakage of novel channel materials (lighter m^*, more tunneling) [11]. This may significantly limit the usability of MC simulation to benchmark the OFF-state performance, in addition to the well-known issue of large statistical noise in the OFF-state, which is inherent to the MC approach. The quantum transport approach is most rigorous in treating quantum mechanical effects such as tunneling while it bears a high numerical cost. In principle, it is possible to treat carrier scattering, but most of quantum transport studies [22]–[25] assume ballistic transport because it can be very expensive to treat even a basic scattering mechanism (such as e-ph).

Most of previous benchmarking studies focused on n-type MOSFET [12], [15]–[23] while few of them reported both n-type MOSFET (nMOS) and p-type MOSFET (pMOS) results [14], [25]. Also, in many of previous studies [15]–[19], [21], [23], the performance benchmarking was done for current-voltage (I-V) characteristics of intrinsic transistors, which is indeed important but may be only a part of the overall circuit performance. We should consider relevant parasitic components such as source/drain resistance (R_{SD}) and parasitic capacitance (C_{par}). To project the device performance in the circuit context, it is important to treat both n- and pMOS and explore complementary MOS (CMOS) performance metrics such as power consumption and switching delay, beyond the simple transistor-level I-V's.

In this paper, we perform comprehensive channel material benchmarking for n- and pMOS at a relevant technology node from the International Technology Roadmap on Semiconductors (ITRS) [1], [30]. The results are based on the hybrid simulation of quantum ballistic transport [31] and MC to capture both effects of quantum transport and carrier scattering. We cover a wide range of channel material options, Si, InAs, $In_{0.7}Ga_{0.3}As$, $In_{0.53}Ga_{0.47}As$, GaAs, and Ge for nMOS, and Si and Ge for pMOS. Comprehensive $I-V$ and capacitance characteristics for n- and pMOS are discussed considering parasitic components such as R_{SD}, contact resistivity (ρ_c), and C_{par}. We also report energy vs. delay for various cases of homogeneous CMOS (same material for n- and pMOS) and hybrid CMOS (different materials for n- and pMOS) for different capacitance loading scenarios (gate capacitance vs. interconnect wire capacitance). The main goal of this paper is to provide a comprehensive and comparative performance projection for various channel material options considering fundamental physics of each material (such as quantum and scattering effects) while keeping other factors (such as device dimensions and parasitics) on an equal footing.



(c)

L_G	EOT	t_b	x	y	z
13 nm	0.8 nm	4.7 nm	[110]	[$\bar{1}$10]	[001]

FIGURE 1. Structure and device parameters of L_G = 13 nm thin-body DG MOSFET. (a) Three-dimensional view with gate (G), source (S), channel (C), and drain (D) regions labeled. (b) Cross-sectional view along the transport (x) and confinement (y) directions. (c) Device parameters and crystal orientations.

This paper is organized as follows. In Section II, we explain the model device, simulation approach, and performance metrics. In Sections III and IV, we present benchmarking results for nMOS and pMOS, respectively. In Section V, we compare CMOS performance metrics for various cases of homogeneous and hybrid combinations of n- and pMOS. In Section VI, we review material-dependent ρ_c's reported in literatures and discuss the sensitivity of the drive current to the R_{SD} and ρ_c. In Section VII, we conclude this paper.

II. APPROACH

A. MODEL DEVICE

Fig. 1(a)-(b) shows the model device diagram. We assume thin-body double-gate (DG) MOSFETs with a gate length (L_G) of 13 nm [1]. Device parameters such as the equivalent oxide thickness (EOT), body thickness (t_b), and crystal orientations are also shown in Fig. 1(c). (For the crystal orientation, we assume the conventional case of present-day CMOS. While it is beyond the scope of this paper, performing a similar channel material benchmarking for other technologically relevant crystal orientations [32]–[36] will be a useful future study.)

The source/drain (S/D) design is essential to realize the optimum performance of each channel material as discussed in previous studies [11], [24], [25]. In this study, we take the S/D tip doping density (N_{tip}) as a knob to balance the source exhaustion (ON-state performance) vs. tunneling leakage (OFF-state performance) [11]. For materials with small band gap (E_g) and light m^* such as III-V's and Ge, small N_{tip} tends to help prevent large tunneling leakage. For materials with large E_g and heavy m^* such as Si, large N_{tip} is preferable because it maximizes the ON-current (minimizes source exhaustion) while the tunneling leakage is less of a concern. For the S/D doping density (N_{SD}), we assume high values (as allowed by the dopant solubility) like in practical devices to reduce R_{SD}. In Fig. 1(b), the length of the highly doped

TABLE 1. List of n- and pMOS channel materials and doping densities considered for each material.

nMOS	Si	InAs	$In_{0.7}Ga_{0.3}As$	$In_{0.53}Ga_{0.47}As$	GaAs	Ge
N_{tip} (cm^{-3})	**10^{20}** 2×10^{20}	10^{19}	**10^{19}**	**10^{19}** 5×10^{19}	**2×10^{19}** 5×10^{19}	**10^{19}** **2×10^{19}** **5×10^{19}**
N_{SD} (cm^{-3})	2×10^{20}	5×10^{19}	5×10^{19}	5×10^{19}	5×10^{19}	10^{20}

pMOS	Si	Ge
N_{tip} (cm^{-3})	**10^{20}**, 2×10^{20}	**10^{19}**, **2×10^{19}**, **5×10^{19}**
N_{SD} (cm^{-3})	2×10^{20}	10^{20}

region (5 nm) is chosen so that it is long enough to maintain flat potential profiles at S/D ends while minimizing the simulation domain size. The channel is un-doped.

Table 1 shows the list of n- and pMOS channel materials and doping densities (N_{tip} and N_{SD}) considered for each material. For some materials such as $In_{0.53}Ga_{0.47}As$ and Ge, we treat multiple cases of N_{tip} to i) illustrate the effect of non-optimum, large N_{tip} on materials with small E_g and light m^* and ii) discuss N_{tip} splits optimized for different operating conditions, e.g., high performance (HP) and low power (LP). In Table 1, the N_{tip} values in bold indicate the cases we focus on for the performance benchmarking in Sections III–V.

B. SIMULATION APPROACH

As mentioned in Section I, we take a hybrid approach of atomistic quantum ballistic simulation and MC simulation. Below we go through each of the two simulation models and explain how they are combined to produce the final result.

B.1. ATOMISTIC QUANTUM BALLISTIC SIMULATION

In this study, atomistic quantum ballistic simulation [31] using $sp^3s^*d^5$ tight-binding (TB) model [37], [38] is the main tool to calculate the $I-V$ and capacitance characteristics of intrinsic MOSFETs. (The TB approach has been widely used to calculate band structures of cubic [39] and wurtzite [40] semiconductors while the model is applicable to a wide variety of crystals [41].) For the TB model in this study, spin-orbit coupling is not included for numerical simplicity. All simulations are done for 300 K. The MOSFET current is scaled by a factor of 2 to account for the effective width (W_{eff}) of DG structure.

Our quantum transport simulation captures essential physical effects such as quantum confinement and tunneling, but it is still missing another important effect – carrier scattering. While the relative importance of carrier scattering may decrease as the device dimension shrinks (i.e., as the device becomes more ballistic), it is expected to remain as an important part to project the $I-V$ performance at $L_G = 13$ nm, especially for materials with high m^* and large density-of-states (DOS) such as Si because they have high carrier scattering rates. As mentioned in Section I, however, it is challenging to incorporate carrier scattering models into the quantum transport simulation framework due to numerical burdens. Because we are dealing with a wide variety of materials with multiple design options as shown in Table 1, it is even more impractical to introduce the carrier scattering model directly into our quantum simulation framework. Therefore, we take a new hybrid approach - we run MC simulation and extract correction factors that comprehend carrier scattering effects. These correction factors are then applied to the ballistic $I-V$ results from the quantum simulation. More details about the MC simulation and correction factor extraction are discussed in the following section.

B.2. MONTE CARLO SIMULATION AND HYBRID APPROACH

As a correction factor to comprehend the carrier scattering effect, we calculate the ballistic ratio (BR) [42], [43], which is defined as $BR = I_{scatt}/I_{ball}$, where I_{ball} and I_{scatt} represent the ballistic current (with no carrier scattering) and current with carrier scattering, respectively. $BR = 1$ means the ballistic limit, and $BR < 1$ means that the current is lost due to carrier scattering.

To calculate BR, we run two sets of MC simulation, with carrier scattering turned off (for I_{ball}) and turned on (for I_{scatt}), for each device in Table 1. For nMOS (Si, InAs, $In_{0.7}Ga_{0.3}As$, $In_{0.53}Ga_{0.47}As$, GaAs, and Ge), we run in-house quantum-corrected MC simulation considering e-ph and impurity scattering. The main strength of the in-house MC simulator is that it can treat advanced quantum correction effects (e.g., valley separations due to quantum confinement [44]), which are expected to be significant in III-V and Ge nMOS. (One thing to note here is that the in-house MC tool has been established for nMOS while it is still in development for pMOS. A related paper is to be published elsewhere by the tool developers.) For pMOS (Si and Ge), we run full-band MC simulation using Sentaurus Device Monte Carlo [45]. And then the BR is obtained at each bias condition as

$$BR(V_G, V_D) = I_{scatt,MC}(V_G, V_D) \big/ I_{ball,MC}(V_G, V_D), \quad (1)$$

where V_G (V_D) is the gate (drain) voltage, and $I_{ball,MC}$ ($I_{scatt,MC}$) is the I_{ball} (I_{scatt}) from the MC simulation. In the Appendix, we show some example MC simulation results for $BR(V_G, V_D)$ and discuss more details.

The BR in (1) is then applied to the ballistic $I-V$ results from the quantum transport simulation as

$$I_{scatt,QT}(V_G, V_D) = I_{ball,QT}(V_G, V_D) \times BR(V_G, V_D), \quad (2)$$

where $I_{ball,QT}$ means I_{ball} from the quantum transport (QT) simulation, and $I_{scatt,QT}$ is the current after the BR correction. The $I_{scatt,QT}(V_G, V_D)$ in (2) represents the final $I-V$ result for the intrinsic MOSFET including effects of both quantum transport and carrier scattering.

One thing to note here is that the BR correction in (2) applies only to the ON-state. In the OFF-state, as mentioned in Section I, MC simulation has two issues. First, it does not capture quantum transport effects (such as tunneling) that are critical to the OFF-state leakage. Secondly, it is prone to statistical errors due to the limited number of carriers

in the OFF-state. Meanwhile, other simulation studies of tunneling devices including the carrier scattering effect [46] suggest that the OFF-state currents are not affected much by carrier scattering. Therefore, in this study, we take the $I-V$ results in the OFF-state as given from the quantum transport simulation while we apply the *BR* correction in the ON-state as shown in (2).

C. PERFORMANCE METRICS

In this section, we explain how we extract performance metrics from the device simulation result. First, we include the effect of R_{SD} in the $I-V$'s. We mainly assume $R_{SD} = 200\ \Omega\text{-}\mu\text{m}$ (for W_{eff}, including effects of both source and drain), a typical value for present-day transistors [1]. (In Section VI, we perform sensitivity analysis and discuss more aspects of R_{SD} effects. We also note that R_{SD} may depend on the geometric structure of S/D contacts, especially for small-m^* materials [47], [48], while we assume idealized contact structures in this study.) From the final $I-V$'s including all relevant effects (quantum transport, carrier scattering, and R_{SD}), we can extract various performance metrics, such as the effective inverter drive current [49]

$$I_{eff} = (I_H + I_L)/2, \tag{3}$$

where I_H and I_L are defined as

$$I_H = \begin{cases} I_D\left(V_G = V_{\rm DD}, V_D = V_{\rm DD}/2\right) & (\text{for nMOS}) \\ I_D\left(V_G = -V_{\rm DD}, V_D = -V_{\rm DD}/2\right) & (\text{for pMOS}) \end{cases}, \tag{4a}$$

$$I_L = \begin{cases} I_D\left(V_G = V_{\rm DD}/2, V_D = V_{\rm DD}\right) & (\text{for nMOS}) \\ I_D\left(V_G = -V_{\rm DD}/2, V_D = -V_{\rm DD}\right) & (\text{for pMOS}) \end{cases}, \tag{4b}$$

where I_D is the drain current, and $V_{\rm DD}$ is the supply voltage.

In addition to $I-V$'s, capacitance characteristics are also important to project the CMOS performance. In this study, they are directly obtained from the device simulation, by integrating the charge density within the model device in Fig. 1. As a key metric, we define C_{eff} [24] as

$$C_{eff} = \begin{cases} \left[Q_G(V_G = V_{\rm DD}, V_D = 0)\right] \Big/ V_{\rm DD}\ (\text{for nMOS}) \\ -\left[Q_G(V_G = -V_{\rm DD}, V_D = 0)\right] \Big/ V_{\rm DD}\ (\text{for pMOS}) \end{cases}, \tag{5}$$

where Q_G is the total gate charge. This C_{eff} represents the average gate capacitance for a given $V_{\rm DD}$, where the Miller effect is inherently included. In addition to the C_{eff} of the intrinsic device ($C_{eff,dev}$), we also include C_{par}, which mainly comes from the external fringing capacitance from the gate to the source and drain contacts. Therefore, the final C_{eff} becomes $C_{eff,dev} + C_{par}$. In this study, we assume $C_{par} = 0.6\ \text{fF}/\mu\text{m}$ (similar to the ITRS node of year 2018 [30], including the gate-to-source and gate-to-drain overlaps, fringing capacitances, and the Miller effect) as a representative case for benchmarking [24], [25].

From the current and capacitance metrics above, we can readily calculate the switching energy and delay metrics for CMOS circuits considering both n- and pMOS. For example, the I_{eff} of an inverter circuit ($I_{eff,n+p}$) is defined as

$$1/I_{eff,n+p} = 1/I_{eff,n} + 1/I_{eff,p}, \tag{6}$$

where $I_{eff,n}$ and $I_{eff,p}$ represent the I_{eff} of n- and pMOS, respectively. (Equation (6) physically means the sum of n- and pMOS delays for a constant capacitance load [50].) In this study, we assume that n- and pMOS have the same device width. The C_{eff} for the inverter circuit ($C_{eff,n+p}$) can be also defined as [25],

$$C_{eff,n+p} = C_{eff,n} + C_{eff,p}, \tag{7}$$

where $C_{eff,n}$ and $C_{eff,p}$ represent the C_{eff} of n- and pMOS, respectively. The switching energy (CV^2) of the CMOS inverter is calculated as

$$CV^2 = C_{load} V_{\rm DD}^2, \tag{8}$$

where C_{load} means the loading capacitance. For C_{load}, we consider two cases, i) $C_{load} = C_{eff,n+p}$ ("gate capacitance loading"), and ii) $C_{load} = C_{wire}$ ("wire capacitance loading"), where C_{wire} means a constant capacitance coming from interconnect wires. In reality, C_{load} may come from both the gate and wire, so the result will lie in-between our two extreme case results. The CMOS inverter delay (CV/I) is calculated as [25]

$$CV/I = C_{load} V_{\rm DD}/I_{eff,n+p}, \tag{9}$$

where we also consider two scenarios for C_{load} (gate vs. wire).

III. NMOS BENCHMARKING

In this section, we report benchmarking results for various nMOS channel material options. We first present $I-V$ results and discuss OFF- and ON-state characteristics. And then we present performance metrics, $I_{eff,n}$ and $C_{eff,n}$, introduced in Section II.

A. I-V CHARACTERISTICS

In Fig. 2, we show simulation results for I_D vs. V_G at different V_D's (with no R_{SD}) for Si, InAs, $In_{0.7}Ga_{0.3}As$, $In_{0.53}Ga_{0.47}As$, GaAs, and Ge nMOS. For each case (except for InAs), the gate work function (WF) is adjusted to give the OFF-current (I_{OFF}) of 5 nA/μm at $V_G = 0$ V and $V_D = V_{\rm DD}$, where $V_{\rm DD} = 0.7$ V. (For InAs, it is not possible to meet the I_{OFF} target even with a small N_{tip}.) The OFF-state characteristics may dramatically change depending on the material and V_D. For Si nMOS (Fig. 2(a)), good subthreshold swing (SS) and drain-induced barrier lowering (DIBL) may be achieved. For InAs (Fig. 2(b)), however, tunneling leakage is so high (especially at high V_D) that it cannot be a good nMOS option that meets a reasonable I_{OFF} target. $In_{0.7}Ga_{0.3}As$ nMOS (Fig. 2(c)) is better than InAs, but still the leakage becomes very high as V_D increases. When N_{tip} is optimized, $In_{0.53}Ga_{0.47}As$ nMOS can be an option for nominal V_D operation as shown in Fig. 2(d) while it may still

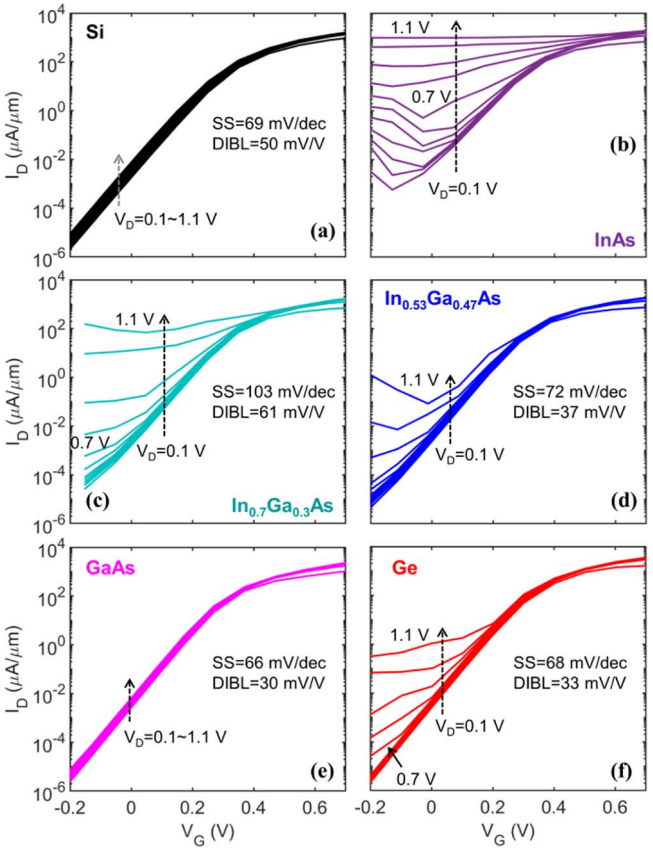


FIGURE 2. Simulation results for I_D vs. V_G (I_{OFF} = 5 nA/μm at V_{DD} = 0.7 V, no R_{SD}) for nMOS. Extracted *SS* (around V_G = 0 V at V_D = 0.7 V) and DIBL (from V_{th} difference between V_D = 0.1 V and 0.7 V) are shown on the graph when available. (a) Si (10^{20}), (b) InAs (10^{19}), (c) $In_{0.7}Ga_{0.3}As$ (10^{19}), (d) $In_{0.53}Ga_{0.47}As$ (10^{19}), (e) GaAs (2 × 10^{19}), (f) Ge (2 × 10^{19}). The value in () is N_{tip} in cm^{-3}.

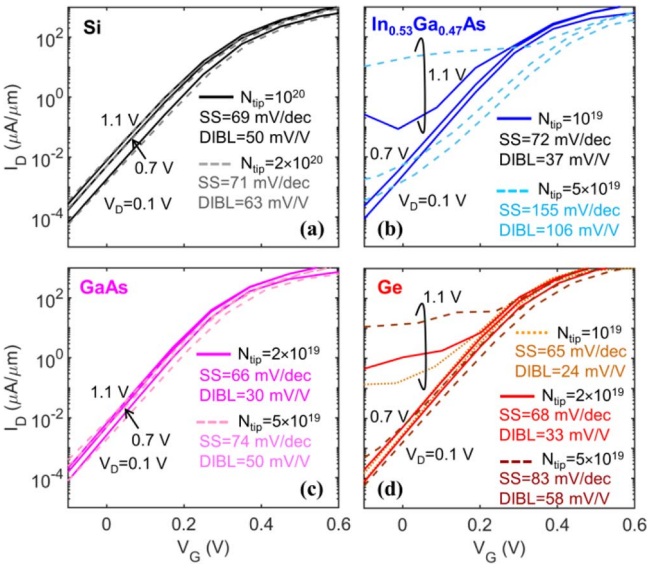


FIGURE 3. Simulation results for I_D vs. V_G (I_{OFF} = 5 nA/μm at V_{DD} = 0.7 V, no R_{SD}) for nMOS with different N_{tip}'s. Extracted *SS* (around V_G = 0 V at V_D = 0.7 V) and DIBL (from V_{th} difference between V_D = 0.1 V and 0.7 V) are shown on the graph. (a) Si (10^{20}, 2 × 10^{20}), (b) $In_{0.53}Ga_{0.47}As$ (10^{19}, 5 × 10^{19}), (c) GaAs (2 × 10^{19}, 5 × 10^{19}), (d) Ge (10^{19}, 2 × 10^{19}, 5 × 10^{19}). The value in () is N_{tip} in cm^{-3}.

suffer from the high leakage at high V_D. For GaAs nMOS (Fig. 2(e)), good *SS* and DIBL are achieved, and it does not suffer from high leakage due to the large E_g [5]. Finally, Ge nMOS (Fig. 2(f)) shows characteristics that are similar to those of $In_{0.53}Ga_{0.47}As$ nMOS – it meets the I_{OFF} target at nominal V_D while it gives high leakage as V_D increases.

In Fig. 3, to explore the effect of N_{tip} on the OFF-state characteristics, we show I_D vs. V_G for Si, $In_{0.53}Ga_{0.47}As$, GaAs, and Ge nMOS with different N_{tip}'s. For Si nMOS (Fig. 3(a)), *SS* and DIBL do not change much with N_{tip}. For $In_{0.53}Ga_{0.47}As$ nMOS (Fig. 3(b)), however, *SS* degrades significantly as N_{tip} increases. (Note that the high N_{tip} gives even worse results for InAs or $In_{0.7}Ga_{0.3}As$ nMOS (not shown) due to the smaller E_g and lighter m^* [5].) For GaAs nMOS (Fig. 3(c)), *SS* and DIBL do not change much with N_{tip}. For Ge nMOS (Fig. 3(d)), *SS* increases as N_{tip} increases while the degradation is not as severe as in $In_{0.53}Ga_{0.47}As$. Therefore, for Ge nMOS, depending on the operating condition (V_{DD} and I_{OFF}), it may be an option to increase N_{tip} to boost the ON-current (less source exhaustion) with some sacrifice of *SS* in the OFF-state [25].

Fig. 4 shows I_D vs. V_D at different V_G's for Si, $In_{0.53}Ga_{0.47}As$, GaAs, and Ge nMOS. (InAs and $In_{0.7}Ga_{0.3}As$ nMOS are not explored anymore due to the leakage current issue discussed in Fig. 2.) For each device, we show $I-V$ results including the carrier scattering effect (*BR* correction, solid lines) along with ballistic $I-V$'s (dashed lines). We show intrinsic results ($R_{SD} = 0$) and final $I-V$'s including R_{SD} = 200 Ω-μm. In Fig. 4, we can clearly see the material-dependent carrier scattering effect. For Si, I_D decreases significantly after the *BR* correction. For example, in the result including R_{SD} (Fig. 4(b)), I_D's at V_G = 0.7 V, V_D = 0.1 V (I_{Dlin}) and $V_G = V_D$ = 0.7 V (I_{Dsat}) are reduced by 43 % (*BR*∼0.57) and 29 % (*BR*∼0.71), respectively. For $In_{0.53}Ga_{0.47}As$, however, $I-V$'s do not change much with carrier scattering because it operates close to the ballistic limit. For example, I_{Dlin} and I_{Dsat} are reduced by 2 % (*BR*∼0.98) and 1 % (*BR*∼0.99), respectively (Fig. 4(d)). For GaAs, the scattering effect is larger than in $In_{0.53}Ga_{0.47}As$ but still much smaller than in Si. The I_{Dlin} and I_{Dsat} are reduced by 8 % (*BR*∼0.92) and 6 % (*BR*∼0.94), respectively (Fig. 4(f)). For Ge, results depend on N_{tip}. For a low N_{tip}, I_{Dlin} and I_{Dsat} decrease by 15 % (*BR*∼0.85) (Fig. 4(h)). For a high N_{tip}, I_{Dlin} and I_{Dsat} are reduced less, by 10 % (*BR*∼0.9) and 14 % (*BR*∼0.86), respectively (Fig. 4(j)). (See the Appendix for more discussions on the material, N_{tip}, and bias dependence of *BR*.)

B. PERFORMANCE METRICS: $I_{EFF,N}$ AND $C_{EFF,N}$

Fig. 5 shows $I_{eff,n}$ vs. V_{DD} for the ballistic case and for the final result with *BR* correction. R_{SD} = 200 Ω-μm is included in all cases. Along with the absolute values of

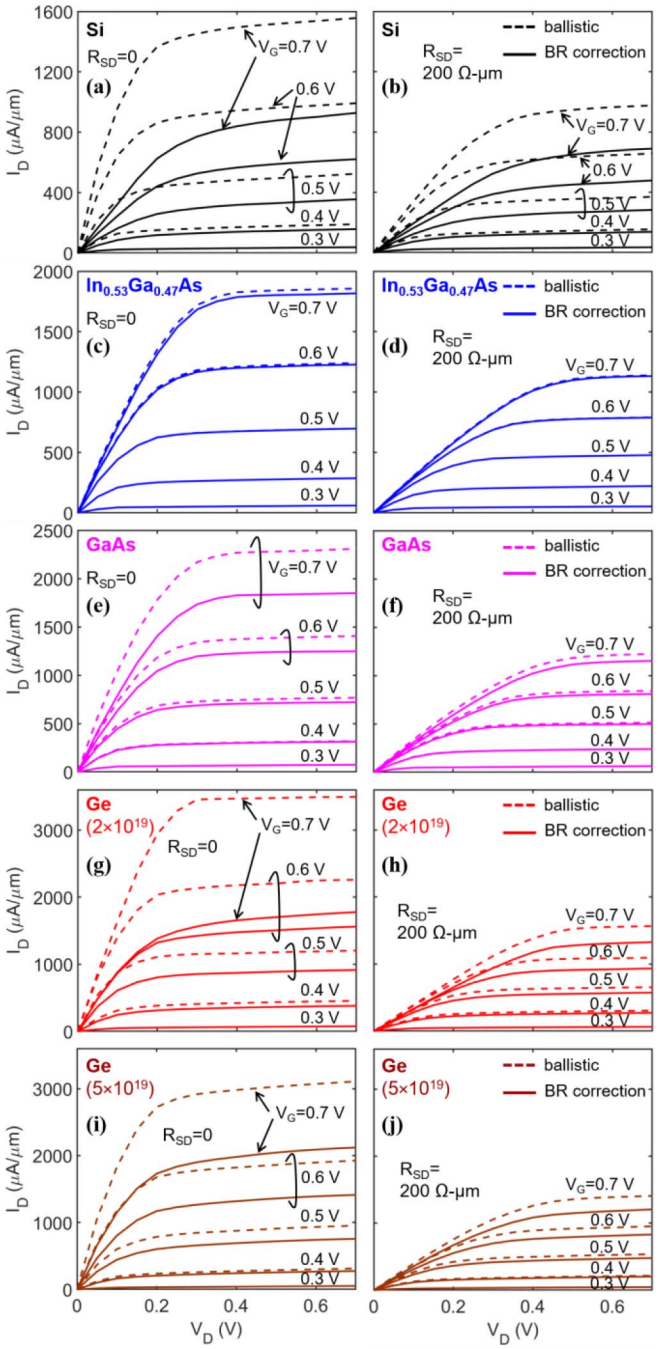


FIGURE 4. Simulation results for I_D vs. V_D (I_{OFF} = 5 nA/μm at V_{DD} = 0.7 V) for nMOS. (a)-(b) Si (10^{20}), (c)-(d) $In_{0.53}Ga_{0.47}As$ (10^{19}), (e)-(f) GaAs (2×10^{19}), (g)-(j) Ge (2×10^{19}, 5×10^{19}). The value in () is N_{tip} in cm^{-3}. For each device, $I-V$ results with *BR* correction (solid lines) are shown along with ballistic results (dashed lines) with R_{SD} = 0 (left column) and R_{SD} = 200 Ω-μm (right column).

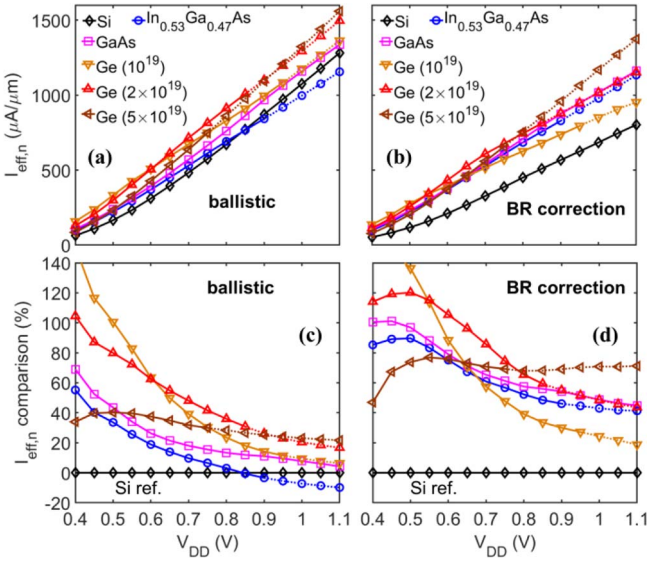


FIGURE 5. Simulation results for $I_{eff,n}$ vs. V_{DD} (I_{OFF} = 5 nA/μm at V_{DD} = 0.7 V) of Si (10^{20}), $In_{0.53}Ga_{0.47}As$ (10^{19}), GaAs (2×10^{19}), and Ge nMOS (10^{19}, 2×10^{19}, 5×10^{19}) (a) for the ballistic case and (b) with *BR* correction. The value in () is N_{tip} in cm^{-3}. R_{SD} = 200 Ω-μm is included in all cases. (c)-(d) Relative comparison with Si reference at each V_{DD}.

$I_{eff,n}$, we also report the relative comparison result against the Si reference at each V_{DD} (0 % baseline in Fig. 5(c)-(d)). For $In_{0.53}Ga_{0.47}As$, while it crosses over Si at high V_{DD} in the ballistic case due to the DOS bottleneck [9], it maintains improvement over Si when the scattering effect is considered. This is because the *BR* is higher for $In_{0.53}Ga_{0.47}As$, i.e., current loss due to carrier scattering is less than in Si. For GaAs nMOS, the $I_{eff,n}$ improvement over Si is larger than in $In_{0.53}Ga_{0.47}As$ and maintained at high V_{DD} (no cross-over) even in the ballistic case (due to the improved DOS), and the relative improvement over Si further increases when the scattering effect is included (*BR* higher than in Si). For Ge nMOS, $I_{eff,n}$ is improved over Si at all V_{DD}'s in the ballistic case, and the relative improvement becomes larger when *BR* is considered. One thing to note here is that for Ge nMOS, depending on the operating condition, a different N_{tip} may be chosen to deliver the best performance [25]. As shown in Fig. 5(b),(d), Ge nMOS with a low N_{tip} gives the best $I_{eff,n}$ at low V_{DD} (up to ~0.55 V). As V_{DD} increases, Ge nMOS with a medium N_{tip} becomes best (up to ~0.8 V). As V_{DD} increases further (>0.8 V), Ge nMOS with a large N_{tip} gives the largest $I_{eff,n}$ (while it may have a leakage problem, see Fig. 6).

One important point to acknowledge here is that in Fig. 5, the gate WF is adjusted to meet the I_{OFF} target at a certain V_{DD} ($I_{OFF,target}$ = 5 nA/μm at V_G = 0 V and V_D = 0.7 V), and the same gate WF is used for all other V_{DD} operations. Therefore, the actual OFF-current ($I_{OFF,actual}$) at different V_{DD}'s may be different than the $I_{OFF,target}$. In Fig. 6, we show $I_{OFF,actual}$ (I_D at V_G = 0 V and $V_D = V_{DD}$) for the cases in Fig. 5. At V_{DD} = 0.7 V, all devices meet the I_{OFF} target as intended. For V_{DD} < 0.7 V, $I_{OFF,actual} < I_{OFF,target}$. For V_{DD} > 0.7 V, $I_{OFF,actual} > I_{OFF,target}$ for all devices while the behaviors are quite different depending on the material. For Si nMOS, the $I_{OFF,actual}$ increases gradually as V_{DD} increases due to the classical short channel effect (SCE). For $In_{0.53}Ga_{0.47}As$, the $I_{OFF,actual}$ first increases gradually

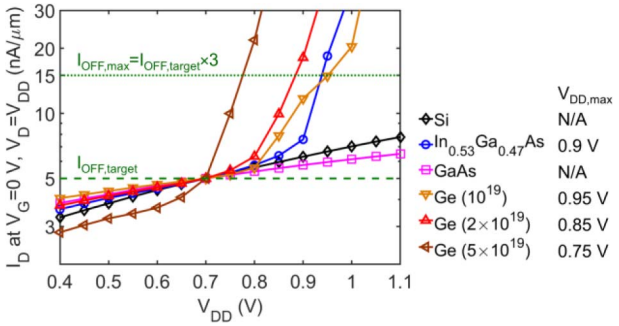


FIGURE 6. Simulation results for $I_{OFF,actual}$ (I_D at $V_G = 0$ V and $V_D = V_{DD}$) vs. V_{DD} for the nMOS cases in Fig. 5. The $I_{OFF,target}$ (5 nA/μm) and the upper limit of allowed I_{OFF} ($I_{OFF,max} = 3 \times I_{OFF,target}$) are also shown for reference. $V_{DD,max}$ to satisfy the $I_{OFF,max}$ condition is also shown for each nMOS (where N/A means that $I_{OFF,actual}$ does not exceed $I_{OFF,max}$ in all V_{DD} range of interest).

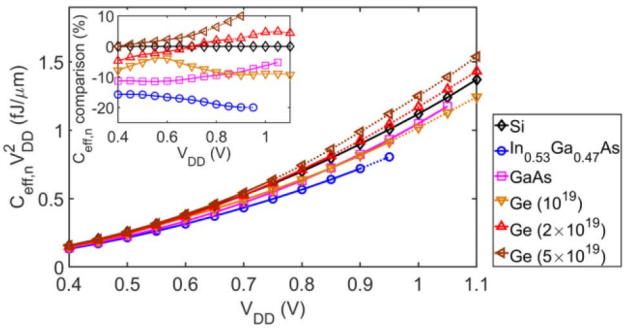


FIGURE 7. Simulation results for $C_{eff,n}V_{DD}^2$ vs. V_{DD} ($I_{OFF} = 5$ nA/μm at $V_{DD} = 0.7$ V) of Si (10^{20}), $In_{0.53}Ga_{0.47}As$ (10^{19}), GaAs (2×10^{19}), and Ge nMOS (10^{19}, 2×10^{19}, 5×10^{19}). The value in () is N_{tip} in cm^{-3}. $C_{par} = 0.6$ fF/μm is considered in all cases. (inset) Relative comparison with Si reference at each V_{DD}.

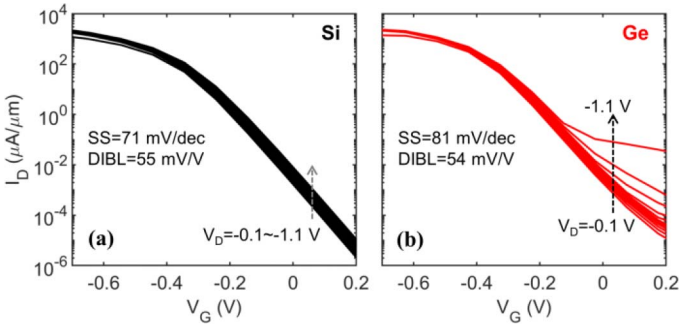


FIGURE 8. Simulation results for I_D vs. V_G at different V_D's ($I_{OFF} = 5$ nA/μm at $V_{DD} = 0.7$ V, no R_{SD}) for pMOS. Extracted *SS* (around $V_G = 0$ V at $V_D = -0.7$ V) and DIBL (from V_{th} difference between $V_D = -0.1$ V and -0.7 V) are also shown on the graph. (a) Si ($N_{tip} = 10^{20}$ cm^{-3}) and (b) Ge pMOS ($N_{tip} = 2 \times 10^{19}$ cm^{-3}).

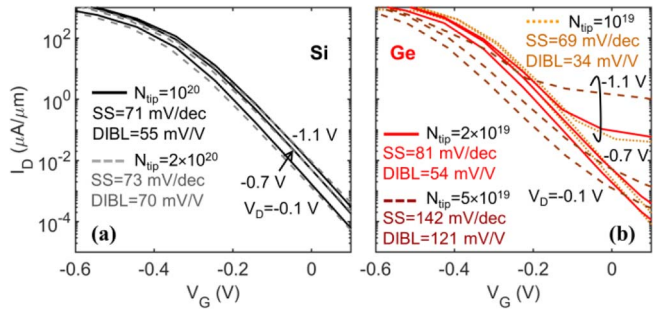


FIGURE 9. Simulation results for I_D vs. V_G ($I_{OFF} = 5$ nA/μm at $V_{DD} = 0.7$ V, no R_{SD}) for Si (N_{tip}=10^{20}, 2×10^{20} cm^{-3}) and Ge pMOS (N_{tip}=10^{19}, 2×10^{19}, 5×10^{19} cm^{-3}). Extracted *SS* (around $V_G = 0$ V at $V_D = -0.7$ V) and DIBL (from V_{th} difference between $V_D = -0.1$ V and -0.7 V) are also shown on the graph.

with V_{DD} (classical SCE). As V_{DD} increases further, however, $I_{OFF,actual}$ increases quickly due to tunneling leakage (e.g., band-to-band tunneling (BTBT)). To avoid high leakage problems, there should be some upper limit of $I_{OFF,actual}$ ($I_{OFF,max}$), which will also set the maximum allowed V_{DD} ($V_{DD,max}$). In this study, we assume $I_{OFF,max} = 3 \times I_{OFF,target}$ (while it can vary depending on the application). As shown in Fig. 6, Si nMOS does not hit this upper limit in the V_{DD} range of interest. $In_{0.53}Ga_{0.47}As$ nMOS, however, goes above this upper limit beyond $V_{DD,max} \sim 0.9$ V. For GaAs, $I_{OFF,actual}$ increases gradually with V_{DD} and does not go above the upper limit (large E_g, no BTBT). For Ge nMOS, the behavior depends on N_{tip}. As N_{tip} increases, $I_{OFF,actual}$ goes above the upper limit at a lower V_{DD} ($V_{DD,max} \sim 0.95$, 0.85 and 0.75 V for $N_{tip} = 10^{19}$, 2×10^{19}, and 5×10^{19} cm^{-3}, respectively). Note that in Fig. 5 and all subsequent figures for nMOS (Fig. 7, Fig. 21), V_{DD} data points beyond $V_{DD,max}$ are plotted using dotted lines.

In Fig. 7, we show $C_{eff,n}V_{DD}^2$ vs. V_{DD} and the relative comparison with Si reference at each V_{DD}. We note that the capacitance results are not affected by R_{SD} or carrier scattering because they are electrostatic properties [24]. $In_{0.53}Ga_{0.47}As$ nMOS shows the lowest capacitance due to the low N_{tip} and small DOS. For GaAs, $C_{eff,n}$ is somewhat lower than the Si reference. For Ge nMOS. $C_{eff,n}$ is lower than the Si reference for a low N_{tip} while it becomes comparable to Si for higher N_{tip}'s.

IV. PMOS BENCHMARKING

In this section, we report benchmarking results for pMOS channel material options. We first present $I-V$ results and discuss OFF- and ON-state characteristics. And then we present performance metrics, $I_{eff,p}$ and $C_{eff,p}$, introduced in Section II.

A. I-V CHARACTERISTICS

In Fig. 8, we show simulation results for I_D vs. V_G at different V_D's for Si and Ge pMOS ($I_{OFF} = 5$ nA/μm at $V_G = 0$ V and $V_D = -0.7$ V with no R_{SD}). The OFF-state characteristics change significantly depending on the material and V_D. For Si pMOS (Fig. 8(a)), good *SS* and DIBL are achieved. For Ge pMOS (Fig. 8(b)), *SS* and DIBL are decent at nominal V_D's while the leakage current may increase significantly at high V_D's.

In Fig. 9, we show I_D vs. V_G for Si and Ge pMOS with different N_{tip}'s. For Si pMOS (Fig. 9(a)), *SS* and DIBL do not change much with N_{tip}. For Ge pMOS (Fig. 9(b)), *SS*

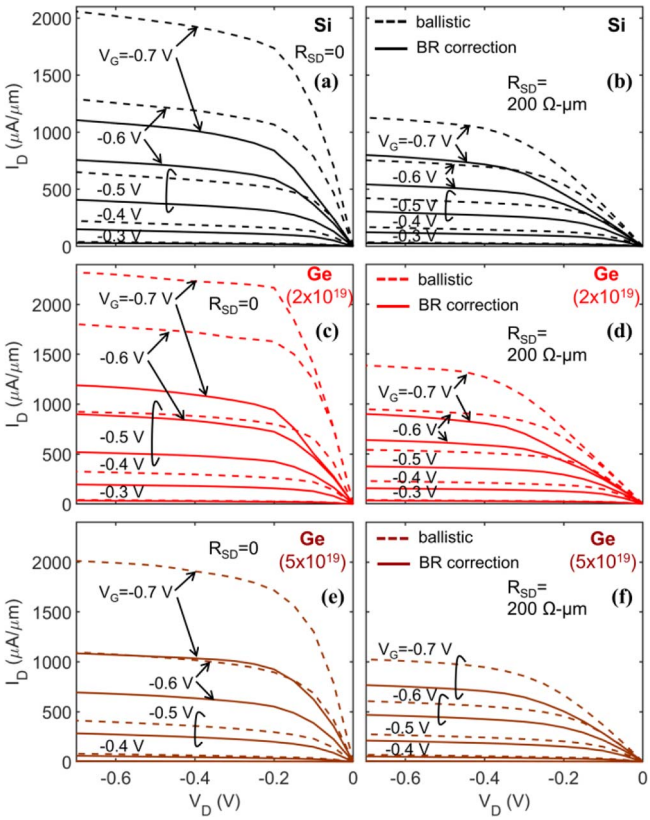


FIGURE 10. Simulation results for I_D vs. V_D at different V_G's (I_{OFF} = 5 nA/μm at V_{DD} = 0.7 V) for (a)-(b) Si ($N_{tip} = 10^{20}$ cm^{-3}) and (c)-(f) Ge pMOS ($N_{tip} = 2 \times 10^{19}$, 5×10^{19} cm^{-3}). For each device, $I-V$ results with *BR* correction (solid lines) are shown along with ballistic results (dashed lines) with $R_{SD} = 0$ (left column) and $R_{SD} = 200$ Ω-μm (right column).

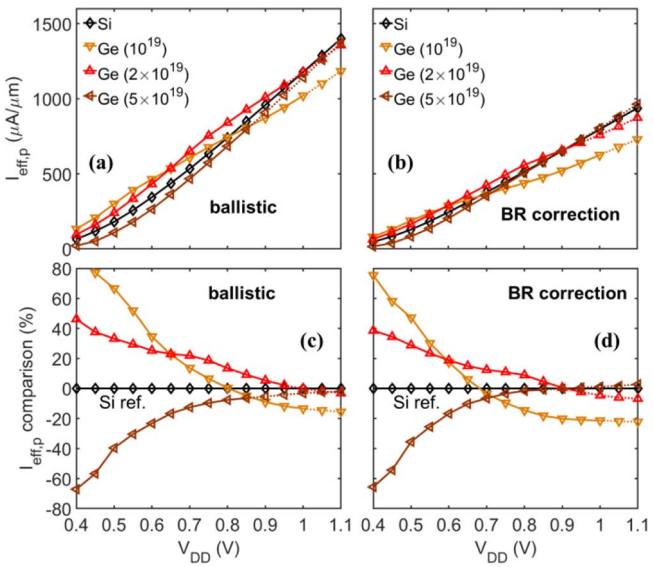


FIGURE 11. Simulation results for $I_{eff,p}$ vs. V_{DD} (I_{OFF} = 5 nA/μm at V_{DD} = 0.7 V) of Si ($N_{tip} = 10^{20}$ cm^{-3}) and Ge pMOS ($N_{tip} = 10^{19}$, 2×10^{19}, 5×10^{19} cm^{-3}) (a) for the ballistic case and (b) with *BR* correction. R_{SD} = 200 Ω-μm is included in all cases. (c)-(d) Relative comparison with Si reference at each V_{DD}.

degrades as N_{tip} increases. One thing to note here is that *SS* increases more rapidly in Ge pMOS than in Ge nMOS (Fig. 3(d)) as N_{tip} increases. This is because the hole effective mass is lighter than the electron effective mass in Ge [5], so there is more source-drain (S-D) tunneling for Ge pMOS than in Ge nMOS [25]. Therefore, while it is still an option to increase N_{tip} for Ge pMOS to boost the ON-current [25], the design space may be relatively limited compared to Ge nMOS because of the larger leakage current.

Fig. 10 shows I_D vs. V_D at different V_G's for Si and Ge pMOS. For each device, we show $I-V$ results including the carrier scattering effect (*BR* correction, solid lines) along with ballistic $I-V$'s (dashed lines). We show intrinsic results ($R_{SD} = 0$) and final $I-V$'s including $R_{SD} = 200$ Ω-μm. For Si pMOS, I_D decreases significantly after the *BR* correction. For example, in the result including R_{SD} (Fig. 10(b)), I_D at $V_G = -0.7$ V, $V_D = -0.1$ V (I_{Dlin}) and $V_G = V_D = -0.7$ V (I_{Dsat}) are reduced by 33 % (*BR*~0.67) and 29 % (*BR*~0.71), respectively. For Ge pMOS, results depend on N_{tip}. For a low N_{tip}, I_{Dlin} and I_{Dsat} decrease by 35 % (*BR*~0.65) (Fig. 10(d)). For a high N_{tip}, I_{Dlin} and I_{Dsat} are reduced less, by 31 % (*BR*~0.69) in Fig. 10(f). (See the Appendix for more discussions on the material, N_{tip}, and bias dependence of *BR*.)

B. PERFORMANCE METRICS: $I_{EFF,P}$ AND $C_{EFF,P}$

Fig. 11 shows $I_{eff,p}$ vs. V_{DD} for the ballistic case and for the final result with *BR* correction. $R_{SD} = 200$ Ω-μm is included in all cases. Along with the absolute values of $I_{eff,p}$, we also report the relative comparison result against the Si reference at each V_{DD} (0 % baseline in Fig. 11(c)-(d)). For Ge pMOS, depending on the operating condition, a different N_{tip} may be chosen to deliver the best performance [25]. As shown in Fig. 11(b),(d), Ge pMOS with a low N_{tip} gives the best $I_{eff,p}$ at low V_{DD} (up to ~0.6 V). As V_{DD} increases, Ge pMOS with a medium N_{tip} becomes best (up to ~0.9 V). As V_{DD} increases further (>0.9 V), Ge pMOS with a large N_{tip} gives the largest $I_{eff,p}$ while the improvement over Si is limited (due to the degraded *SS* discussed in Fig. 9).

As also discussed in Section III-B, we should note that in Fig. 11, the gate WF is adjusted to meet the $I_{OFF,target}$ at a certain V_{DD}, and the same gate WF is used for all other V_{DD} operations. Therefore, the $I_{OFF,actual}$ at different V_{DD}'s may be different than the $I_{OFF,target}$. In Fig. 12, we show $I_{OFF,actual}$ (I_D at $V_G = 0$ V and $V_D = -V_{DD}$) for the cases in Fig. 11. At $V_{DD} = 0.7$ V, all devices meet $I_{OFF,target}$ as intended. For $V_{DD} < 0.7$ V, $I_{OFF,actual} < I_{OFF,target}$. For $V_{DD} > 0.7$ V, $I_{OFF,actual} > I_{OFF,target}$ for all devices while the behaviors are quite different depending on the material. For Si pMOS, the $I_{OFF,actual}$ increases gradually as V_{DD} increases due to the classical SCE. To avoid high leakage problems, we set the upper limit of $I_{OFF,actual}$ ($I_{OFF,max}$) as $I_{OFF,max} = 3 \times I_{OFF,target}$ like in the nMOS case. This will also set the maximum allowed V_{DD} ($V_{DD,max}$). As shown

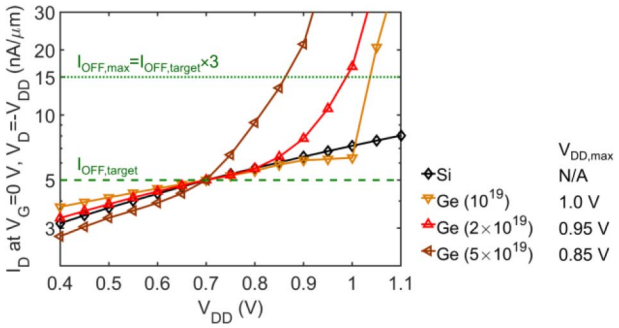


FIGURE 12. Simulation results for $I_{OFF,actual}$ (I_D at $V_G = 0$ V and $V_D = -V_{DD}$) vs. V_{DD} for the pMOS cases in Fig. 11. The $I_{OFF,target}$ (5 nA/μm) and the upper limit of allowed I_{OFF} ($I_{OFF,max} = 3 \times I_{OFF,target}$) are also shown for reference. $V_{DD,max}$ to satisfy the $I_{OFF,max}$ condition is also shown for each pMOS (where N/A means that $I_{OFF,actual}$ does not exceed $I_{OFF,max}$ in all V_{DD} range of interest).

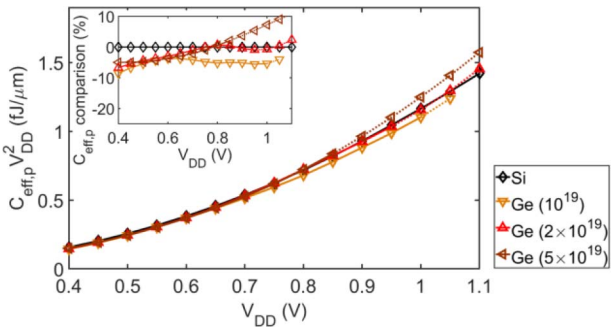


FIGURE 13. Simulation results for $C_{eff,p}V_{DD}^2$ vs. V_{DD} ($I_{OFF} = 5$ nA/μm at $V_{DD} = 0.7$ V) of Si ($N_{tip} = 10^{20}$ cm^{-3}) and Ge pMOS ($N_{tip} = 10^{19}$, 2×10^{19}, 5×10^{19} cm^{-3}). $C_{par} = 0.6$ fF/μm is considered in all cases. (inset) Relative comparison with Si reference at each V_{DD}.

in Fig. 12, Si pMOS does not hit this upper limit in the V_{DD} range of interest. For Ge pMOS, the behavior depends on N_{tip}. As N_{tip} increases, $I_{OFF,actual}$ goes above the upper limit at a lower V_{DD} ($V_{DD,max} \sim 1.0, 0.95$ and 0.85 V for $N_{tip} = 10^{19}$, 2×10^{19}, and 5×10^{19} cm^{-3}, respectively). Note that in Fig. 11 and all subsequent figures for pMOS (Fig. 13, Fig. 21), V_{DD} data points beyond $V_{DD,max}$ are plotted using dotted lines.

In Fig. 13, we show $C_{eff,p}V_{DD}{}^2$ vs. V_{DD} and the relative comparison with Si reference at each V_{DD}. For Ge pMOS, $C_{eff,p}$ is lower than the Si reference for a low N_{tip} while it becomes comparable to Si for higher N_{tip}'s.

V. CMOS BENCHMARKING

In this section, we present benchmarking results for CMOS considering both n- and pMOS using the approach discussed in Section II-C. Along with homogeneous CMOS where n- and pMOS have the same channel material (Si CMOS, Ge CMOS), we also consider various types of hybrid CMOS with different n- and pMOS materials (III-V hybrid CMOS, Ge hybrid CMOS) as summarized in Table 2. (Note that the hybrid CMOS approach is also being actively explored experimentally [51]–[53].) The values in the parentheses are the N_{tip} in cm^{-3}. We also show the $V_{DD,max}$ of each CMOS, which is the minimum of the $V_{DD,max}$ values of n- and pMOS (from Fig. 6 and Fig. 12). In all following figures for CMOS (Figs. 14-17), V_{DD} data points beyond $V_{DD,max}$ are plotted using dotted lines. In Table 2, n- and pMOS material names in bold indicate the cases we focus on for the CMOS energy vs. delay analysis in Section V-B.

A. PERFORMANCE METRICS: $I_{EFF,N+P}$ AND $C_{EFF,N+P}$

In Fig. 14, we show simulation results for $I_{eff,n+p}$ vs. V_{DD} and the relative comparison with the Si CMOS reference. We consider $R_{SD} = 200$ Ω-μm for each n- and pMOS, and effects of carrier scattering are all included. At up to $V_{DD}\sim0.55$ V, Ge CMOS with a low N_{tip} shows the best $I_{eff,n+p}$ while III-V-Ge hybrid CMOS also delivers good performance. At $V_{DD} \sim 0.6 - 0.85$ V, Ge CMOS with a medium N_{tip} is the best while GaAs-Ge hybrid CMOS also gives good performance. At $V_{DD} > 0.9$ V, Ge CMOS with a high N_{tip} gives the largest $I_{eff,n+p}$ while it may have a leakage problem. GaAs-Si hybrid CMOS may be an option here because it also gives significant $I_{eff,n+p}$ improvement over Si CMOS while it does not have the leakage problem.

In Fig. 15, we show $C_{eff,n+p}V_{DD}{}^2$ vs. V_{DD} for homogeneous and hybrid CMOS and the relative comparison with the Si CMOS reference at each V_{DD}. $In_{0.53}Ga_{0.47}As$-Ge CMOS shows the lowest capacitance due to the low N_{tip} and small DOS. For Ge CMOS, $C_{eff,n+p}$ is lower than the Si CMOS reference for a low N_{tip} while it becomes comparable to Si for higher N_{tip}'s.

TABLE 2. Homogeneous and hybrid n- and pMOS combinations for CMOS benchmarking. $V_{DD,max}$ to satisfy the $I_{OFF,max}$ condition is also shown for each case (N/A: condition met in all V_{DD} range of interest).

	nMOS	pMOS	$V_{DD,max}$
Si CMOS	**Si** (10^{20})	**Si** (10^{20})	N/A
III-V hybrid CMOS	**$In_{0.53}Ga_{0.47}As$** (10^{19})	**Si** (10^{20})	0.9 V
	$In_{0.53}Ga_{0.47}As$ (10^{19})	Ge (10^{19})	0.9 V
	$In_{0.53}Ga_{0.47}As$ (10^{19})	**Ge** (2×10^{19})	0.9 V
	GaAs (2×10^{19})	**Si** (10^{20})	N/A
	GaAs (2×10^{19})	Ge (10^{19})	1.0 V
	GaAs (2×10^{19})	**Ge** (2×10^{19})	0.95 V
Ge hybrid CMOS	Si (10^{20})	Ge (10^{19})	1.0 V
	Si (10^{20})	**Ge** (2×10^{19})	0.95 V
	Ge (10^{19})	Si (10^{20})	0.95 V
	Ge (2×10^{19})	**Si** (10^{20})	0.85 V
Ge CMOS	**Ge** (10^{19})	**Ge** (10^{19})	0.95 V
	Ge (2×10^{19})	**Ge** (2×10^{19})	0.85 V
	Ge (5×10^{19})	**Ge** (5×10^{19})	0.75 V

B. PERFORMANCE METRICS: ENERGY VS. DELAY

In Figs. 16-17, we show simulation results for the energy (CV^2) vs. delay (CV/I) and relative comparison with the Si CMOS reference. For each n- and pMOS, parasitic components ($R_{SD} = 200$ Ω-μm and $C_{par} = 0.6$ fF/μm) and scattering effects are included. These are the key result of this paper. As discussed in Section II-C, CV^2 and CV/I are calculated for two scenarios, gate capacitance loading ($C_{load} = C_{eff,n+p}$, Fig. 16) and interconnect wire capacitance loading ($C_{load} = C_{wire}$, Fig. 17). In Figs. 16-17, symbols

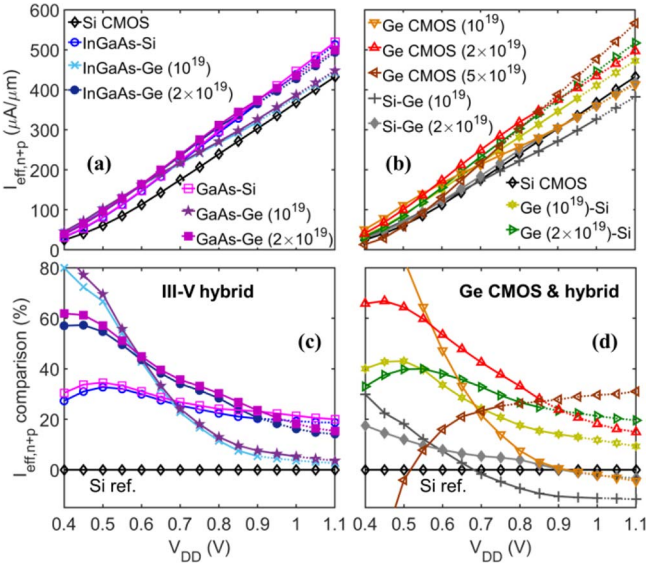


FIGURE 14. Simulation results for $I_{eff,n+p}$ vs. V_{DD} (I_{OFF} = 5 nA/μm at V_{DD} = 0.7 V) of homogeneous and hybrid CMOS in Table 2. (a) Si CMOS and III-V hybrid CMOS. (b) Ge hybrid CMOS and Ge CMOS. (For hybrid CMOS, the material names are shown as nMOS-pMOS. InGaAs means $In_{0.53}Ga_{0.47}As$.) R_{SD} = 200 Ω-μm is included for each n- and pMOS. All results are after the *BR* correction. (c)-(d) Relative comparison with Si CMOS at each V_{DD}.

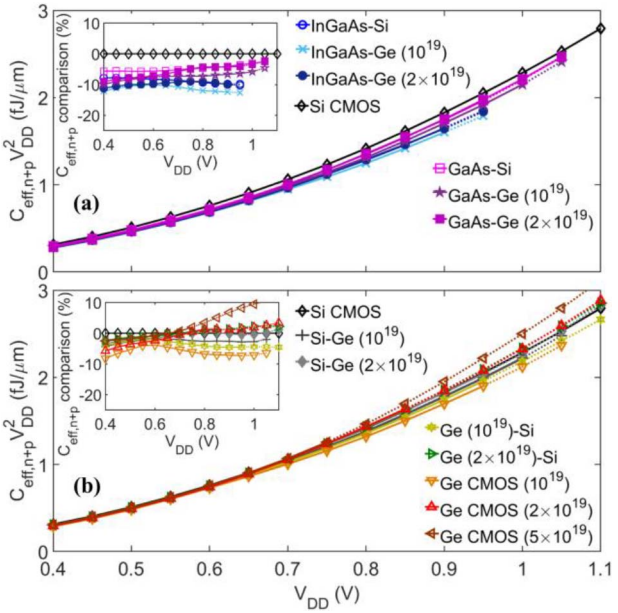


FIGURE 15. Simulation results for $C_{eff,n+p}V_{DD}^2$ vs. V_{DD} (I_{OFF} = 5 nA/μm at V_{DD} = 0.7 V) of homogeneous and hybrid CMOS in Table 2. (a) Si CMOS and III-V hybrid CMOS. (b) Ge hybrid CMOS and Ge CMOS. (For hybrid CMOS, the material names are shown as nMOS-pMOS. InGaAs means $In_{0.53}Ga_{0.47}As$.) C_{par} = 0.6 fF/μm is considered for each n- and pMOS. (insets) Relative comparison with Si CMOS at each V_{DD}.

(along with numbers next to them) indicate the V_{DD}-sweep data points with 50 mV spacing. Relative comparisons with the Si CMOS reference are done along two directions, i) energy comparison for the same delay (guiding arrows from top to bottom), and ii) delay comparison for the same energy (guiding arrows from right to left).

In Fig. 16 ("gate capacitance loading"), when we compare CV^2 for the same CV/I (Fig. 16(b)), Ge CMOS with a low N_{tip} gives the largest energy reduction for large delay (low frequency) operation. This is because Ge CMOS with a low N_{tip} gives the best $I_{eff,n+p}$ (Fig. 14(b),(d)) along with significant reduction of $C_{eff,n+p}$ at low V_{DD}'s (Fig. 15(b)). For example, when compared with Si CMOS at V_{DD} = 0.7 V (guiding arrows from top to bottom), Ge CMOS with a low N_{tip} delivers the same delay at $V_{DD} \sim$ 0.5 V, resulting in a significant energy reduction (by ~55 %). As the delay decreases, a cross-over occurs so that $In_{0.53}Ga_{0.47}As$-Ge CMOS delivers the best performance. This is because the drive current is still good (Fig. 14(a),(c)) while $C_{eff,n+p}$ reduction is the best (Fig. 15(a)). The trends are similar when we compare the delay for the same energy (Fig. 16(c)). For low energy operation, Ge CMOS with a low N_{tip} gives the largest delay reduction. As the energy increases, $In_{0.53}Ga_{0.47}As$-Ge hybrid CMOS gives the smallest delay.

For a constant C_{wire}, we assume that it is 4 times of $C_{eff,n+p}$ of Si CMOS (like fan-out of 4) [25]. While the absolute values of CV^2 vs. CV/I (Fig. 17(a)) may change depending on the value of C_{wire}, the relative comparison results in Fig. 17(b)-(c) do not change because C_{wire} is constant and applies the same to all cases. The energy vs. delay results in Fig. 17 are basically determined by $I_{eff,n+p}$ of each CMOS combination (Fig. 14). When we compare CV^2 for the same CV/I (Fig. 17(b)), Ge CMOS with a low N_{tip} gives the largest energy reduction due to the best $I_{eff,n+p}$ in the low V_{DD} region (Fig. 14(b),(d)). For example, when compared with Si CMOS at V_{DD} = 0.7 V (guiding arrows from top to bottom), Ge CMOS with a low N_{tip} gives the same delay at V_{DD}~0.55 V, giving a significant energy reduction (by ~40 %). As the delay decreases, a cross-over occurs so that Ge CMOS with a medium N_{tip} gives the best performance, as also indicated by the largest $I_{eff,n+p}$ in Fig. 14(b),(d) at $V_{DD} \sim 0.6-0.85$ V. The trends are similar when we compare the delay for the same energy (Fig. 17(c)). For low energy operation, Ge CMOS with a low N_{tip} gives the largest delay reduction. As the energy increases, Ge CMOS with a medium N_{tip} gives the best performance. As the energy increases further, Ge CMOS with a large N_{tip} delivers the shortest delay.

VI. DISCUSSION: EFFECTS OF CONTACT RESISTIVITY

In the benchmarking results so far, we assumed that the R_{SD} is matched across different n- and pMOS materials. In reality, however, R_{SD} can be material dependent. For example, the metal-semiconductor (M-S) contact resistivity (ρ_c) may depend on the semiconductor material. For non-Si materials, there may be experimental challenges to deliver good ρ_c's. In Figs. 18-20, we provide comprehensive literature search results (exhaustive list of relevant papers published for the past decade or so) for experimental ρ_c's of n-$In_{0.53}Ga_{0.47}As$ [54]–[79], n-Ge [80]–[122], and

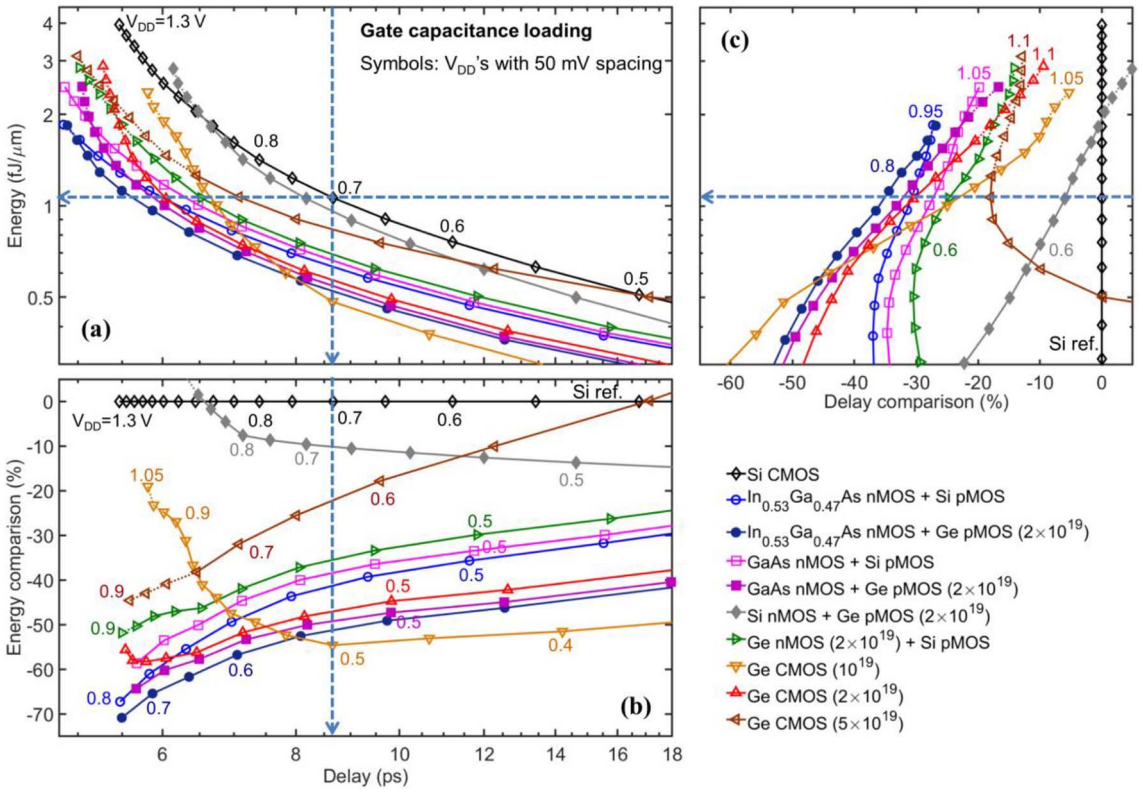


FIGURE 16. Simulation results for (a) CV^2 vs. CV/I with gate capacitance loading. Relative comparisons of (b) energy for the same delay (guiding arrows from top to bottom) and (c) delay for the same energy (guiding arrows from right to left) against Si CMOS. The gate WF of each n- and pMOS is adjusted to meet I_{OFF} = 5 nA/μm at V_{DD} = 0.7 V. Symbols (along with numbers next to them) indicate the V_{DD}-sweep data points with 50 mV spacing. R_{SD} = 200 Ω-μm, C_{par} = 0.6 fF/μm, and scattering effects (*BR* corrections) are all considered for each n- and pMOS.

p-Ge [100], [103], [116], [117], [123]–[138]. (For guidance, lines are drawn at $\rho_c = 10^{-8}$ Ω-cm^2, to represent a typical number for a decent contact.) Data points are categorized using different symbols to represent different approaches to realize good ρ_c's. For n-$In_{0.53}Ga_{0.47}As$ (Fig. 18), ρ_c has been around $\sim10^{-8}$ Ω-cm^2 with the best value of 5×10^{-9} Ω-cm^2 [55]. For n-Ge (Fig. 19), achieving a low ρ_c has been specifically challenging due to the high Schottky barrier height, limited solubility of dopants, and Fermi level pinning. The ρ_c of n-Ge has been continuously improved for the past decade, and the best value is 1.6×10^{-9} Ω-cm^2 [122] while there are multiple papers that report $\sim 10^{-8}$ Ω-cm^2. For p-Ge (Fig. 20), low ρ_c's have been reported with the best value of 5×10^{-10} Ω-cm^2 [135].

To explore the effect of material-dependent R_{SD}, we perform a sensitivity analysis of I_{eff} vs. V_{DD}. For this, we define a new performance metric, $R_{SD,Ieffmatched}$, which means the R_{SD} required for a device (either n- or pMOS) to have the same I_{eff} as Si with a reference R_{SD} ($R_{SD,ref}$). Higher $R_{SD,Ieffmatched}$ ($R_{SD,Ieffmatched} > R_{SD,ref}$) means that the device can tolerate a larger R_{SD} (i.e., has a relaxed R_{SD} requirement) to deliver the I_{eff} matched to that of Si. Therefore, the higher $R_{SD,Ieffmatched}$, the better.

In Fig. 21(a), we show simulation results for $R_{SD,Ieffmatched}$ vs. V_{DD} for $In_{0.53}Ga_{0.47}As$ nMOS, Ge nMOS, and Ge pMOS with the Si reference (n- or pMOS) with $R_{SD,ref}$ = 200 Ω-μm. In general, $In_{0.53}Ga_{0.47}As$ and Ge channel materials give higher $R_{SD,Ieffmatched}$ (more relaxed R_{SD} requirement) at low V_{DD} while $R_{SD,Ieffmatched}$ decreases as V_{DD} increases. As examples, the actual values of $R_{SD,Ieffmatched}$ are shown at V_{DD}=0.7 V in Fig. 21(a). At this V_{DD}, $R_{SD,Ieffmatched} > R_{SD,ref}$ for all cases (~460, 530, 270 Ω-μm for $In_{0.53}Ga_{0.47}As$ nMOS, Ge nMOS, and Ge pMOS, respectively), meaning that R_{SD} requirements are all relaxed for those materials. Ge nMOS has the largest $R_{SD,Ieffmatched}$, which also means that it can deliver the largest $I_{eff,n}$ if R_{SD} is matched to $R_{SD,ref}$. We also note that for $In_{0.53}Ga_{0.47}As$ nMOS and Ge nMOS, R_{SD} requirements remain relaxed ($R_{SD,Ieffmatched} > R_{SD,ref}$) at up to V_{DD}=1.1 V while for Ge pMOS, R_{SD} requirement becomes tighter ($R_{SD,Ieffmatched} < R_{SD,ref}$) at $V_{DD} \geq 0.9$ V.

For a given R_{SD}, we may also extract the corresponding ρ_c using the information on the S/D contact dimension. In this discussion, we assume $R_{SD} = R_c + R_{other}$, where R_c is the M-S contact resistance, and R_{other} includes all other R_{SD} components such as the spreading and tip resistances. For simplicity, we assume R_{other} = 150 Ω-μm (while we note that it can depend on the material and geometric structures of S/D contacts [47], [48]). And then, we use $R_c = \rho_c/L_{conact} \times 2$, where $L_{contact}$ is the contact length, and the factor 2 arises because R_c includes effects of both source and drain. In this discussion, we assume $L_{contact}$ = 8 nm

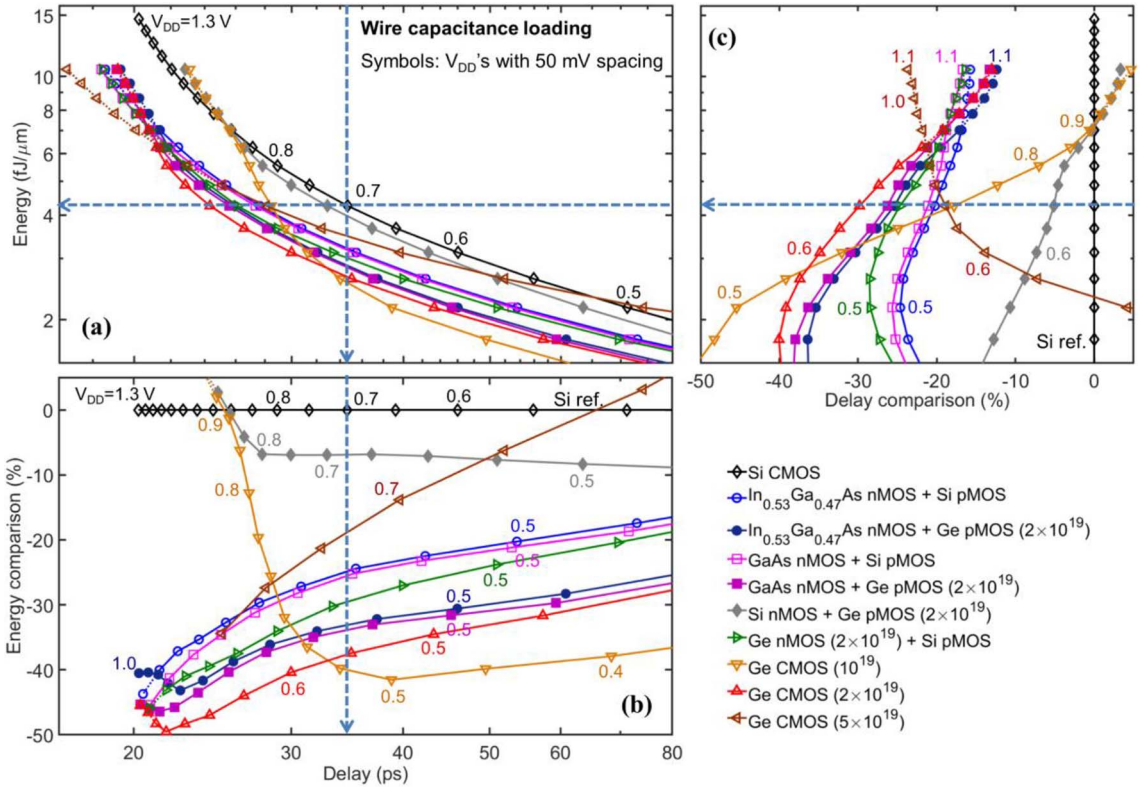


FIGURE 17. Simulation results for (a) CV^2 vs. CV/I with wire capacitance loading. Relative comparison of (b) energy for the same delay (guiding arrows from top to bottom) and (c) delay for the same energy (guiding arrows from right to left) against Si CMOS. The gate WF of each n- and pMOS is adjusted to meet I_{OFF} = 5 nA/μm at V_{DD} = 0.7 V. Symbols (along with numbers next to them) indicate the V_{DD}-sweep data points with 50 mV spacing. R_{SD} = 200 Ω-μm, C_{par} = 0.6 fF/μm, and scattering effects (*BR* corrections) are all considered for each n- and pMOS.

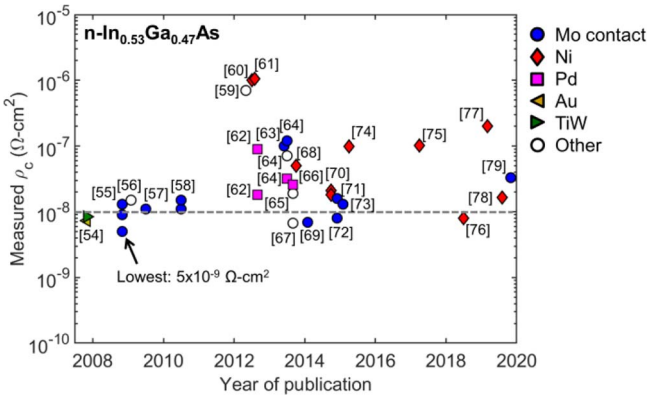


FIGURE 18. Comprehensive literature search result for experimental ρ_c's of n-$In_{0.53}Ga_{0.47}As$ vs. year of publication [54]–[79]. Different symbols represent various approaches (metal contact materials) to realize good ρ_c's.

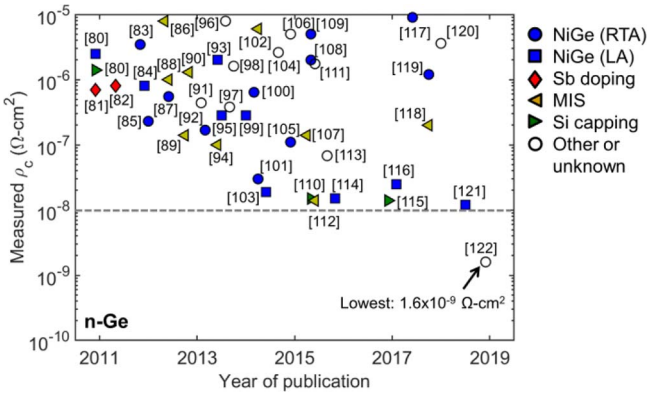


FIGURE 19. Comprehensive literature search result for experimental ρ_c's of n-Ge vs. year of publication [80]–[122]. Different symbols represent various approaches to realize good ρ_c's (NiGe using rapid thermal anneal (RTA) or laser anneal (LA), metal-insulator-semiconductor (MIS), etc.).

(similar to the ITRS node of year 2019 [1]), and then $\rho_c = 2 \times 10^{-9}$ Ω-cm^2 for $R_{SD,ref} = 200$ Ω-μm. Now we can readily define another metric, $\rho_{c,Ieffmatched}$, which means the ρ_c value required to match the I_{eff} of Si with a reference ρ_c ($\rho_{c,ref}$). In Fig. 21(b), we show results for $\rho_{c,Ieffmatched}$ vs. V_{DD} for $In_{0.53}Ga_{0.47}As$ nMOS, Ge nMOS, and Ge pMOS. As examples, we also show the actual values of $\rho_{c,Ieffmatched}$ at $V_{DD} = 0.7$ V. Note that those values ($\rho_{c,Ieffmatched} \sim 1.2\times10^{-8}$, 1.5×10^{-8}, and 4.8×10^{-9} Ω-cm^2 for $In_{0.53}Ga_{0.47}As$ nMOS, Ge nMOS, and Ge pMOS, respectively) are within the range of experimentally reported ρ_c's in Figs. 18-20.

In the Appendix, as a supplementary approach to discuss the effect of material-dependent ρ_c, we provide another CV^2 vs. CV/I plot using R_{SD} estimated from

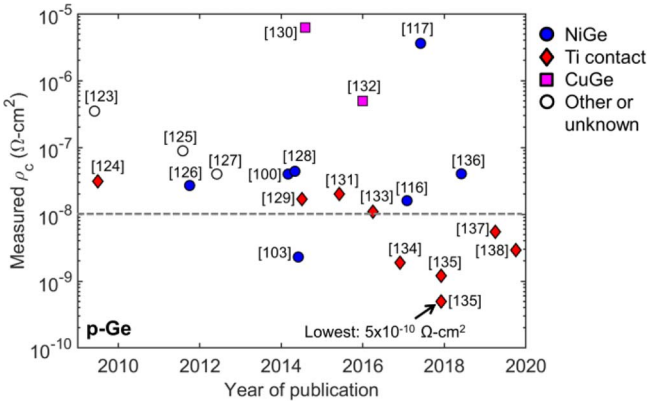


FIGURE 20. Comprehensive literature search result for experimental ρ_c's of p-Ge vs. year of publication [100], [103], [116], [117], [123]–[138]. Different symbols represent various approaches (metal contacts) to realize good ρ_c's.

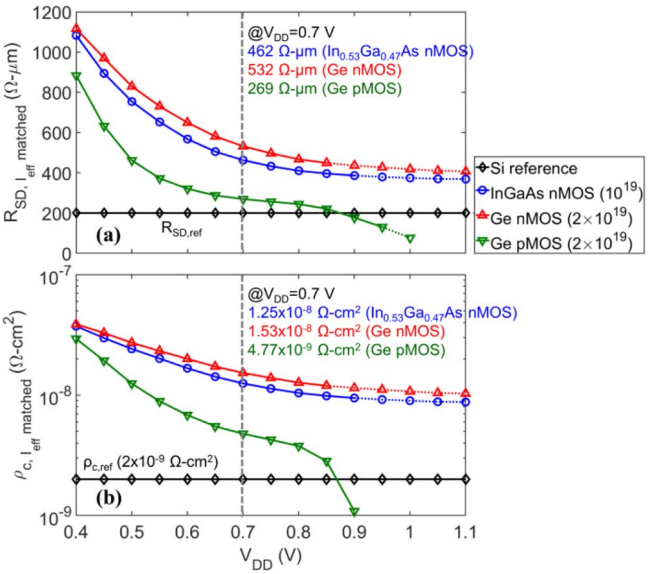


FIGURE 21. Simulation results for (a) $R_{SD,Leffmatched}$ vs. V_{DD} and (b) $\rho_{c,Leffmatched}$ vs. V_{DD} (I_{OFF} = 5 nA/μm at V_{DD} = 0.7 V) for $In_{0.53}Ga_{0.47}As$ nMOS (10^{19}), Ge nMOS (2×10^{19}), and Ge pMOS (2×10^{19}) with Si n- or pMOS reference (10^{20}) with $R_{SD,ref}$ = 200 Ω-μm and $\rho_{c,ref} = 2 \times 10^{-9}$ Ω-cm^2. The value in () is N_{tip} in cm^{-3}. The higher $R_{SD,Leffmatched}$ ($\rho_{c,Leffmatched}$), the better because it means the R_{SD} (ρ_c) requirement can be relaxed to deliver I_{eff} matched to that of Si. Actual values of $R_{SD,Leffmatched}$ and $\rho_{c,Leffmatched}$ at V_{DD} = 0.7 V are also shown on the graph.

the best experimental ρ_c reported in literatures for each material [55], [122], [134], [135] (also see Figs. 18-20). This is basically a revision of Fig. 16 where R_{SD} is assumed to be matched among all materials. See the Appendix for more discussions.

VII. CONCLUSION

In this paper, we performed comprehensive channel material benchmarking for n- and pMOS considering effects of quantum transport and carrier scattering. We covered various channel material options, Si, InAs, $In_{0.7}Ga_{0.3}As$, $In_{0.53}Ga_{0.47}As$, GaAs, and Ge for nMOS, and Si and Ge for

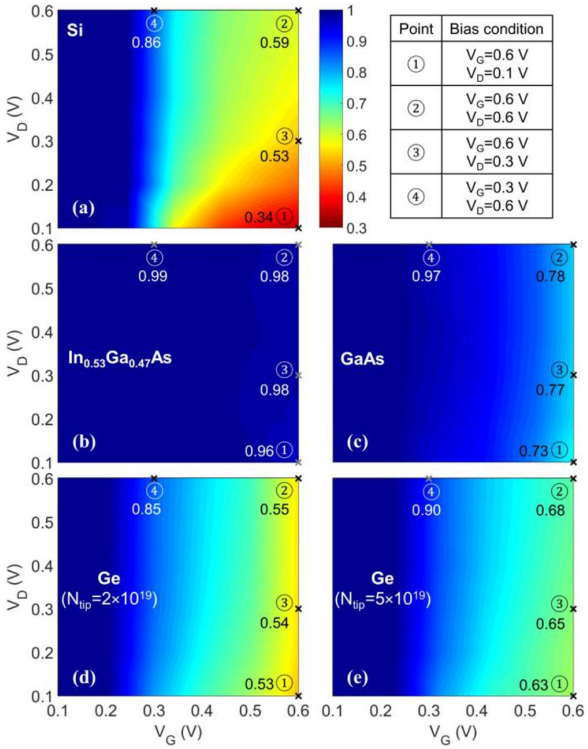


FIGURE 22. 2D color plots of MC simulation results for $BR(V_G, V_D)$ of (a) Si nMOS ($N_{tip} = 10^{20}$ cm^{-3}), (b) $In_{0.53}Ga_{0.47}As$ nMOS ($N_{tip} = 10^{19}$ cm^{-3}), (c) GaAs nMOS ($N_{tip} = 2 \times 10^{19}$ cm^{-3}), and (d)-(e) Ge nMOS ($N_{tip} = 2 \times 10^{19}$, 5×10^{19} cm^{-3}) with no R_{SD} (intrinsic V_G and V_D). The reference V_G is set to satisfy I_{OFF} = 100 nA/μm at V_G = 0 V and V_D = 0.6 V. On the 2D color plot, BR values are also shown at 4 relevant bias conditions (table in the upper right).

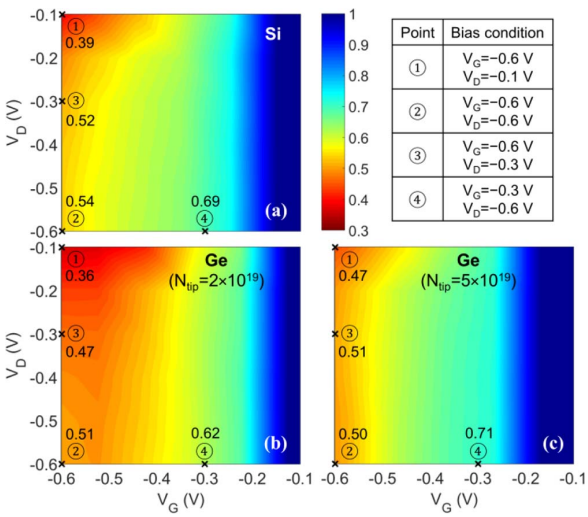
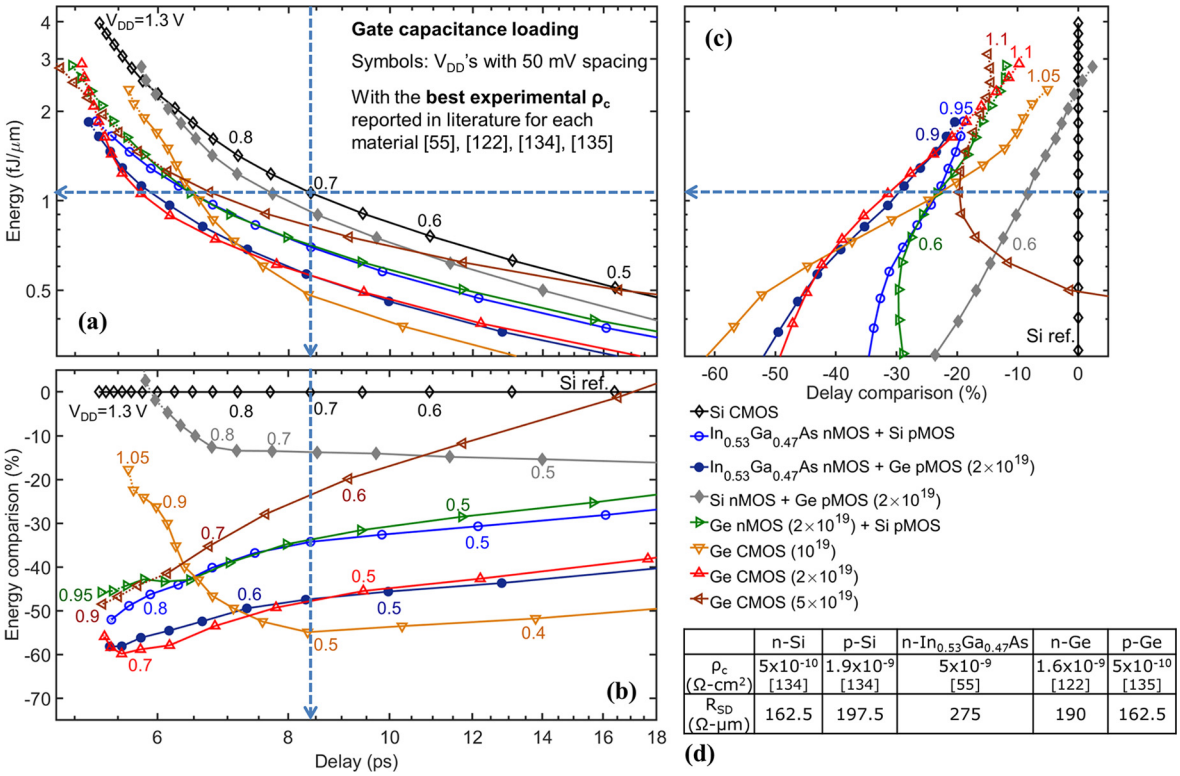


FIGURE 23. 2D color plots of MC simulation results for $BR(V_G, V_D)$ of (a) Si pMOS ($N_{tip} = 10^{20}$ cm^{-3}) and (b)-(c) Ge pMOS ($N_{tip} = 2 \times 10^{19}$, 5×10^{19} cm^{-3}) with no R_{SD} (intrinsic V_G and V_D). The reference V_G is set to satisfy I_{OFF} = 100 nA/μm at V_G = 0 V and V_D = −0.6 V. On the 2D color plot, BR values are also shown at 4 relevant bias conditions (table in the upper right).

pMOS, using hybrid simulation of quantum transport and semi-classical Monte Carlo. Comprehensive $I-V$ characteristics and performance metrics such as the capacitance and



(d)

	n-Si	p-Si	n-$In_{0.53}Ga_{0.47}As$	n-Ge	p-Ge
ρ_c (Ω-cm^2)	5×10^{-10} [134]	1.9×10^{-9} [134]	5×10^{-9} [55]	1.6×10^{-9} [122]	5×10^{-10} [135]
R_{SD} (Ω-μm)	162.5	197.5	275	190	162.5

FIGURE 24. Simulation results for (a) CV^2 vs. CV/I with gate capacitance loading using R_{SD} estimated from the best experimental ρ_c reported in literatures for each material [55], [122], [134], [135] (also see Figs. 18-20). Relative comparisons of (b) energy for the same delay (guiding arrows from top to bottom) and (c) delay for the same energy (guiding arrows from right to left) against Si CMOS. (d) The best ρ_c values and corresponding R_{SD}'s (estimated for $L_{contact}$ = 8 nm, see Section VI). The gate WF of each n- and pMOS is adjusted to meet I_{OFF} = 5 nA/μm at V_{DD} = 0.7 V. Symbols (along with numbers next to them) indicate the V_{DD}-sweep data points with 50 mV spacing. C_{par} = 0.6 fF/μm and scattering effects (*BR* corrections) are all considered for each n- and pMOS.

effective drive current (I_{eff}) are explored considering device parasitic components. For nMOS, InAs and $In_{0.7}Ga_{0.3}As$ may not be a good option due to the high leakage problem. For LP operation, $In_{0.53}Ga_{0.47}As$ and GaAs nMOS may deliver good performance while Ge nMOS with different S/D tip designs (e.g., tip doping density) may give performance advantage over Si from LP to HP operations. For pMOS, Ge with different S/D tip designs may still deliver good performance while the improvement over Si could be limited due to the higher leakage. We also explored various kinds of homogeneous and hybrid combinations of n- and pMOS (Si CMOS, III-V hybrid CMOS, Ge hybrid CMOS, and Ge CMOS) and presented benchmarking results for I_{eff}, capacitance, and switching energy vs. delay for two capacitance loading scenarios (gate capacitance vs. wire capacitance). Finally, we performed sensitivity analysis of I_{eff} on the parasitic resistance (R_{SD}) and contact resistivity (ρ_c). Novel channel materials such as $In_{0.53}Ga_{0.47}As$ and Ge may relax the R_{SD} and ρ_c requirements to match the I_{eff} performance of Si reference. We also performed exhaustive literature search of experimental ρ_c's for novel materials to discuss the effect of material-dependent R_{SD}. We expect that the comprehensive CMOS benchmarking results and literature review reported in this paper will help guide the material selection for future CMOS technology nodes.

APPENDIX

Fig. 22 shows two-dimensional (2D) color plots of MC (in-house quantum-corrected MC) simulation results for *BR* as a function of intrinsic V_G and V_D for nMOS. (One thing to note here is that while we consider the bias-dependence as $BR(V_G, V_D)$ in this study, most *BR* results in literatures [43], [139]–[141] are reported as a single number at a fixed bias condition such as the saturation.) As examples, we show results for Si nMOS, $In_{0.53}Ga_{0.47}As$ nMOS, GaAs nMOS, and Ge nMOS. On the 2D color plots, we also show the values of *BR* at 4 bias condition points that are often relevant, i) $V_G = V_{DD}$, $V_D = 0.1$ V (like I_{Dlin}), ii) $V_G = V_D = V_{DD}$ (like I_{Dsat}), iii) $V_G = V_{DD}$, $V_D = V_{DD}/2$ (like I_H), and iv) $V_G = V_{DD}/2$, $V_D = V_{DD}$ (like I_L).

For all cases in Fig. 22, *BR* decreases as V_G increases. The *BR* tends to increase as V_D increases while the dependence is relatively weak. For heavy-m^*/large DOS materials such as Si, *BR* significantly decreases as V_G increases. For light-m^*/small DOS material such as $In_{0.53}Ga_{0.47}As$, *BR* remains high (close to 1) even at high V_G, indicating that it operates close to the ballistic limit. For GaAs and Ge, m^* of the lowest conduction band is small so that the *BR* is high at low to medium V_G. As V_G increases further, however, heavy-m^* upper valleys start to be occupied resulting in increased carrier scattering and a rapid decrease of *BR*.

In Fig. 22(d)-(e), we also notice the N_{tip}-dependence for Ge nMOS. For a lower N_{tip}, *BR* decreases more rapidly as V_G increases. (Note that the *BR* in this study inherently includes the effect of S/D tip because we turn on and turn off scattering for the whole device in Fig. 1.) Analysis of potential profile and charge distribution (not shown) suggests that with a lower N_{tip}, the source exhaustion becomes severer (i.e., source exhaustion starts at a lower V_G) when scattering is included. This means that the tip resistance may become more of an issue when carrier scattering comes into the picture.

In Fig. 22, there are a couple of other points worth noting. First, the *BR* results in Fig. 22 are fairly consistent with those available in literatures, such as the experimental Si nMOS with a similar L_G (*BR*~0.6 in saturation) [141] and theoretical $In_{0.53}Ga_{0.47}As$ nMOS (*BR*>0.97 in saturation) [43]. Second, we check that Si nMOS results from Sentaurus Device Monte Carlo (test simulation, not shown) are similar to those from the in-house MC tool in Fig. 22(a). For III-V and Ge nMOS, however, results may not agree well because the significant effect of quantum correction (e.g., valley-dependent quantum confinement [44]) is well treated by the in-house MC tool while it is not fully captured by Sentaurus Device Monte Carlo.

In Fig. 23, we show 2D color plots of MC (Sentaurus Device Monte Carlo [45]) simulation results for *BR* as a function of intrinsic V_G and V_D for Si and Ge pMOS. On the 2D color plots, we also show the values of *BR* at 4 bias condition points that are often relevant. Like in the nMOS case, *BR* tends to decrease as V_G increases or V_D decreases while the V_D-dependence is relatively weak. For Ge pMOS with different N_{tip}'s (Fig. 23(b)-(c)), we also see that *BR* decreases more rapidly at high V_G for a lower N_{tip}.

Fig. 24(a)-(c) shows simulation results for CV^2 vs. *CV/I* and relative comparison with Si CMOS using R_{SD} estimated from the best experimental ρ_c reported in literatures for each material, n- and p-Si [134], n-$In_{0.53}Ga_{0.47}As$ [55] (see Fig. 18), n-Ge [122] (Fig. 19), and p-Ge [135] (Fig. 20). The best ρ_c values and corresponding R_{SD}'s (estimated for $L_{contact}$=8 nm, see Section VI for details) are summarized in Fig. 24(d). For simplicity, only the "gate capacitance loading" scenario is shown, so Fig. 24 is basically a revision of Fig. 16 where R_{SD} is assumed to be the same for all materials. Due to the high ρ_c of n-$In_{0.53}Ga_{0.47}As$, the relative benefit of $In_{0.53}Ga_{0.47}As$-based hybrid CMOS may be reduced. We also note that while ρ_c and R_{SD} of Ge nMOS may lag behind those of Si nMOS, the relative benefit may be restored for Ge CMOS due to the good ρ_c of Ge pMOS. While Fig. 24 may be useful for practical purposes as of today, we note as a final remark that it is far from conclusive because reducing ρ_c is an actively on-going effort for any MOS channel materials.

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