Received 7 April 2020; accepted 27 April 2020. Date of publication 29 April 2020; date of current version 20 May 2020.
The review of this article was arranged by Editor C. C. McAndrew.

Digital Object Identifier 10.1109/JEDS.2020.2991355

2.3 kV 4H-SiC Accumulation-Channel Split-Gate Planar Power MOSFETs With Reduced Gate Charge

ADITI AGARWAL, KIJEONG HAN, AND B. JAYANT BALIGA (Life Fellow, IEEE)

Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27695, USA

CORRESPONDING AUTHOR: A. AGARWAL (e-mail: aagarw12@ncsu.edu)

ABSTRACT 2.3 kV 4H-SiC split-gate (SG) planar accumulation-channel power MOSFETs have been successfully manufactured in a 6 inch commercial foundry with good parametric distributions. The measured electrical characteristics of these devices are compared with conventional ACCUFETs manufactured with the same cell-pitch and process to quantify the improved performance. The gate charge and high-frequency figures-of-merit (HF-FOM) of the 2.3 kV SG-MOSFETs were experimentally verified to be a factor of 1.8x better than that of the conventional MOSFETs with no difference in specific on-resistance.

INDEX TERMS 4H-SiC, 2.3 kV devices, accumulation channel, C_{gd}, planar-gate MOSFET, Q_{gd}, $R_{on,sp}$, silicon carbide, split-gate.

I. INTRODUCTION

Silicon Carbide power MOSFETs allow reduction of switching loss compared with silicon IGBTs in applications. Most publications have reported 1.2 kV planar-gate MOSFETs with design optimizations to improve performance [1]–[4]. Various cell topologies (linear, square, hexagonal, octagonal) for 1.2 kV devices have been recently compared [5]–[6]. Impact of reducing the gate oxide thickness for 600-V 4H-SiC power MOSFETs has also been reported [7].

Overall power loss for a power MOSFET can be minimized by reducing the on-resistance (R_{on}), reverse-transfer capacitance (C_{gd}) and gate-drain charge (Q_{gd}). The High-Frequency Figures-of Merit (HF-FOMs), expressed as the products [$R_{on} \times C_{gd}$] and [$R_{on} \times Q_{gd}$], can therefore be used to evaluate relative performance of power MOSFETs for high frequency applications. Reduced values for the HF-FOM are desired to achieve improved performance. HF-FOMs for 1.2 kV 4H-SiC power MOSFETs can be significantly improved using the split-gate (SG) and buffered-gate (BG) structures [8]–[10].

Substituting 1.2 kV devices with 2.3 kV devices in solar inverter applications allows using a single-level versus more complex and expensive 2-level and 3-level converters [11]. Only a few studies discuss SiC MOSFETs with breakdown voltage of 2.0-2.5 kV [12]–[14], all based on the inversion-channel structure.

The split-gate concept is extended to 2.3 kV devices in this paper. For 1.2 kV 4H-SiC SG-MOSFETs, enhanced gate oxide electric field occurs at the SG electrode edge [8]. Optimization of the structure was required to make this electric field below 4 MV/cm to ensure reliable operation. The extension of this concept to 2.3 kV power MOSFETs is challenging due to the much larger operating voltage. The larger drain bias voltage of 2.3 kV compared with 1.2 kV for previous devices can lead to larger electric fields in the JFET region. This could produce electric field in the gate oxide that exceeds values required for reliable operation. It is therefore not obvious that the split-gate concept can be applied to 2.3 kV devices. In this paper, the successful fabrication of 2.3 kV split-gate 4H-SiC accumulation-channel planar power MOSFETs in a 6-inch commercial foundry with superior characteristics is reported, with assessment of quantified benefits, for the first time.

The 2.3 kV SG-MOSFETs discussed in this paper utilize an accumulation-channel structure. Accumulation-channel MOSFETs (or ACCUFETs) contain an n-type base-region which is completely depleted by the built-in potential of the junction between the P^+ shielding region and the

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

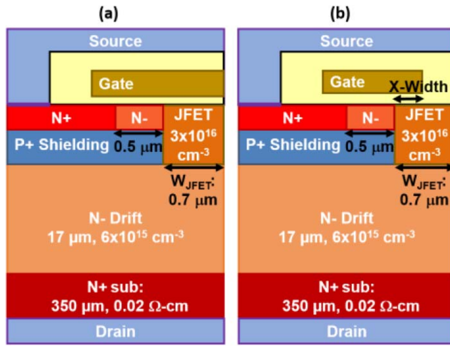

FIGURE 1. Cross-sections for the fabricated 2.3 kV 4H-SiC accumulation-channel linear cell power MOSFETs: (a) conventional structure and (b) split-gate (SG) structure.

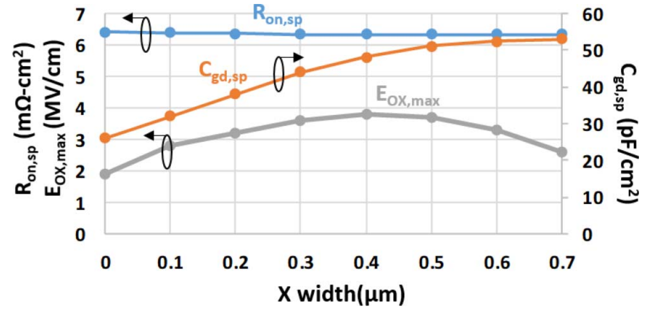

FIGURE 2. Simulation results for variation of specific on-resistance ($R_{on,sp}$), maximum gate oxide electric field ($E_{OX,max}$), and specific gate-drain capacitance ($C_{gd,sp}$) with dimension X in the SG-MOSFET structure.

N-base region. A positive gate bias above a threshold voltage is required to operate the device in its on-state just like inversion-channel structures. This produces the desired normally-off or enhancement mode device. The main benefit of the accumulation-channel is that its mobility has been shown to be about 2-times larger than the inversion-channel mobility [6]. It also allows obtaining a smaller threshold voltage. 1.2 kV SiC power MOSFETs with accumulation-channels have been shown to be superior to their inversion-channel counterparts due to lower specific on-resistance and superior switching characteristics [15]. A comparison of 1.2 kV inversion versus accumulation-channel split-gate (SG) MOSFETs was previously reported demonstrating the superior characteristics for the accumulation-channel devices [10]. For this reason, only accumulation-channel structures were chosen for this work on 2.3 kV SiC SG-MOSFETs.

II. DEVICE STRUCTURE AND ANALYSIS

Cross-sections for the fabricated linear cell accumulation-channel 4H-SiC conventional and split-gate (SG) planar power MOSFETs are shown in Fig. 1(a) and Fig. 1(b), respectively. The accumulation-channel structure with channel length of 0.5 mm is formed for both structures using an N-base region to obtain a larger channel mobility [6]. A JFET region with doping concentration of 3 x 10^{16} cm^{-3} and width of 0.7 mm was chosen based on experience in optimizing 1.2 kV devices [6].

Numerical simulations of both the conventional and split-gate 2.3 kV SiC power MOSFETs was performed using TCAD. The overlap of the gate electrode over the JFET region, called the X-width, was varied during the optimization. The specific on-resistance ($R_{on,sp}$) and reverse-transfer (gate-drain) capacitance ($C_{gd,sp}$) were obtained from the simulations. In addition, the electric field in the gate oxide was monitored.

Fig. 2 shows the results obtained for the specific on-resistance (@V_{gs} = 20 V and I_d = 10 A) with changes in the X-width. From the simulations results, it can be concluded that $R_{on,sp}$ has a weak dependence on the X-width. The specific gate-drain capacitance extracted @ V_{ds} = 1.2 kV is also shown in Fig. 2 with variation of the SG-electrode overhang (X-width). The value for $C_{gd,sp}$ decreases monotonically with smaller X-width due to reduction of the gate overlap area over the JFET region. Consequently, it is desirable to reduce the X-width as much as possible to obtain a low gate-drain capacitance ($C_{gd.sp}$) without sacrificing the magnitude of the specific on-resistance.

The maximum gate-oxide electric field, $E_{OX,max}$ @ V_{ds} = 2 kV occurs at the middle of the JFET region, i.e., the right-hand-edge of the structure shown in Fig. 1(a), for the conventional structure. In contrast, the maximum electric field in the gate oxide occurs at the edge of the polysilicon electrode above the JFET region in the split-gate structure. The values for $E_{OX,max}$ @ V_{ds} = 2 kV are plotted in Fig. 2 for the SG-MOSFET structure. The largest value for $E_{OX,max}$ occurs when the X-width is 0.4 µm. Lower values are observed for values smaller and larger than this value for reasons discussed previously for the 1.2 kV SG-MOSFETs [8].

As discussed above, the best performance for the 2.3 kV SiC power MOSFET is achieved by reducing the X-width as much as possible. During device fabrication, the X-width is determined by the alignment of the gate electrode patterning mask and the P^+ shielding region ion-implantation mask, which defines the edge of the channel. Based up on the foundry alignment design rules, an X-width of 0.3 µm was chosen for the fabricated 2.3 kV SG-MOSFET structure. This is the optimum value for the extension of the split gate electrode beyond the edge of the channel for reducing the gate-drain capacitance and charge while maintaining adequate process tolerances.

The conventional and SG-MOSFETs were simultaneously fabricated at a commercial foundry X-Fab on the same wafer with drift region doping concentration of 6 x 10^{15} cm^{-3} and thickness of 17 µm using the NCSU PRESiCE™ process [16]. This ensured that both the conventional and SG-MOSFETs had identical 55 nm gate oxide thickness (T_{ox}), 0.5 µm channel length (L_{CH}), 0.7 µm JFET width (W_{JFET}), and 3 x 10^{16} cm^{-3} JFET doping concentration to

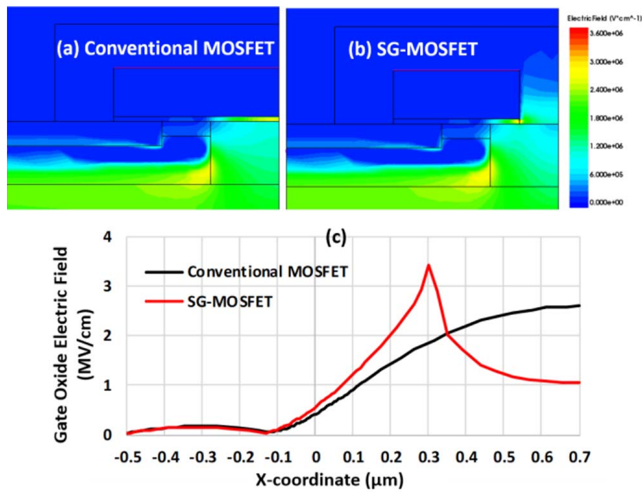

FIGURE 3. Electric field distribution maps obtained by numerical simulation for: (a) conventional MOSFET and (b) split-gate MOSFET. (c) Comparison of electric field in the gate oxide for conventional MOSFET (black) and SG-MOSFET (red) at drain bias of 2 kV.

allow comparison of performance. The active area for both devices was 0.045 cm^2.

It is worth comparing the electric field in the gate oxide for the fabricated 2.3 kV conventional and SG-MOSFET structures. The gate oxide electric field was obtained at a drain voltage (V_{ds}) of 2 kV by numerical simulations. The electric field map for the conventional and SG-MOSFET structures are shown in Fig. 3(a) and (b). A high electric field is observed at the corner of the P^+ shielding region in the SiC for both devices. The largest gate oxide electric field occurs at the middle of the JFET region for the conventional structure. In contrast, the maximum electric field in the gate oxide is observed at the edge of the gate electrode for the SG-MOSFET structure. The magnitude of the electric field in the gate oxide is shown in Fig. 3(c) for both structures. The electric field in the gate oxide has a maximum value of 2.8 MV/cm for the conventional MOSFET at the middle of the JFET region. In contrast, a maximum electric field of 3.6 MV/cm is observed at the edge of the gate electrode for the SG-MOSFET structure. Both values are below 4 MV/cm considered acceptable from reliability considerations [17]. This is an important observation from this work indicating that the Split-Gate concept can be applied to 2.3 kV 4H-SiC power MOSFETs.

The specific on-resistance of the 2.3 kV SG-MOSFET was observed to be weakly dependent on the X-width. The reason for this can be understood by comparing the current distribution within the conventional and SG-MOSFET structures using numerical simulations. Fig. 4 shows the on-state current distribution for the 2.3 kV conventional MOSFET and SG-MOSFET structures. The current flow pattern is nearly identical for both cases despite the absence of an accumulation layer above a portion of the JFET region in the SG-MOSFET structure. Consequently, the on-resistance remains unaffected by the split-gate electrode.

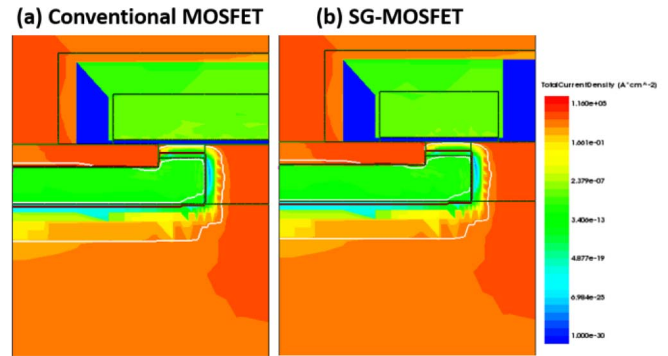

FIGURE 4. On-state (@ I_d = 10 A and V_{GS} = 20 V) current flow within the 2.3 kV (a) conventional MOSFET and (b) SG-MOSFET structures.

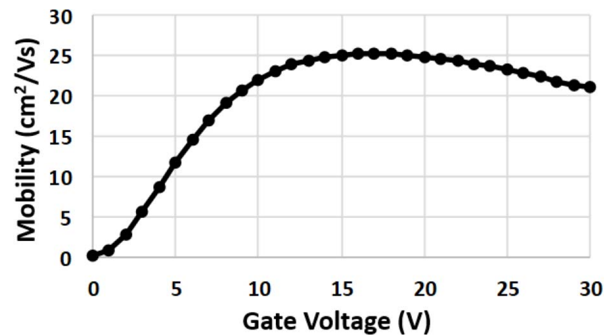

FIGURE 5. Measured accumulation-channel channel mobility in the 2.3 kV wafers using a lateral FATFET test structure.

III. EXPERIMENTAL RESULTS AND DISCUSSION

Previous studies have demonstrated higher mobility for electrons in accumulation-channel structures compared to inversion-channel structures [6]. For confirmation, the accumulation-channel mobility values for the MOSFETs in the 2.3 kV wafers used for this work were measured using a long-channel lateral test structure (FATFET). Fig. 5 shows the variation of mobility with gate voltage. It was found that the mobility peaks at 25 cm^2/Vs in the gate voltage range of 15-20 V. This is optimal for obtaining the smallest channel resistance contribution in the accumulation-channel 2.3 kV SiC power MOSFETs on the on-state. This mobility value is larger than the 15 cm^2/Vs value typically observed in inversion-channel devices [6].

The measured output characteristics of the 2.3 kV conventional MOSFET and SG-MOSFET were found to be nearly identical as shown in Fig. 6. This consistent with the results shown in the previous section with similar current distribution and on-resistance obtained with numerical simulations for the two cases. The on-resistance was extracted at a drain current of 10 A with a gate bias of 20 V. Data was measured for 60 devices of each type across the 6 inch wafer. The average and lowest (best) values obtained for the specific on-resistance for the SG and conventional MOSFET are given in Table 1. It is observed that the average $R_{on,sp}$ for the SG-MOSFET of 8.4 mΩ-cm^2 is slightly (4%) lower than the conventional MOSFET but within the standard deviation

TABLE 1. Experimental results.

Characteristics	MOSFET	SG-MOSFET
*Avg. $R_{on,sp}$ [mΩ-cm^2]	8.43 ± 8.5%	8.12 ± 7%
*Best $R_{on,sp}$ [mΩ-cm^2]	6.98	7.12
Avg. BV (@ I_d=100 μA) [V]	2390 ± 3.3%	2379 ± 3.6%
Avg. I_{leak} (@V_{ds}=1.2 kV) [nA]	3.0	12.5
V_{th} (@V_{ds}=0.1 V, I_d=1 mA) [V]	2.1	2.1
G_m (@V_{ds}=10 V, I_d=10 A) [S]	2.84	2.89
$C_{iss,sp}$ (@ V_{ds}=1 kV) [nF/cm^2]	28.4	30.0
$C_{oss,sp}$ (@V_{ds}=1 kV) [nF/cm^2]	0.75	0.75
$C_{rss,sp}$ (@ V_{ds}=1 kV) [pF/cm^2]	63	18
$C_{rss,sp}$ (@ V_{ds}=0 V) [pF/cm^2]	20585	5040
$Q_{gd,sp}$ [nC/cm^2]	356	202
HF-FOM (R_{on}*C_{rss}) [mΩ-pF]	531	146
HF-FOM (R_{on}*Q_{gd}) [mΩ-nC]	3001	1640
Best HF-FOM (R_{on}*C_{rss}) [mΩ-pF]	440	128
Best HF-FOM (R_{on}*Q_{gd}) [mΩ-nC]	2485	1438
FOM (C_{iss}/C_{rss})	451	1667

*$R_{on,sp}$ @I_d=10A, includes $R_{sub,sp}$ (~0.7 mΩ-cm^2)

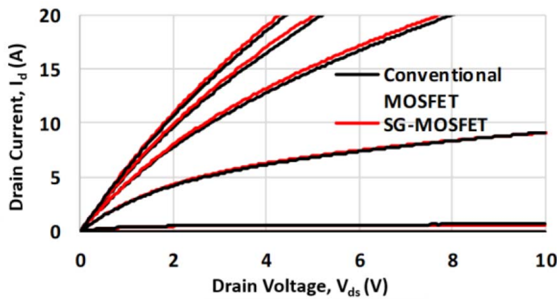

FIGURE 6. Measured output characteristics for 2.3 kV conventional MOSFET vs SG-MOSFET with gate bias up to 20 V in steps of 5 V.

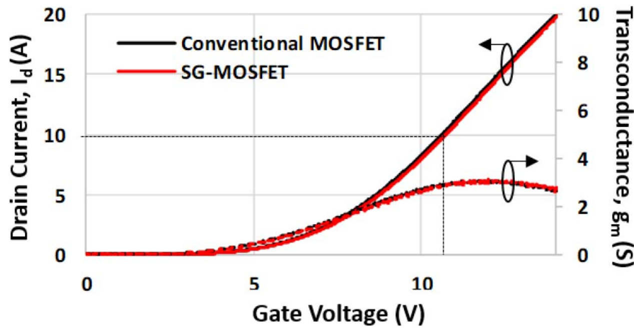

FIGURE 7. Measured transfer characteristics for 2.3 kV conventional MOSFET vs SG-MOSFET at V_{ds} = 10 V.

of 7-8 % for each device type. The lowest (best) value of 7.0 mΩ-cm^2 for the specific on-resistance for both cases is about 15% smaller than the average values.

Fig. 7 shows the transfer characteristics measured at $V_{ds} = 10$ V for the 2.3 kV conventional MOSFET and SG-MOSFET structures. It can be observed from Fig. 7 that, in spite of different gate design for the two structures, the transfer characteristics are nearly identical. The transfer characteristics for both MOSFETs are determined by the channel region [18]. The transfer characteristics are identical

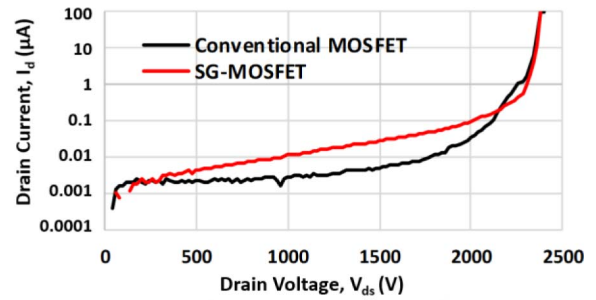

FIGURE 8. Measured blocking characteristics for the 2.3 kV conventional MOSFET vs SG-MOSFET at zero gate bias.

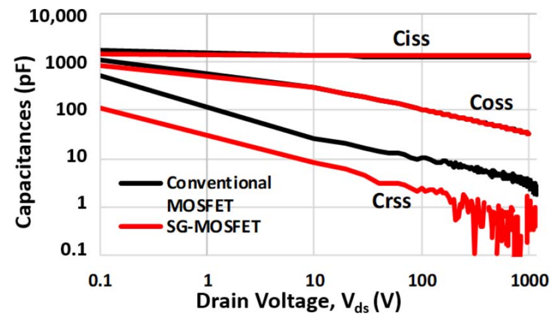

FIGURE 9. Measured input, output and reverse transfer capacitances (C_{iss}, C_{oss} and C_{rss}) for the 2.3 kV conventional MOSFET vs SG-MOSFET.

because both structures were simultaneously fabricated using the same channel region doping profile, channel length, and gate oxide thickness. Consequently, the SG-MOSFET structure has the same threshold voltage and transconductance as the conventional MOSFET structure. The measured V_{th} (at $V_{ds} = 0.1$ V and $I_{ds} = 1$ mA) and G_m (at $V_{ds} = 10$ V and $I_{ds} = 10$ A) values are listed in Table 1 for both structures. The peak in the transconductance occurs at a gate bias above 12 V, which is beneficial for improved switching performance [18].

The blocking characteristics for the SG-MOSFET structure can be compared to that for the conventional MOSFET structure in Fig. 8. The leakage currents for both structures are very low (< 0.1 μA) up to 2000 V and they have similar breakdown voltages of over 2.3 kV. The larger leakage current for the SG-MOSFET compared with the conventional MOSFET at lower drain bias voltages may be due to a larger electric field in the SiC drift region at the edge of the gate electrode for the SG-MOSFET. The magnitude for the leakage current for the SG-MOSFET is still sufficiently small to avoid any power dissipation problems. The average leakage current at 1.2 kV for both structures is provided in Table 1. The average breakdown voltages (BV) at 100 μA for both cases, obtained using 60 devices of each type across the 6-inch wafer, are >2300 V as documented in Table 1.

The measured input ($C_{\Omega iss}$), output (C_{oss}) and reverse-transfer capacitance (C_{rss}) are shown in Fig. 9 for the 2.3 kV conventional and SG-MOSFET devices. The measured C_{iss} for the two devices are very close because it is determined

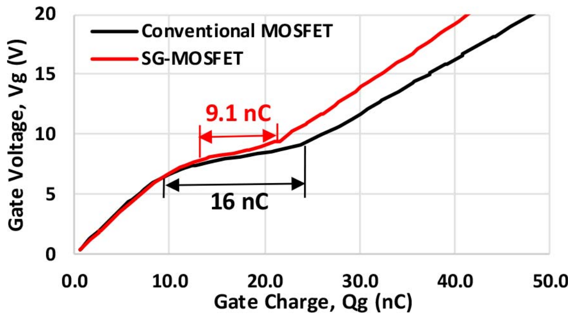

FIGURE 10. Measured gate charge at V_{ds} = 1200V and I_d = 10A for the 2.3 kV conventional MOSFET vs SG-MOSFET structures.

by the capacitance of the portion of the gate electrode that overlaps with the N^+ source and base regions [18]. The measured C_{oss} is also the same for both devices because it is determined by the area of the junction between the P^+ shielding region and the drift region [18], which is identical in the two devices. However, the measured C_{rss} for the SG-MOSFET can be seen to be significantly smaller as compared to the conventional MOSFET. The measured values for these capacitances are provided in Table 1 for comparison. The C_{rss} for the 2.3 kV SG-MOSFET is 3.4-4.0x smaller than that for the conventional MOSFET. This quantifies the benefits of applying the split-gate structure, with much smaller overlap between gate and drain, to SiC power MOSFETs with a higher blocking voltage capability of 2.3 kV for the first time.

The gate charge characteristics for the 2.3 kV conventional and split-gate devices were measured at V_{ds} = 1.2 kV and I_d = 10A. Both devices have the same plateau voltage as shown in Fig. 10 due to similar threshold voltage and transconductance values [18]. The gate-drain charge (Q_{gd}) for the 2.3 kV SG-MOSFET is observed to be much smaller (factor 1.76x) than that of the conventional MOSFET, verifying the benefits of reducing the gate-to-drain overlap. This data quantifies a second advantage of the split-gate structure to 2.3 kV SiC power MOSFETs.

Most (> 90 %) of the 60 dies for each of the 2.3 kV conventional MOSFET and SG-MOSFET structures were found to be functional on the 6 inch 4H-SiC wafer. Fig. 11(a) compares the specific on-resistance distribution for the conventional MOSFET (black) and the SG-MOSFET (red) devices. The distribution for both devices is very tight with a standard deviation of 7-9 %. The average $R_{on,sp}$ values for both devices is within 4 %, which is smaller than the standard deviation. This data demonstrates that the split-gate structure does not degrade the on-resistance value and its distribution for SiC power MOSFETs with a 2.3 kV breakdown voltage.

Box plots of leakage current (green) and breakdown voltage (purple) are shown in Fig. 11(b) for the two device structures based up on measurements taken on 60 devices of each type across the 6-inch 4H-SiC wafer. The average breakdown voltage of 2379 V for the SG-MOSFET is very close (within 0.5 %) to the conventional structure. This

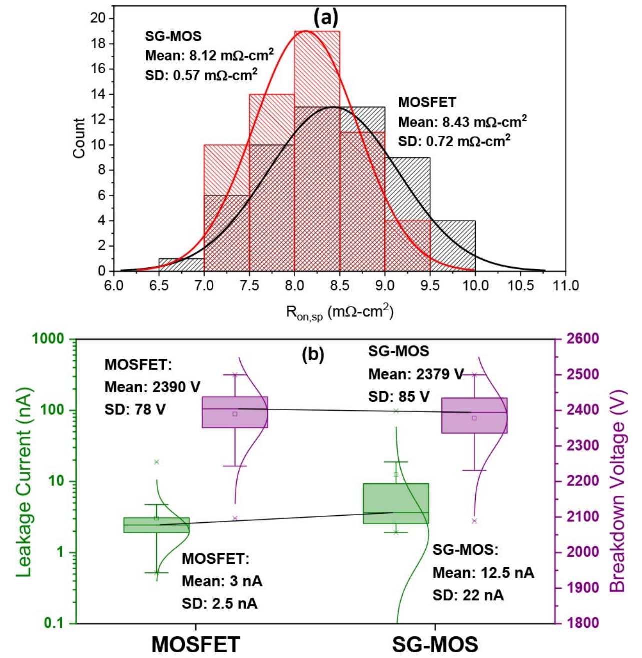

FIGURE 11. (a) $R_{on,sp}$ distribution for the 2.3 kV conventional MOSFET vs SG-MOSFET measured at V_{gs} = 20; (b) Leakage current (green) at 1200V and breakdown voltage (purple) for the conventional MOSFET and SG-MOSFET.

data demonstrates that the breakdown voltage of 2.3 kV SiC power MOSFETs is not compromised by using the split-gate structure. The average leakage current of 12.5 nA at 1.2 kV for the SG MOSFET structure is larger than the 3.0 nA for the conventional structure. It is still sufficiently small to avoid any power dissipation problems in the blocking mode.

IV. CONCLUSION

2.3-kV 4H-SiC split-gate (SG) power MOSFETs were successfully fabricated in a 6-inch commercial foundry. Their yield and parametric spread was close to that for the conventional MOSFET structure.

The high-frequency figures-of-merit HF-FOM[R_{on}*C_{rss}] and HF-FOM[R_{on}*Q_{gd}] are commonly used to assess the relative performance of power MOSFETs in applications with high operating frequency [18]. The calculated values for these figures-of-merit from the measured data on the fabricated 2.3 kV devices are provided in Table 1. It is found that the SG structure produces 3.5x reduction in C_{rss} at 1 kV resulting in a similar improvement in HF-FOM[R_{on}*C_{rss}]. The calculated HF-FOM[R_{on}*Q_{gd}] for the SG-MOSFET is 1.8x smaller than the conventional structure, which is beneficial for reducing the switching power loss in high-frequency applications. Another useful figure-of-merit for power MOSFET is the ratio of C_{iss} to C_{rrs}. A larger value for this ratio provides greater immunity against shoot-through currents under switching with high dV/dt in applications [18]. The FOM[C_{iss}/C_{rss}] for the 2.3 kV SG-MOSFET is 3.7× better than the conventional MOSFET

producing less vulnerability to shoot-through current in high frequency power circuits.

In conclusion, the split-gate structure has been experimentally demonstrated to significantly reduce the reverse-transfer capacitance and gate-to-drain charge for 2.3 kV SiC power MOSFETs without altering the specific on-resistance. This paper provides experimental documentation of the benefits of the split-gate structure for 2.3 kV 4H-SiC power MOSFETs for the first time.

REFERENCES

[1] Q. J. Zhang *et al.*, "Latest results on 1200 V 4H-SiC CIMOSFETs with Rsp, on of 3.9 mΩ· cm^2 at 150° C," in *Proc. 27th Int. Symp. Power Semicond. Devices IC's*, 2015, pp. 89–92, doi: 10.1109/ISPSD.2015.7123396.

[2] Y. Nanen, M. Aketa, Y. Nakano, H. Asahara, and T. Nakamura, "Electrical characterization of 1.2 kV-class SiC MOSFET at high temperature up to 380°C," *Mater. Sci. Forum*, vol. 858, pp. 885–888, May 2016, doi: 10.4028/www.scientific.net/MSF.858.885.

[3] W. Sung, K. Han, and B. J. Baliga, "Optimization of the JFET region of 1.2kV SiC MOSFETs for improved high frequency figure of merit (HF-FOM)," in *Proc. IEEE 5th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, 2017, pp. 238–241, doi: 10.1109/WiPDA.2017.8170553.

[4] S. Chowdhury, K. Matocha, B. Powell, G. Sheh, and S. Banerjee, "Next generation 1200V, 3.5mΩ.cm^2 SiC planar gate MOSFET with excellent HTRB reliability," in *Proc. 30th Int. Symp. Power Semicond. Devices IC's*, 2018, pp. 427–430, doi: 10.1109/ISPSD.2018.8393694.

[5] K. Han and B. J. Baliga, "The 1.2-kV 4H-SiC OCTFET: A new cell topology with improved high-frequency figures-of-merit," *IEEE Electron Device Lett.*, vol. 40, no. 2, pp. 299–302, Feb. 2019, doi: 10.1109/LED.2018.2889221.

[6] K. Han and B. J. Baliga, "Comparison of four cell topologies for 1.2-kV accumulation- and inversion-channel 4H-SiC MOSFETs: Analysis and experimental results," *IEEE Trans. Electron Devices*, vol. 66, no. 5, pp. 2321–2326, May 2019, doi: 10.1109/TED.2019.2905736.

[7] A. Agarwal, K. Han, and B. J. Baliga, "600 V 4H-SiC MOSFETs fabricated in commercial foundry with reduced gate oxide thickness of 27 nm to achieve IGBT-compatible gate drive of 15 V," *IEEE Electron Device Lett.*, vol. 40, no. 11, pp. 1792–1795, Nov. 2019, doi: 10.1109/LED.2019.2942259.

[8] K. Han, B. J. Baliga, and W. Sung, "Split-gate 1.2-kV 4H-SiC MOSFET: Analysis and experimental validation," *IEEE Electron Device Lett.*, vol. 38, no. 10, pp. 1437–1440, Oct. 2017, doi: 10.1109/LED.2017.2738616.

[9] K. Han, B. J. Baliga, and W. Sung, "A novel 1.2 kV 4H-SiC buffered-gate (BG) MOSFET: Analysis and experimental results," *IEEE Electron Device Lett.*, vol. 39, no. 2, pp. 248–251, Feb. 2018, doi: 10.1109/LED.2017.2785771.

[10] K. Han and B. J. Baliga, "Operation of 1.2-kV 4H-SiC accumulation and inversion channel split-gate (SG) MOSFETs at elevated temperatures," *IEEE Trans. Electron Devices*, vol. 65, no. 8, pp. 3333–3338, Aug. 2018, doi: 10.1109/TED.2018.2841940.

[11] X. She, P. Losee, H. Hu, W. Earls, and R. Datta, "Evaluation of 2.5 kV silicon carbide MOSFET for 1.5 kV solar inverter application," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, 2018, pp. 2516–2523, doi: 10.1109/ECCE.2018.8557524.

[12] K. Matocha, K. Chatty, S. Banerjee, and L. B. Rowland, "1700V, 5.5mΩ-cm^2 4H-SiC DMOSFET with stable 225°C operation," *Mater. Sci. Forum*, vol. 778, pp. 903–906, Feb. 2014, doi: 10.4028/www.scientific.net/MSF.778-780.903.

[13] A. Bolotnikov *et al.*, "Overview of 1.2kV–2.2kV SiC MOSFETs targeted for industrial power conversion applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2015, pp. 2445–2452, doi: 10.1109/APEC.2015.7104691.

[14] Q. J. Zhang *et al.*, "Next generation planar 1700 V, 20 mΩ 4H-SiC DMOSFETs with low specific on-resistance and high switching speed," *Mater. Sci. Forum*, vol. 897, pp. 521–524, May 2017, doi: 10.4028/www.scientific.net/MSF.897.521.

[15] A. Agarwal, A. Kanale, K. Han, B. J. Baliga, and S. Bhattacharya, "Experimental study of switching and short-circuit performance of 1.2kV 4H-SiC accumulation and inversion channel power MOSFETs," in *Proc. Int. Conf. Silicon Carbide Related Mater. (ICSCRM)*, 2019.

[16] B. J. Baliga, W. Sung, K. Han, J. Harmon, A. Tucker, and S. Syed, "PRESiCE^{TM}: Process engineered for manufacturing SiC electronic devices," *Mater. Sci. Forum*, vol. 924, pp. 523–526, Jun. 2018, doi: 10.4028/www.scientific.net/MSF.924.523.

[17] P. A. Losee *et al.*, "SiC MOSFET design considerations for reliable high voltage operation," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2017, pp. 2A-2.1–2A-2.8, doi: 10.1109/IRPS.2017.7936254.

[18] B.J. Baliga, *Fundamentals of Power Semiconductor Devices*, 2nd ed. Cham, Switzerland: Springer, 2019, ch. 6, pp. 394–403.