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Subthreshold Mismatch in Nanometer CMOS at Cryogenic Temperatures

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ABSTRACT Cryogenic device models are essential for the reliable design of the cryo-CMOS electronic interface necessary to build future large-scale quantum computers. This paper reports the characterization of the drain-current mismatch of NMOS and PMOS devices fabricated in a commercial 40-nm bulk CMOS process over the temperature range from 4.2 K to 300 K. By analysing the variability of device parameters over a wide range of device area and length, the validity of the Pelgrom area-scaling law is assessed for the threshold voltage, the current factor and the subthreshold swing. The Croon model is employed to model the drain-current mismatch in moderate to strong inversion, while the weak inversion region is modeled by taking the subthreshold slope variability into account. This results in the first model capable of predicting CMOS-device mismatch over all operating regions and in the whole temperature range from 300 K down to 4.2 K.

INDEX TERMS

I. INTRODUCTION

Quantum computers promise to solve several problems that are beyond the capability of today's supercomputers. They operate by processing the information stored in quantum bits (qubits), which must be typically cooled to deep-cryogenic temperatures below 1 K for proper operation and therefore reside in dilution refrigerators [1]. Although the actual computations are carried out by qubits, classical electronics is still required to control and readout the state of the qubits. Current state-of-the-art quantum processors comprise only a few tens of qubits [2], which are directly wired to conventional room-temperature control electronics. However, future quantum computers will require thousands or even millions of qubits in order to address any practical problem. Scaling to such a large number of qubits will be unpractical when using the current approach, as it will become infeasible to wire the thousands of cables required to connect the cryogenic qubits to the room-temperature electronics. To overcome these constraints, the control electronics can be placed in close proximity to the qubits, but, this requires that the classical electronics also operate at cryogenic temperatures. Since typical dilution refrigerators offer very low-cooling power (< 1 mW) at the mK-temperature stage, the preferred operating temperature for the electronics is above 4.2 K, at which significant cooling power (> 1 W) can be provided [3].

Nanometer CMOS operating at cryogenic temperature (cryo-CMOS) is the technology of choice by virtue of its high speed/bandwidth capability, its high level of integration and the potential to operate at temperatures as low as 30 mK [4], [5], which together enable the complex circuits required to control a very large number of qubits. Due to the limited cooling power, the power efficiency of those circuits is paramount. A very attractive solution is to operate cryo-CMOS circuits in the subthreshold region to minimize power consumption. The availability of accurate device models validated at cryogenic temperatures is indispensable for the

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design of such cryo-CMOS circuits. Although recent work has focused on cryogenic DC and RF models in advanced technology nodes [4], [6]–[8], mismatch models are still lacking for this target temperature range.

Device mismatch can severely limit the performance of many sensitive circuits, such as current/voltage references and data converters, that are essential components of the target cryo-CMOS controller. There is evidence in literature indicating a deterioration of mismatch at low temperatures [9]–[11], thus stressing even more the importance of the cryogenic modeling of this effect. Mismatch has been studied extensively over the military temperature range (−55–125°C) [9]–[13], including the subthreshold region [14]–[20]. Work on cryogenic device mismatch, however, has been limited to moderate to strong inversion [21]–[24]. To fill this gap, subthreshold device mismatch of a commercial 40-nm bulk CMOS technology was studied in [25], of which this paper is an extension. In this paper, the behaviour of the subthreshold drain current (I_D) is studied as a function of device geometry over the temperature range from 300 K (room temperature; RT) down to 4.2 K (liquid Helium temperature; LHT). In addition to the variability of threshold voltage (V_{TH}) and current factor (β), the subthreshold swing (SS) variability is specifically investigated for its impact on the subthreshold mismatch. Moreover, the validity of the Pelgrom area-scaling law for these three parameters is also assessed at both room and cryogenic temperatures. Furthermore, this work demonstrates a complete model of the drain-current mismatch, valid from the subthreshold to the strong inversion regime over the full temperature range from 300 K down to 4.2 K, which is obtained by combining the Croon model [26] and the subthreshold mismatch model [17].

This paper is structured as follows: a description of the devices under test, the measurement setup and parameter extraction is given in Section II; the mathematical foundations of the subthreshold and Croon models are established in Section III; the measurement results are presented in Section IV, which are discussed in Section V. Finally, a conclusion is drawn in Section VI.

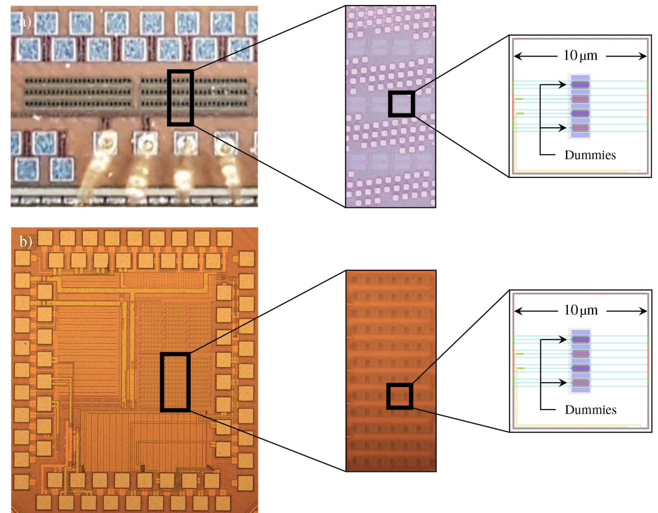

FIGURE 1. Micrograph of the chips used for mismatch characterization: (a) chip #1 comprising 3 different device geometries (results also presented in [25]); (b) chip #2 comprising an extended set of device geometries. Inset shows the layout details of the matched pairs.

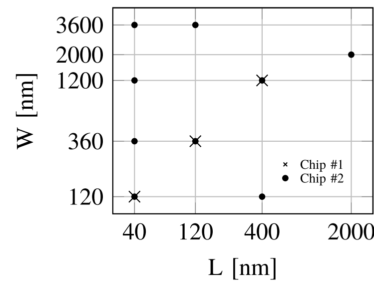

FIGURE 2. Device geometries available in the two test chips.

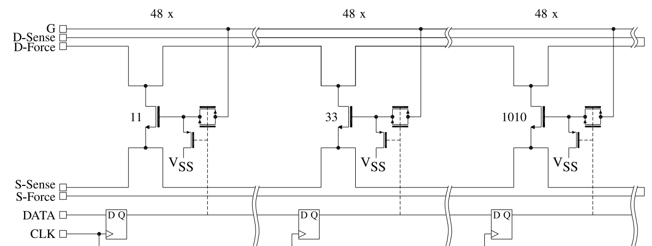

FIGURE 3. Simplified schematic of the NMOS mismatch characterization array of chip #1.

II. MEASUREMENT SETUP AND METHODS

A. MEASUREMENT SETUP

Two separate test chips were designed specifically to characterize subthreshold mismatch at cryogenic temperatures. Both chips were fabricated in the same 1.1-V 40-nm bulk CMOS process but in two different batches and comprise thin-oxide NMOS and PMOS devices with standard threshold voltage.

The first test chip (chip #1) enabled the characterization of three different device geometries laid out in a matched-pair configuration as indicated in Fig. 1a and Fig. 2. The results of the characterization of chip #1 have also been presented in [25]. A second test chip (chip #2, Fig. 1b) was designed to include 6 additional device geometries, as indicated in Fig. 2, thereby extending the scope of the work, e.g., to include mismatch dependency on device length.

A simplified circuit diagram of the NMOS array is shown in Fig. 3. A similar setup is adopted for PMOS devices. All devices (48 device pairs for each of the 3 geometries) share their drain and source terminals. When a device is selected, its gate is connected to a common bond pad through a transmission gate. When not selected, the gate is either connected to V_{SS} (for the NMOS) or V_{DD} (for the PMOS). Due to the higher threshold voltage at 4.2 K, the resistance of the transmission gate can significantly increase when biasing the device under test (DUT) in subthreshold. This, combined

with the gate current of the DUT, caused the anomalous drain current behavior reported in [25]. To overcome this limitation, the supply of the transmission gates was raised by 400 mV (up to 1.5 V) for all the characterization at 4.2 K, preventing the anomalous behavior. The transmission gates are controlled by a latched shift register to enable automatic characterization. The potential of the N-well and of the substrate is fixed by contact rings biased at $V_{DD} = 1.1$ V and $V_{SS} = 0$ V, respectively. Kelvin connections are made to the source and drain to mitigate the effect of series resistance in the measurement path, which is particularly important for the reliable extraction of device parameters in strong inversion where a non-negligible current is expected.

Chip #1 comprises one NMOS array and one PMOS array, each comprising 3 sets of 24 device pairs. Between the arrays, the shift register is daisy-chained and the gate pad is shared. Source and drain are routed to separate bond pads for each array, in order to minimize leakage. Chip #2 contains 3 NMOS arrays and 3 PMOS arrays. Their layout and connections are similar to those of chip #1. Device geometries with similar expected leakage were grouped in each array to increase the measurable subthreshold-current range.

Care was taken to reduce the impact of systematic mismatch, edge effects and mechanical stress by placing the devices in each pair at minimum distance with symmetrical connections, by surrounding them with identical dummy devices and by keeping metallization further than 5 µm away from the active devices, as indicated in Fig. 1.

It should be noted that these chips have been fabricated in a different 40-nm bulk CMOS process than the one presented in [21], [22] and that the test structures have been redesigned. This was necessary to minimize leakage and consequently, enable accurate subthreshold-current measurement.

For the electrical characterization, two Keithley 2636B Source Measurement Units (SMUs) were connected to the samples by low-leakage triaxial guarded connections. The measurement setup did not limit the lowest measurable current of the instruments, which is in the range of 10 fA. Since the time required to characterize a single die exceeds 36 hours due to the long instrument settling times associated with the low current range, an automated setup with samples directly submerged into liquid Helium is preferred over a manual setup with a cryogenic probestation. Intermediate temperatures between LHT and RT were reached by positioning the sample at different heights in the Helium vapour inside an Helium dewar.

For chip #1 and chip #2 a total of six dies (3 dies for chip #1; 3 dies for chip #2; 72 matched pairs per geometry) were characterized, both in triode ($|V_{DS}| = 50$ mV) and in the saturation region ($|V_{DS}| = 1.1$ V) at RT and at LHT. In addition to these two temperatures, the devices on chip #2 were also measured at 100 K and a single device of each geometry was characterized at 9 temperature points from 300 K down to 4.2 K.

All devices have been characterized sequentially in a 3-step procedure: 1) a single device is selected by loading

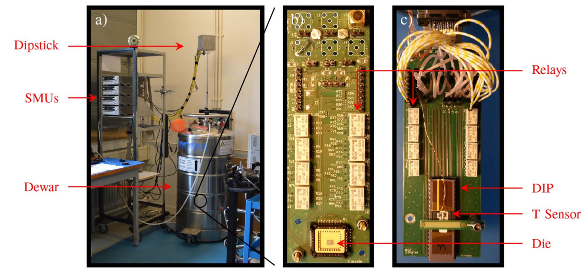

FIGURE 4. Measurement setup. (a): dipstick and instruments; (b) detail of the PCB designed for characterizing chip #1; (c) detail of the PCB for characterizing chip #2.

the correct bit pattern into the digital interface; the drain current is measured as a function of gate-source voltage (V_{GS}) and recorded; 2) the first measurement is repeated, but with fewer V_{GS} bias points to save time; 3) all devices are deselected and the measurement of the chip output is carried out a third time. Step 2 is employed to assess the Short Time Repeatability (STR) of the measurement setup, which is an indication of the reliability of the experiment and is used to guard against measurement error due to bad contacts, sudden (unintended) temperature changes and interference. The STR was always below 0.6 % over the bias range, thus not significantly impacting the measurement results. Step 3 characterizes the inevitable leakage of the array (∼4 nA at RT; <10 fA at LHT). To extend the subthreshold range to lower currents, the leakage is subtracted from the value of I_D measured in step 1. This corrected data is then used for data analysis.

Since the leakage is weakly bias and temperature dependent, a residual error remains after compensation. Data were discarded for low current ranges, to ensure that this error is always below 10 %. The array data was validated against individual devices directly accessible via reserved bond pads in chip #1.

As shown in Fig. 4, the dies were either wire bonded to a CLCC (chip #1) or a DIP package (chip #2). These PCBs were mounted at the tip of a dipstick, which was inserted into a liquid Helium dewar to reach cryogenic temperatures. The die temperature was continuously monitored with a Cernox temperature sensor. Temperature drift between the characterization of paired devices was below 10 mK at LHT, 1.1 K at RT and 0.3 K at 100 K. Due to a design error, the PMOS with W/L=120n/40n suffered from excess leakage current and are not included in the following analysis of subthreshold mismatch.

B. PARAMETER EXTRACTION

The device parameters relevant for drain-current mismatch modeling in strong inversion, i.e., V_{TH} and β, were extracted from the $I_D - V_G$ curves with the use of the Extrapolation in Linear Region (ELR) method [27]. The ELR method was chosen for its reliability over the other two well-known methods, i.e., the constant current [27] and the 3-point [28] method, as it does not depend on arbitrarily chosen extraction

points. Moreover, it was verified that the ELR results fit very well with the mismatch models employed in this work.

The subthreshold swing is an important device parameter in the subthreshold mismatch model. It is extracted by calculating the inverse slope of a line through two I_D points in the subthreshold regime:

$$SS^{-1} = \frac{\left|\log\left(I_{D_{hi}}/I_{D_{lo}}\right)\right|}{V_{GS_{hi}} - V_{GS_{lo}}}, \quad (1)$$

where the '*hi*' and '*lo*' subscripts indicate a bias point at the edge between weak and moderate inversion and a bias point at the lowest current above the measurement limit, respectively.

As Drain Induced Barrier Lowering (DIBL) decreases the V_{TH} for devices in saturation, the value extracted by ELR in triode will be over-estimated. Therefore, for these devices, the V_{TH} term in Eq. (5) is extracted with the use of the Extrapolation in Saturation Region (ESR) method [27], which captures the impact of DIBL.

III. MODELING

The subthreshold drain current is modeled by the simplified exponential equation:

$$I_D = I_0 e^{(V_{GS} - V_{TH})/SS}, \quad (2)$$

where I_0 is a temperature and geometry-dependent constant. Due to both the exponential nature and the increased I_D variability in this operating regime at cryogenic temperatures, Taylor expansion of Eq. (2) becomes impractical, thus making it more appropriate to use a logarithmic transform with base 10 [14], [17]:

$$\log(I_D) \propto \frac{1}{\ln(10)} \frac{V_{GS} - V_{TH}}{SS}. \quad (3)$$

If we assume V_{TH} and SS to be the sources of variability, a first-order Taylor expansion of Eq. (3) yields:

$$\Delta \log(I_D) = \frac{1}{\ln(10)}\left[-\frac{1}{SS}\Delta V_{TH} - \frac{(V_{GS} - V_{TH})}{SS}\frac{\Delta SS}{SS}\right]. \quad (4)$$

The subthreshold drain-current mismatch can then be modeled by the variance of Eq. (4) as [17]:

$$\sigma^2_{\Delta \log I_D} = \frac{1}{\ln(10)^2}\left[\left(\frac{\sigma_{\Delta V_{TH}}}{\overline{SS}}\right)^2 + \left(\frac{\overline{V_{GS} - V_{TH}}}{\overline{SS}}\frac{\sigma_{\Delta SS}}{\overline{SS}}\right)^2 + 2\frac{\overline{(V_{GS} - V_{TH})}}{\overline{SS}^3}\sigma_{\Delta V_{TH}}\sigma_{\Delta SS}\rho_{\Delta V_{TH},\Delta SS}\right]. \quad (5)$$

Here the overline indicates the average value over all matched pairs with a given geometry and $\rho_{\Delta V_{TH},\Delta SS}$ is the correlation coefficient between ΔV_{TH} and ΔSS. This correlation was found to be statistically insignificant at RT, 100 K and LHT. Therefore, this term is ignored in the following analysis.

The drain-current mismatch over all temperatures in moderate to strong inversion is modeled by the Croon model [26], as such model has already been proven to apply at cryogenic temperatures in [22]. It can be shown that:

$$\sigma^2_{\Delta I_D/I_D} = \ln(10)^2 \sigma^2_{\Delta \log I_D}, \quad (6)$$

therefore the Croon model is expressed as:

$$\sigma^2_{\Delta \log I_D} = \frac{1}{\ln(10)^2}\left[\sigma^2_{\Delta\beta/\beta} + \left(\frac{\bar{g}_m}{\bar{I}_D}\right)^2 \sigma^2_{\Delta V_{TH}}\right], \quad (7)$$

where g_m is the transconductance of the devices. For the Croon model in Eq. (7), no correlation term is introduced, as it is typically neglected in moderate/strong inversion [22], [26].

The increased subthreshold mismatch resulting from the increased SS variability cannot adequately be modeled by Eq. (7), therefore the Croon model is only used outside the subthreshold region. In weak inversion, the subthreshold model of Eq. (5) is employed.

Pelgrom's scaling law [12] is used to model the area dependency of $\sigma_{\Delta V_{TH}}$, $\sigma_{\Delta\beta/\beta}$ and $\sigma_{\Delta SS/SS}$:

$$\sigma_{\Delta V_{TH}} = \frac{A_{VT}}{\sqrt{WL}} \quad \sigma_{\Delta\beta/\beta} = \frac{A_\beta}{\sqrt{WL}} \quad \sigma_{\Delta SS/SS} = \frac{A_{SS}}{\sqrt{WL}} \quad (8)$$

where A_{VT}, A_β and A_{SS} are the threshold-voltage, current-factor and subthreshold-swing area-scaling parameters, respectively, and WL is the device active area. By combining Eq. (8) with (5) and (7), the drain-current mismatch for any device geometry can be computed.

Finally, it is important to note that the model parameters in Eq. (5) and (7) ($\sigma_{\Delta V_{TH}}$, $\sigma_{\Delta\beta/\beta}$ and $\sigma_{\Delta SS/SS}$) have not been selected to fit the proposed models to the measured data. Instead, the mismatch in each parameter (V_{TH}, β, SS) was extracted from the $I_D - V_G$ data of each pair and subsequently used to compute the respective standard deviation used in the models described by Eq. (5) and (7). This is a strong argument for the validity of the adopted model.

IV. EXPERIMENTAL RESULTS

Fig. 5 shows the $I_D - V_G$ characteristics for 48 NMOS and PMOS devices from a single die at RT, 100K and LHT. The temperature impact on the three relevant parameters can clearly be identified: V_{TH} increases ($V_{TH_{4.2K}} - V_{TH_{300K}} \approx$ 100 mV), mobility increases ($\beta_{4.2K}/\beta_{300K} \approx 2\times$) and SS decreases ($SS_{300K} \approx 90$ mV/dec $\rightarrow SS_{4.2K} \approx 20$ mV/dec), which is consistent with prior works [4], [6], [22].

To investigate the cryogenic subthreshold drain-current behavior, additional measurements were carried out over a larger set of temperatures. Fig. 6a shows the $I_D - V_G$ curves of a single W/L=1.2μ/40n NMOS device at intermediate temperatures between RT and LHT in steps of 40 K. It is clear from this plot that the SS value decreases down to 40 K after which it starts to saturate.

To study the impact of device geometry on SS, Fig. 6b shows data at LHT for NMOS devices from all available geometries, demonstrating a very weak sensitivity to device geometry.

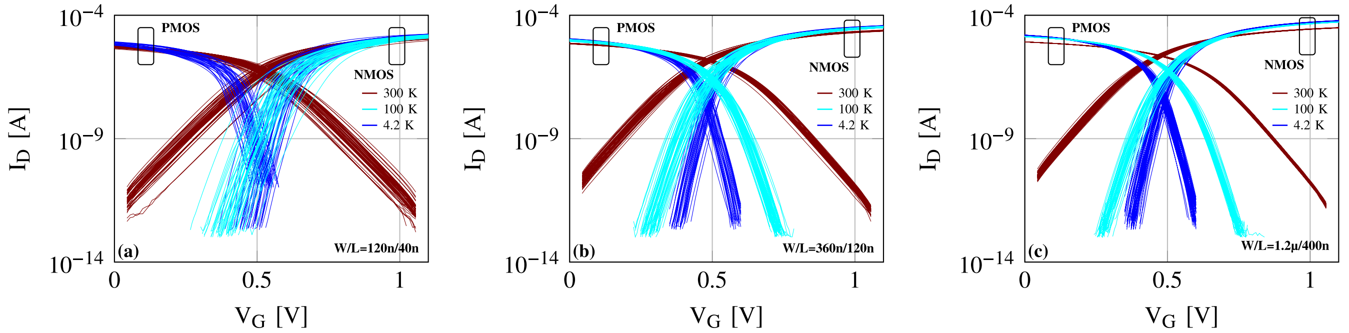

FIGURE 5. $I_D - V_G$ curves for a single die (48 devices per geometry) at T = 300 K, 100 K and 4.2 K: (a) W/L=120n/40n; (b) W/L=360n/120n and (c) W/L=1.2µ/400n. $|V_{DS}|$ = 50 mV. V_S = 0 V for NMOS and 1.1 V for PMOS, respectively.

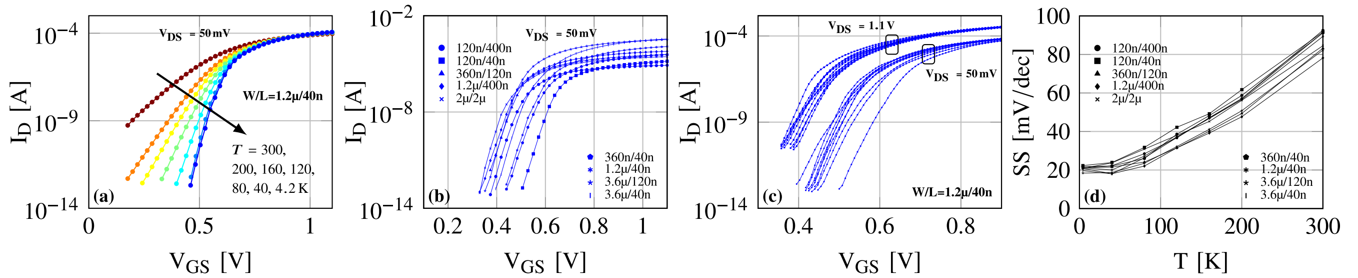

FIGURE 6. NMOS device behaviour over temperature: (a) $I_D - V_G$ curves of a W/L=1.2µ/40n device; (b) $I_D - V_G$ curves of all 9 geometries at T = 4.2 K; (c) $I_D - V_G$ curves of 10 W/L=1.2µ/40n devices at T = 4.2 K and (d) extracted SS (V_{DS} = 50 mV) as function of temperature for all 9 geometries.

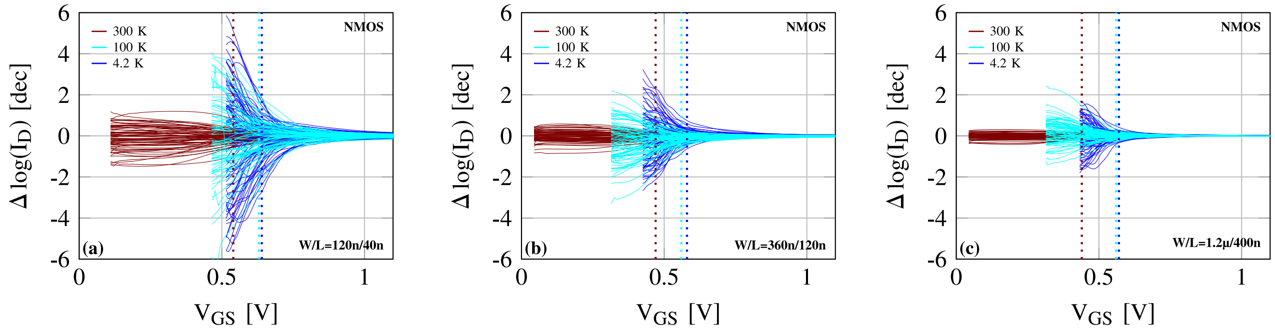

FIGURE 7. NMOS drain-current mismatch of 72 device pairs (3 dies) at T = 300 K, 100 K and 4.2 K: (a) W/L=120n/40n; (b) W/L=360n/120n and (c) W/L=1.2µ/400n. V_{TH} marked by dashed lines. V_{DS} = 50 mV.

To assess the subthreshold drain-current variability for devices with equal geometry, the drain current of 10 NMOS devices with W/L=1.2µ/40n at T = 4.2 K, biased both in triode (V_{DS} = 50 mV) and saturation (V_{DS} = 1.1 V), is reported in Fig. 6c. A slight V_{TH} decrease due to DIBL and a subthreshold current increase can clearly be seen for the saturated devices with respect to those operated in triode. The impact of the V_{TH} and SS variability on the subthreshold drain-current distribution is clearly visible in this plot.

To be complete, the temperature behaviour of the extracted SS for all 9 available NMOS geometries is shown in Fig. 6d. SS improves with decreasing temperature up to 4× from RT to LHT. At temperatures below 40 K, the slope saturates (see Fig. 6a). Similar curves are obtained for the PMOS devices.

To investigate subthreshold mismatch, $\Delta\log(I_D) = \log(I_{D1}) - \log(I_{D2})$ was computed for 72 device pairs at RT, 100 K and LHT, as plotted in Fig. 7. The combination of the increased V_{TH} and the steeper SS causes I_D to reach the instrument's current floor at a much higher V_{GS} at cryogenic temperatures compared to RT. The subthreshold mismatch is orders of magnitude higher at LHT compared to RT, which is attributed to an increased SS mismatch further exacerbated by the steeper subthreshold slope.

Pelgrom plots for $\sigma_{\Delta V_{TH}}$, $\sigma_{\Delta\beta/\beta}$ and $\sigma_{\Delta SS/SS}$ are shown in Fig. 8 and Fig. 9 for PMOS and NMOS, respectively. The linear fittings are inversely weighted with the 95 % confidence bounds, with the slopes representing the A-factors in Eq. (8). For both NMOS and PMOS devices, the Pelgrom law is effective in modeling $\sigma_{\Delta V_{TH}}$ and $\sigma_{\Delta\beta/\beta}$ at RT, 100 K and LHT.

The $\sigma_{\Delta SS/SS}$ dependency on area plotted in Fig. 8c and Fig. 9c can be successfully modeled by the Pelgrom law at

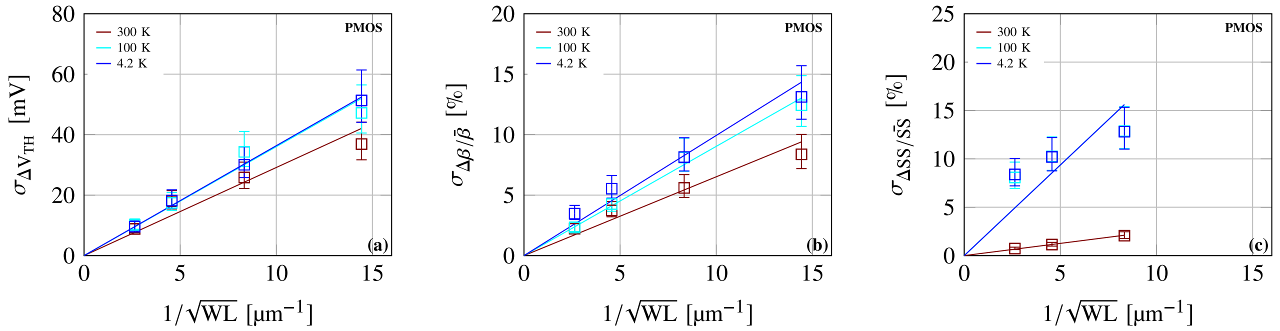

FIGURE 8. Pelgrom plots of PMOS with L=40n device length at T = 300 K, 100 K and 4.2 K for: (a) $\sigma_{\Delta V_{TH}}$; (b) $\sigma_{\Delta\beta/\beta}$ and (c) $\sigma_{\Delta SS/SS}$. 95% confidence intervals are shown.

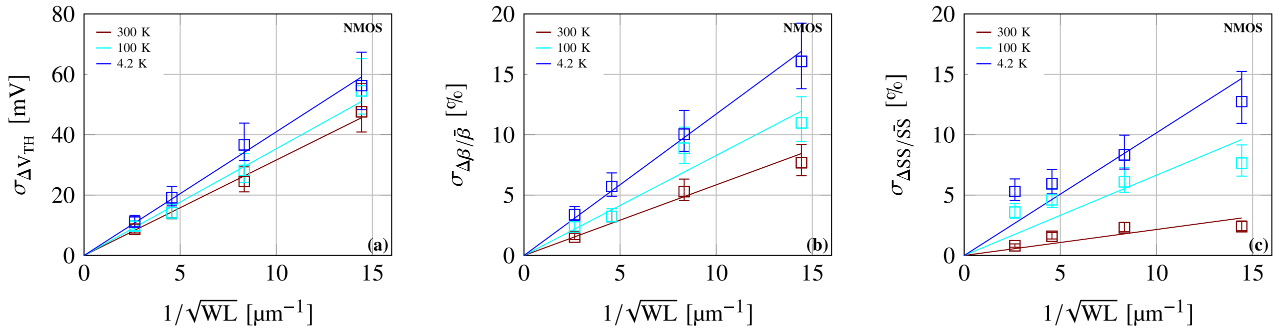

FIGURE 9. Pelgrom plots of NMOS with L=40n device length at T = 300 K, 100 K and 4.2 K for: (a) $\sigma_{\Delta V_{TH}}$; (b) $\sigma_{\Delta\beta/\beta}$ and (c) $\sigma_{\Delta SS/SS}$. 95% confidence intervals are shown.

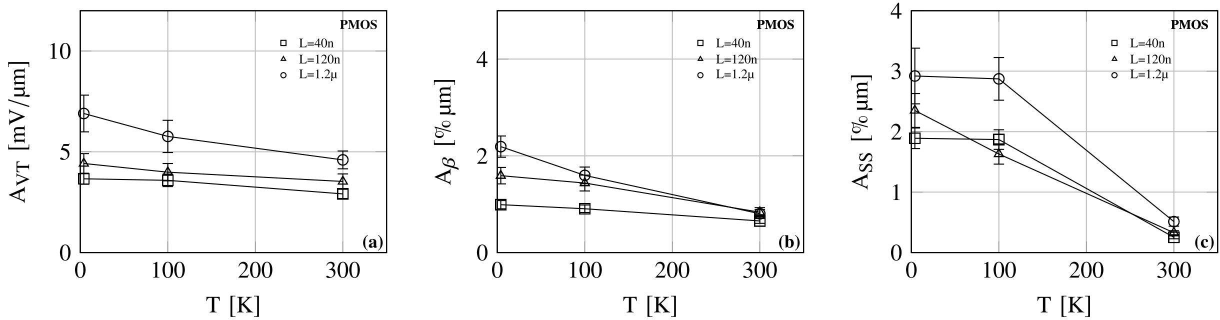

FIGURE 10. A-factors as a function of temperature for 3 different PMOS device lengths: (a) A_{VT}; (b) A_{β} and (c) A_{SS}. 95% confidence intervals are shown.

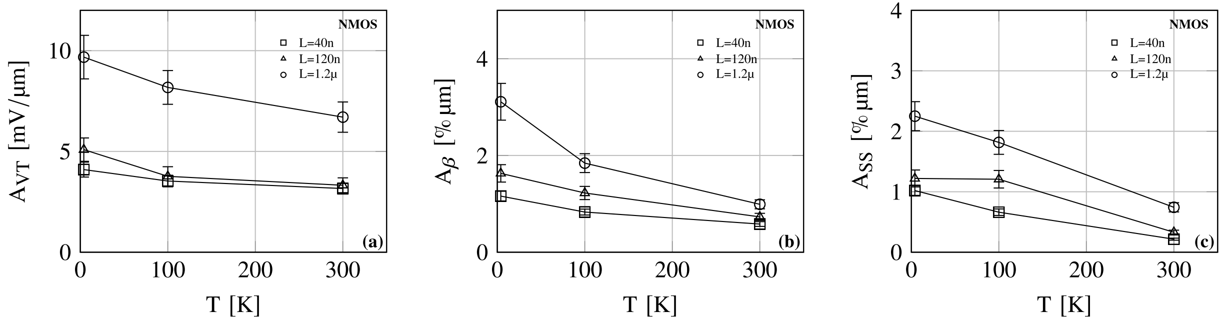

FIGURE 11. A-factors as a function of temperature for 3 different device NMOS lengths: (a) A_{VT}; (b) A_{β} and (c) A_{SS}. 95% confidence intervals are shown.

RT, 100 K and LHT. Only devices with L=40n are shown in these plots for clarity.

The temperature and length dependency of the extracted A-factors is shown in Fig. 10 and Fig. 11 with error bars representing 95 % confidence intervals. For both NMOS and PMOS, A_{VT} shows a significant increase of $\sim$1.5× at LHT with respect to RT for L=400n, while no significant increase is observed for L=40n. A_{β} increases significantly over the

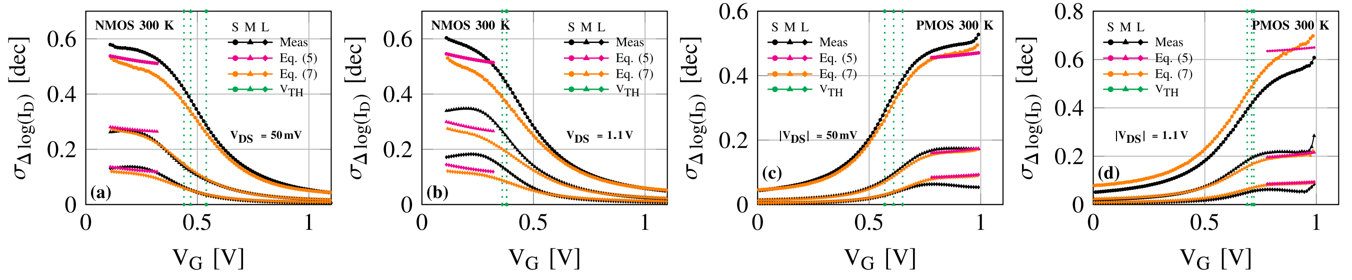

FIGURE 12. Drain-current mismatch as function of gate bias for 3 geometries at T = 300 K: S (W/L=120n/40n); M (W/L=360n/120n) and L (W/L=1.2μ/400n). V_{TH} and V_{DS} indicated in each figure. V_S = 0 V for NMOS and 1.1 V for PMOS.

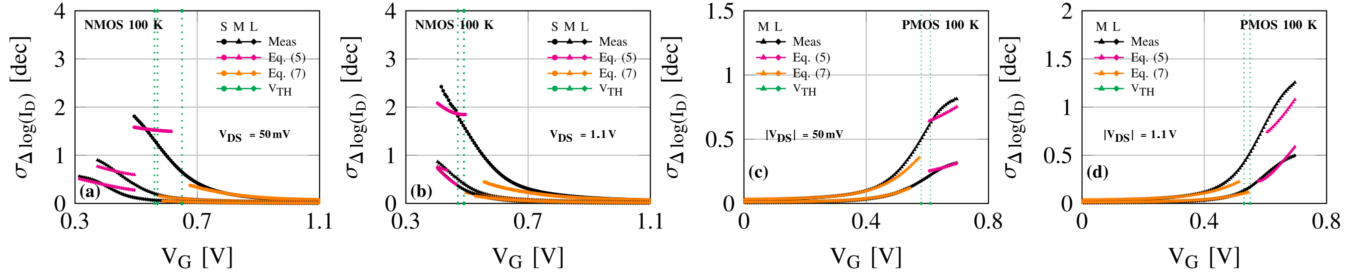

FIGURE 13. Drain-current mismatch as function of gate bias for 3 geometries at T = 100 K: S (W/L=120n/40n); M (W/L=360n/120n) and L (W/L=1.2μ/400n). V_{TH} and V_{DS} indicated in each figure. V_S = 0 V for NMOS and 1.1 V for PMOS.

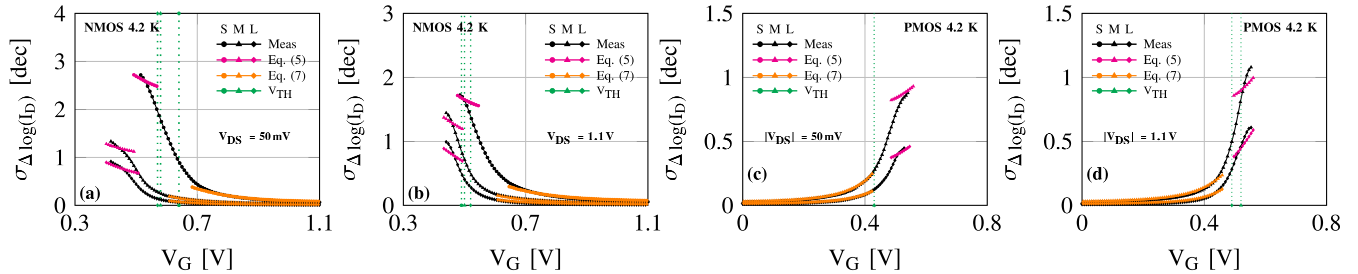

FIGURE 14. Drain-current mismatch as function of gate bias for 3 geometries at T = 4.2 K: S (W/L=120n/40n); M (W/L=360n/120n) and L (W/L=1.2μ/400n). V_{TH} and $|V_{DS}|$ indicated in each figure. V_S = 0 V for NMOS and 1.1 V for PMOS.

same temperature range: ∼2× for N- and PMOS devices with L=40n and up to ∼4.2× for L=400n NMOS devices, respectively. For all lengths, A_{SS} significantly increases by ∼3× and ∼5× at 100 K compared to RT for NMOS and PMOS devices, respectively. Below 100 K, A_{SS} saturates or increases only slightly.

Drain-current mismatch for devices operating in triode and saturation at various temperatures and geometries is plotted in Fig. 12, 13 and 14, together with the Croon and the subthreshold models of Eq. (5) and (7). It should be noted that the $\sigma_{\Delta V_{TH}}$, $\sigma_{\Delta\beta/\beta}$ and $\sigma_{\Delta SS/SS}$ used in these two equations are the same as reported for the Pelgrom plots and have been directly derived from the measurements and not by fitting the models. Only 3 of the 9 available geometries are shown here for brevity, but similar trends hold for the omitted curves.

At 300 K, in Fig. 12, both the Croon and the subthreshold models are able to predict mismatch over the full bias range for both NMOS and PMOS and in all operating regimes. At RT, drain-current mismatch reaches a plateau in the subthreshold region due to the low variability of SS at RT.

Drain-current mismatch at 100 K, as plotted in Fig. 13, shows an increased subthreshold mismatch compared to RT. The Croon model is capable of fitting the data in strong to moderate inversion, but it ceases to be adequate in subthreshold. The subthreshold model is able to give a better prediction in this region.

In Fig. 14, the subthreshold mismatch at LHT increases further compared to 100 K, which is in line with the $\Delta\log(I_D)$ plots in Fig. 7 while the trend of the curves stays similar with those at RT and 100 K. The Croon model is again able to predict mismatch in strong to moderate inversion but the subthreshold model needs to be employed for weak inversion.

V. DISCUSSION

As mentioned in Section II-A, the anomalous behavior previously reported in [25] was identified as an artifact due to an excessive parasitic resistance in series to the gate of the DUT. Although those artifacts have been eliminated in this paper, discontinuities in the SS were still observed at

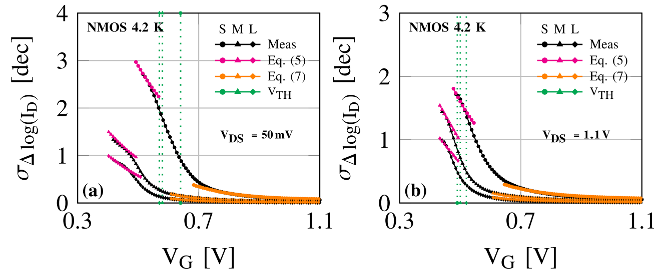

FIGURE 15. Drain-current mismatch modeled using the Croon and the subthreshold model and tuning $\sigma_{\Delta SS/SS}$ and $\sigma_{\Delta V_{TH}}$ for the best fit between experimental data and models: (a) $V_{DS} = 50$ mV; (b) $V_{DS} = 1.1$ V.

4.2 K both in the multiplexed devices and in separate bare, pad-accessible devices, similar to the observations in prior work [7], [29]–[32]. Such behavior was attributed to resonant electron/hole tunneling through a quantum dot (QD) [29] or through the electronic states of dopants [7], [31], [32], to the freeze-out of superficial impurities [30] or to conduction at the device edges [30]. Because of the significant random nature of those mechanisms, a severe impact on subthreshold matching could be expected. However, since the *SS* is extracted here from the average subthreshold slope over a wide current range, local discontinuities of *SS* cannot be captured. Although the model in Fig. 14 uses the variability of the *SS* extracted in this way, it is still able to accurately match the measured data, thus pointing to a negligible impact of those small *SS* discontinuities on the subthreshold mismatch statistics.

The observed length dependency of $\sigma_{\Delta V_{TH}}$ and $\sigma_{\Delta\beta/\beta}$ (see Fig. 8 and 9) is compatible with prior results presented in [22].

Based on the A-factors for L=40n, for which the largest number of geometries are available and, hence the highest accuracy is reached, it can be concluded that A_{VT} has no statistically significant variation with temperature, while A_β and A_{SS} increase significantly from RT to LHT.

As highlighted in Section IV, the Croon model is able to accurately predict mismatch in moderate to strong inversion at all temperatures and bias conditions, as also demonstrated in [22], while the subthreshold model must be adopted in weak inversion. Although the models and the experimental data already show good agreement when using $\sigma_{\Delta V_{TH}}$, $\sigma_{\Delta\beta/\beta}$ and $\sigma_{\Delta SS/SS}$ extracted from the measurements, as described in Section II-B and IV, an even smaller discrepancy is obtained when fitting the models described in Eq. (5) and (7) with the experimental data, as shown in Fig. 15.

VI. CONCLUSION

This paper reports, for the first time, the characterization and modeling of the subthreshold device mismatch of CMOS devices at cryogenic temperatures. Mismatch increases at cryogenic temperatures in all operating regions and, in particular, subthreshold matching deteriorates by more than several orders of magnitude. As the Croon model does not take subthreshold-swing variability into account, a specific subthreshold model is shown to adequately model mismatch in the weak inversion region at these temperatures. Improving matching by increasing the device area as predicted by Pelgrom law proves to be valid at cryogenic temperatures in all operating regions including subthreshold. As a result, the proposed mismatch models can become an essential tool for the design of the cryo-electronics that will enable scalable quantum computers.

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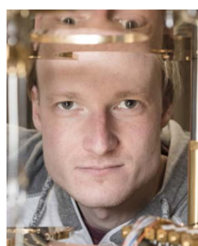

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