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Reset Variability in Backfilled Resistive Random Access Memory and Its Correlation to Low Frequency Noise in Read

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ABSTRACT Fast and stable switching between states is one of the key factors for the success resistive random access memory (RRAM) development. In an array, wide reset efficiency variation in RRAM cells is found to link to the characteristics of its low frequency noise (LFN) in bit-cell current. Through Monte Carlo simulation on randomly placing conductive filaments (CF), LFN characteristics correspond to the densities of the CF in the RRAM film. Further correlations between LFN features and the reset efficiency are found. In addition, CF topography are found to change after long term cycling tests. A trimming process is proposed to minimize the impacts of stochastic CF generation, leading to increase reset speed.

INDEX TERMS Variability, resistive random access memory, low frequency noise, Monte Carlo simulation, conductive filament.

I. INTRODUCTION

In recent years, resistive random access memory (RRAM) has been regarded as a promising solution with very competitive features for meeting the needed to expanding embedded nonvolatile storage demands [1]–[3]. With advantages such as its simple structure, superior scalability and high compatibility to CMOS processes, RRAM becomes very competitive for various embedded non-volatile memory applications [4]–[6]. However, variabilities from device-to-device and between cycles have become one of the most critical challenges in the development of RRAM as a reliable storage medium [7]–[10].

The generation/recombination of oxygen vacancies (Vo) occurred during set/reset operation, corresponding to the construction/rupture conductive paths, are believed to responsible for resistive switching characteristics in RRAM film [11]–[13]. Oxygen vacancies based RRAM can be categorized into two types based its operational model, namely, bipolar mode and unipolar cells [14]–[16]. For bipolar devices, positive and negative biases are applied respectively for set and reset. It enables drift force to be applied in opposite directions, pushing oxygen ion from and to its source electrode [17], [18]. For unipolar RRAM, set operations are identical with that in bipolar devices, triggered by high electric field, while its reset mechanism is believed that is attributed to Joule heating assisted diffusion of oxygen ion [19]. Raised temperature as a result of local heating enhances the diffusion of oxygen ion and the recombination with Vo, increasing the resistance levels [20], [21].

Stochastic process in the generation/recombination of oxygen vacancies during set/reset operation, resulting in random changes in its conductive paths, has been found as one of root causes of RRAM variability [22]–[24]. To directly monitor the change in CF properties in transition metal oxide (TMO) layer, imaging tools, such as transmission electron microscopy (TEM) and atomic force microscope (AFM), were used for detail physical analysis [25]–[28]. In addition, monitoring random telegraph noise (RTN) and LFNs of RRAM have also been proposed as a pathway for probing the miniscule changes in the shape and distribution of CFs [29]–[32]. In these proposed studies, properties of defects and CFs in dielectric film are characterized by this unique charge trapping/detrapping behavior. Numerical models to correlate noise characteristics with CF diameters has been reported for more detail understanding of the underline

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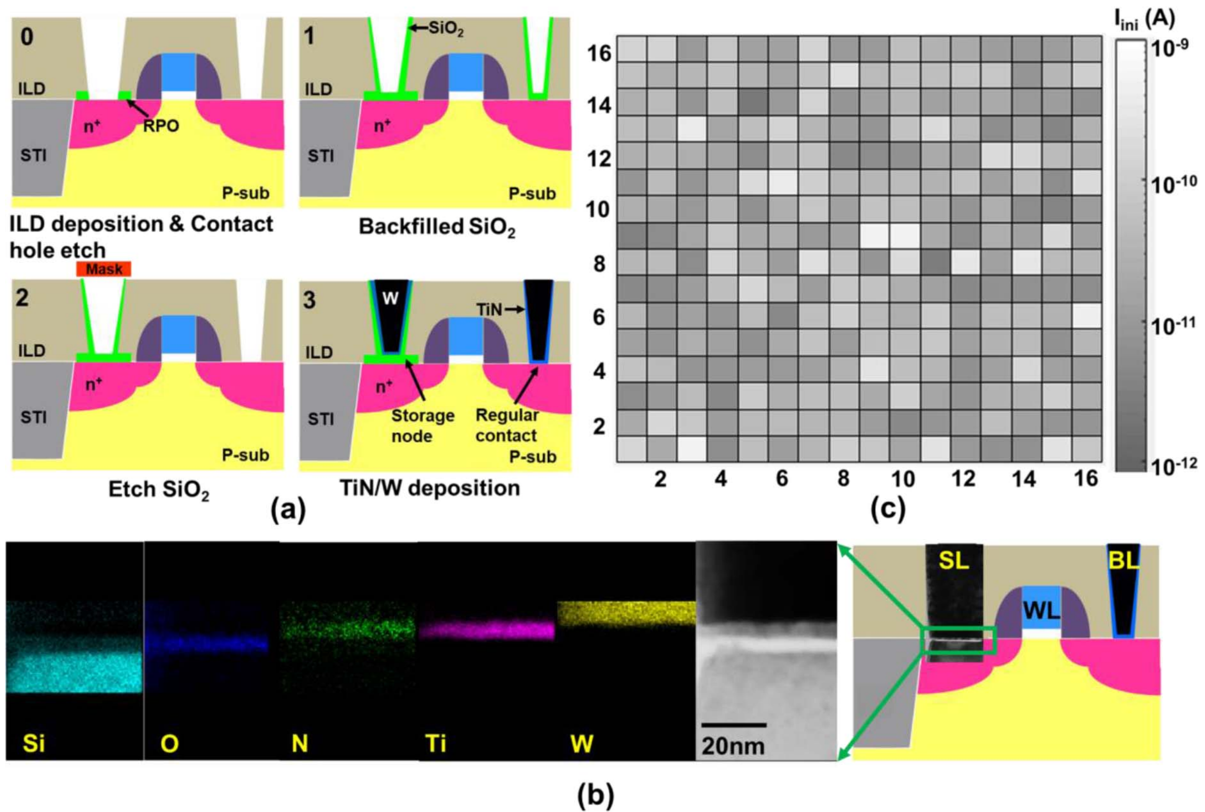

FIGURE 1. **(a) Process flow of BCRRAM in a CMOS logic process platform. (b) Composition mapping of the TMO layer, TiN/TiON/SiO_2 stacks sandwiched between tungsten plug and n^+ diffusion region. (c) Bit map of read current in pristine state of 16 × 16 NOR type BCRRAM memory array.**

sources of the change in device characteristics [30]. On the other hand, the dependence of capture/emission time constants on bias voltage was studied to investigate trap location in dielectric film [31]. Models including multiple time constants were reported to further track the shifts in trap-sites at different stress stages [32]. Aside from analysis of properties of defects and traps in the TMO film, RTN was also regarded as an index to examine endurance of cells. Chai *et al.* provided a RTN-based technique to monitor the spatial and energy profile of filament, which further links set failure with trap locations and energy level [29]. These studies have shown that RTN signals in RRAM cells become windows for researchers to probe the properties of CF and Vo, providing new links for in-depth analysis.

In this study, the connections between the topographies of CF and LFN signals are first established by Monte Carlo simulation [30]. Next, cells with different distinctive LFN signals are categorized into several groups for analyzing the probable correlations between CF topographies and reset speed. Large variations in the reset speed from device-to-device are addressed by a newly proposed trimming operation for tightening the distribution. Finally, the progress of CF during repeated set/reset cycles are investigated, giving insights into the failure modes during cycling and methods to improve cells' endurance levels.

II. DEVICE STRUCTURE

High density contact resistive random access memory (CRRAM) arrays with full-compatibility to CMOS logic processes successfully fabricated by high-k metal gate technologies was reported [33]. In sizable arrays, these cells subject to limitations on etching control, therefore, are showing large variation on TMO film thickness and quality [34], [35]. A new backfilled resistive random access memory (BCRRAM) cell was proposed to enhance TMO thickness control. Its added processing step to standard CMOS logic process platform is outlined in Figure 1(a). [36], [37] As illustrated, after transistor fabrication and resist protection oxide (RPO) layer deposition, inter layer dielectric (ILD) deposition and contact hole etching steps follow subsequently. Instead of keeping a remaining oxide layer in CRRAM process, complete removal of RPO film is expected on the specifically defined regions for BCRRAMs. Next, SiO_2 film is backfilled into contact holes by PECVD. After removal of the backfilled oxide on regular contacts, barrier layer, TiN, and tungsten plug are formed following standard contact processing steps. The cross-sectional TEM image with resolution 0.2 nm and energy dispersive X-ray (EDX) based composition maps with resolution 2 nm of BCRRAM in Figure 1(b) are carried out by JEOL JEM-2800 transmission electron microscopic with energy 200 keV. As can be seen, EDX

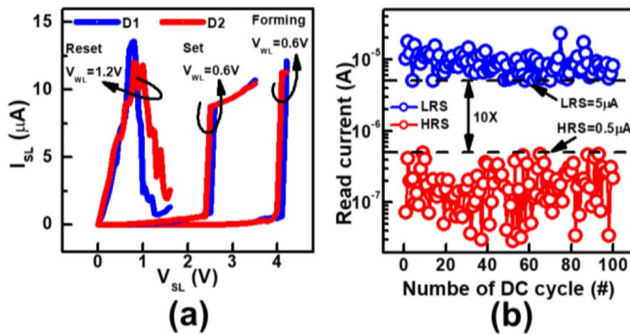

FIGURE 2. (a) DC characteristics of forming/set/reset operations of 2 BCRRAM memory devices. (b) 10 × stable read current window by DC set/reset sweeps under read conditions of $V_{BL} = 0.5$ V and $V_{WL} = 0.8$ V.

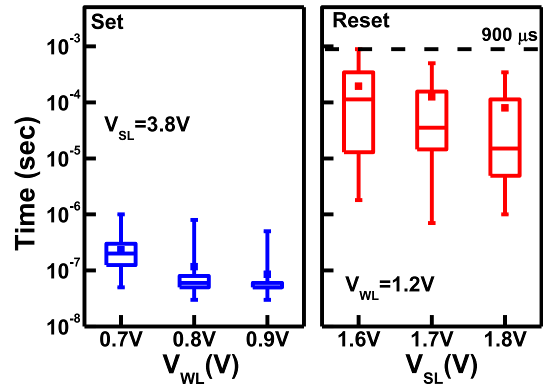

FIGURE 3. Distribution of set/reset time under different bias conditions for cells in an array. Shorter and tighter set time is achievable while larger device-to-device variation is found in its reset time, suggesting that the resistance states dominate the resistance switching time.

TABLE 1. Operation conditions of forming/set/reset/LFN analysis of unipolar BCRRAM devices.

Operation	V_{WL}	V_{SL}	V_{BL}	$V_{P\text{-}sub}$	Rate
Forming	0.6 V	4.2 V	0 V	0 V	--
Set	0.6 V	3.8 V	0 V	0 V	--
Reset	1.2 V	1.6V	0V	0V	--
Read	0.8 V	0 V	0.5 V	0V	--
Current sampling	0.8V	0.2V	0V	0V	200Hz

analysis demonstrates that 5 nm TiN barrier layer and 5 nm SiO_2 dielectric film consist of a 10 nm TMO layer in the TiN/TiON/SiO_2 stacks, sandwiched between a tungsten electrode and the silicon diffusion region.

After physical analysis, electrical characterization, including DC sweeps, current sampling tests and set/reset by AC pulsing, are completed on a probe station through a semiconductor parameter analyzer and a pulse generator. With precise control of the backfilled process, see Figure 1(c), low initial current less than 1 nA under read conditions, arranged in Table 1, across a 256-bit array can be achieved. The DC sweep characteristics of forming/set/reset operation with conditions, outlined in Table 1, are depicted in Figure 2(a). n^+ silicon serves as the bottom electrode with resistivity of 0.1(Ω-cm). BCRRAM is an unipolar device, which high and low resistance state are set to 1 MΩ and 100 KΩ, respectively. During LFN measurement, the bias conditions is $V_{SL} = 0.2$ V, $V_{WL} = 0.8$ V at a 200 Hz sample rate. The common p-type Si substrate for all the devices is electrical grounded during all operations. In forming operation, lower voltage 0.6 V is applied on word line (WL) to pass 0 V of bit line (BL) to n^+ diffusion region below storage node. When resistance switching triggered by high source line (SL) voltage, current level is limited by the select transistor in series. BCRRAM cells can repeatedly switch between low resistance states (LRS) and high resistance states (HRS) for 100 times by applying set/reset voltage to control the generation/rupture of CFs, as shown in Figure 2(b).

III. RESET SPEED VARIATION IN BCRRAM ARRAY

To ensure stable switching between LRS/HRS, a high forming voltage for creating conductive paths in TMO layer is required. Meanwhile, high forming voltage is found to cause larger variations on the resistive states [38]. The impact of strong forming stress on cells requires careful investigation to best optimize the operation procedures for a cell array. Switching speed is one of the key performance aspects in embedded memory applications. Time to set/reset are obtained by adding the overall pulses that a device experienced before a switch between states occurs, where the pulse width incrementally increases from 30 ns to 100 μs. Figure 3 comparing the distributions of the set/reset speed from cells in an array, reveals shorter and tighter set time, on the other hand, slower and wider reset-time spread, while SL voltage shows little effect. Cells require exceptionally long reset can be problematic in embedded memory application which favor fast random access write and low power operation. In this study, we aim at finding the physical causes for these slow cells and come up with methods to improve their speed.

As mentioned, LFNs/RTNs are helpful techniques indicating the state of Vo and CF in a TMO layer. The causes of LFNs are different in LRS from that in HRS. In LRS, LFN signals are generally attributed to electron trapping/detrapping at a defect close to the main CF. The trapped electron create a shielding region along the conductive path, leading to a small decrease in its read current [30], [39]. In HRS, the LFN signal is governed by one or a few electrons captured by Vo in the tunneling path, resulting in the fluctuations on its trap-assisted tunneling current [40]–[42]. Here, to clarify the variation source in reset operations, LFN signals after forming operation and its corresponding trend of power spectrums are compared in a series of plots in Figure 4.

Measured LFNs in Figure 4(a) and the respective noise spectrums in Figure 4(b) reveal that types of LFN can be roughly categorized into Type A/Type B/Type C. As depicted in Figure 5, devices in Type A with single trap near the one dominant CF exhibit bi-level current fluctuations in Figure 4(a) and two discrete current populations in Figure 4(c), showing slope ~ -2 in its power

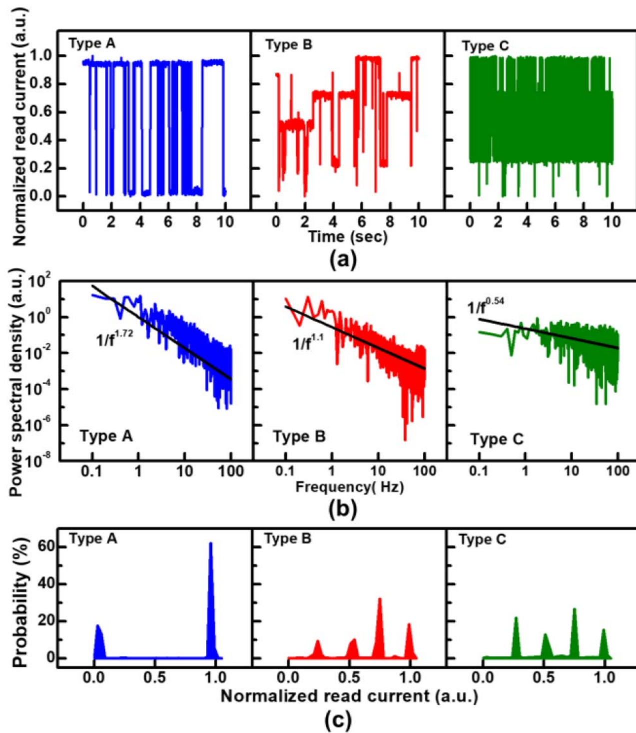

FIGURE 4. Different LFN signals found in BCRRAM cells after forming operation. (a) Read current of samples showing different kinds of LFN signals and the corresponding (b) noise spectrums of the three type of cells. (c) 2^N current states found in three types of LFNs.

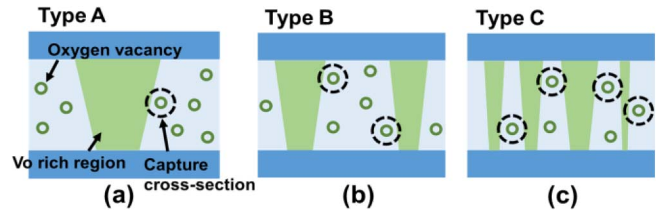

FIGURE 5. Illustrations of the filaments and trap states in the TMO layer of the cells in (a) Type A (b) Type B (c) Type C.

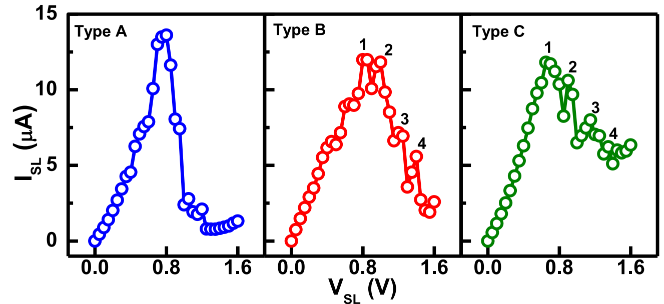

FIGURE 6. Observation of DC sweep characteristics of 30 BCRRAM devices. Sharp current drop probably found in Type A with one dominant CF, but slowly reset transitions in Type B/Type C are attributed to multiple CFs elimination process in DC reset sweeping.

TABLE 2. Types of devices are systematically classified by slopes in its noise spectrum to correlate to their CF status.

LFN type	$1/f^{\alpha}$
Type A	$\alpha > 1.5$
Type B	$1.1 > \alpha > 0.8$
Type C	$0.6 > \alpha > 0.3$

spectrum [43]–[45]. The same sample also shows sudden reset current transition in Figure 6 [46]–[48]. Type B devices with conductive paths affected by the multiple trapping/de-trapping processes, hence, multiple current populations in Figure 4(c), which also corresponds to a noise power spectrum's slope of -1 [43]–[45]. Fast and anomalous switch between current states have been investigated in previous studies. Puglisi *et al.* claim that existence of metastable states of Vo contribute to anomalous random telegraph noise (A-RTN) [49]. A-RTN found in their study is constituted by fast and slow RTN. More distinct current levels are obtained rather than a generally superposition of two-level fluctuations. On the other hand, A-RTN with dynamic time constant result from 2 stables state and 2 metastable states was found by Guo *et al.*[50]. Anomalous current fluctuations are believed to result from multiple traps [49]–[51]. However, no switch in time constants and 2^N current states of Type C, shown in Figure 4(a) and (c), contradict with findings in presented studies. Data in Figure 6 show that gradual reset transitions in Type B and Type C can be fully explained by existence of multiple CFs instead of multiple traps [46]–[48]. Type C cell is believed that includes multiple CFs with interactive processes between the trap states, where Vo can capture/emission electron from/to more than one conductive path, leading to irregular LFNs.

Decreasing trends in noise spectrum are attribute to larger number of CFs, which has been reported in previous studies [43]. Noise spectrum has been used as an indicator for the shapes and forms of CFs and traps in a TMO layer [43], [44]. Further discussion of types of samples, devices are categorized into three groups by its corresponding LF noise spectrums, as outlined in Table 2.

To further confirm the correlation between cells with types of LFNs and its CF topographies, a Monte Carlo simulation for describing random trapping/de-trapping processes is constructed, as explained by the flow chart in Figure 7(a) [30]. The corresponding parameters used in the simulation are listed in Table 3. As illustrated in Figure 7(b), shapes of CF and Vo in this model are approximated as cuboid in this simulation, but electron capture cross-sections of traps are set to be circles with radius of Debye lengths. See in Figure 7(b), given a device area of 50×50 nm^2, different size and numbers of CFs in parallel are first distributed by fitting the measured I-V characteristics from BCRRAM cells. Subsequently, oxygen vacancies with energies and screening length of capture cross-section within a given range -0.2 eV to 0.2 eV and 5 nm to 10 nm, [29], [52] are placed randomly within the region of interest. Once the main parameters for CFs and Vo are defined, the probabilities of trapped/detrapped are determined by Eq. (1) to Eq. (3) [30], [53]. Here, carrier concentration in each CFs, n,

TABLE 3. Corresponding physical parameters of low frequency noise model and joule heating simulation.

Parameter	Name	Value
l_{CF}	Length of CF	2~14(nm) [26]
t_{CF}	Thickness of TMO layer	20 (nm)
τ_c	Capture time	--
τ_e	Emission time	--
Pc	Electron trapping probability	--
Pe	Electron detrapping probability	--
N_{CF}	Number of CFs	--
σ	Capture cross-section	5~10(nm) [52]
E_T	Trap energy	--
E_F	Fermi energy level	--
E_F-E_T	Energy difference	0.2~-0.2(eV) [29]
N_R	Random number	--
λ_S	Screen length	3 (nm) [42]
d	Distance between Vo and CF	--
g	Degeneracy factor	--
n	Carrier concentration in CF	--
v_{th}	Thermal velocity	--
k_B	Boltzmann constant	8.6×10^{-5} (eV/K)
ρ_{CF}	Resistivity of CF	8×10^{-4} (Ωm)
ρ_{ox}	Resistivity of oxide	10^{15} (Ωm) [54]
k	Thermal conductivity	1.4 (W/mK) [55]

and thermal velocity, v_{th}, and degeneracy factor, g, are assumed to be constants. As shown in Equation (1), (2) and Figure 7(b), Vo can capture/emission electron from/to more than one CF. Cells with several closely placed CFs may experience interferences between them during these random trapping events, leading to higher capture/emission probabilities. If portion of CF is shielded, see in Figure 7(c), an increase in resistance can be described in Eq. (4) [42].

$$P_c = \frac{1}{\tau_c} = N_{CF} n v_{th} \sigma \quad (1)$$

$$P_e = \frac{1}{\tau_e} = \frac{g N_{CF} n v_{th} \sigma}{\exp\left[(E_F - E_T)/k_B T\right]} \quad (2)$$

$$\begin{cases} P_c > N_R & \text{(electron trapping)} \\ P_e > N_R & \text{(electron detrapping)} \end{cases} \quad (3)$$

$$R = \frac{\rho_{CF}(t_{CF} - \lambda_S)}{l_{CF}^2} + \frac{\rho_{CF}\lambda_S}{l_{CF}^2 - (\lambda_S - d)^2} \quad (4)$$

Finally, total resistance levels of 2000 sampling time points can be obtained by putting CFs in parallel. As compared in Figure 8(a), measured LFNs can be predicted by simulation results with good agreements on different types of cells. Correlation between number of CFs inside the RRAM regions and types of LFN signals can be further revealed by the simulated results summarized in Figure 9. Among cells with single CF, higher portion of them will exhibit Type A. On the other hand, a larger fraction of cells with more CFs placed in TMO layer showing Type C characteristic.

With the linkage between types of LFN noises and number of conductive paths, we try to correlate the reset efficiency of BCRRAM cells to its LFN signals and further down to its CF topographies. Figure 10(a) shows that cells exhibiting Type A leads to faster reset, resulting from single conductive path. While longer reset time is found in BCRRAM

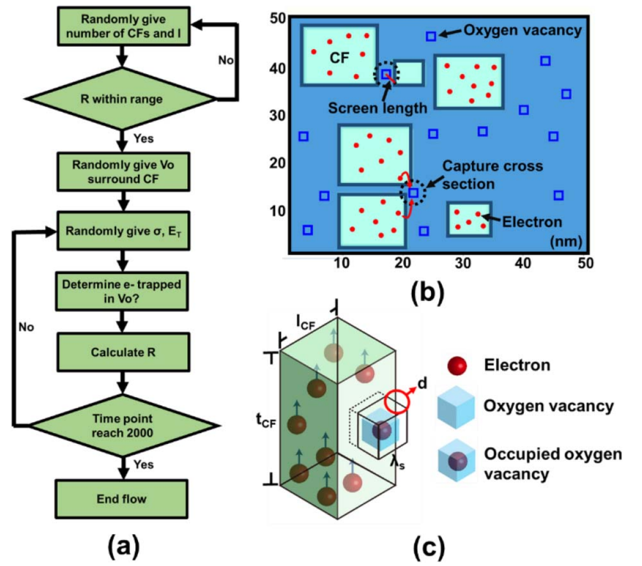

FIGURE 7. **(a) Simulation flow of effect of trapping/detrapping behavior in TMO layer, by putting density and size of filaments as variables to meet measured resistance within range 33KΩ to 100KΩ. (b) Illustrations of trapping/detrapping process. Oxygen vacancy can capture/emission electron from/to more than one CFs within its capture cross-section. (c) Oxygen vacancies occupied by electrons screen out part of CF, resulting in an increase in its resistance.**

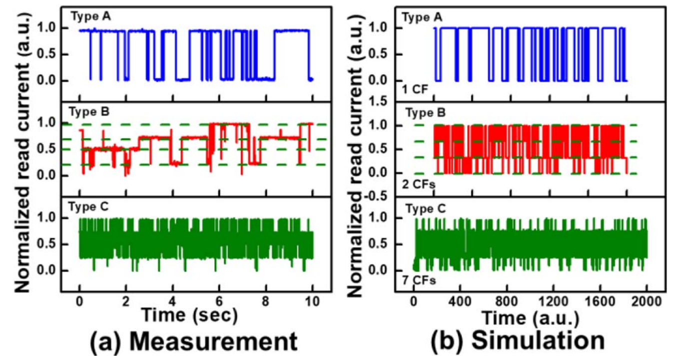

FIGURE 8. **(a) Measured and (b)simulated read current fluctuations in three different types of cells. Different LFN signals can be predicted by changes the density of CFs in TMO layer, affecting both the number of current levels in the LFNs and capture and emission times.**

cells with Type C, which may be caused by the tiny CFs in TMO layer. It is believed that the reset process in an unipolar RRAM device is triggered by high localized heating inside conductive paths. The temperature profiles of TMO layers with different CF densities are compared in Figure 10(b) [56], [57]. Cells with single dominant CF leads to higher localized temperature, hence, enabling more efficient reset. On the contrary, less focus heating during reset process in structures with multiple CFs, is expect to cause slow reset in cells with either Type B and Type C.

IV. RESET TRIMMING SCHEME

Based on previous discussion, unnecessary CFs in BCRRAM cells generated during stochastic forming/set process must

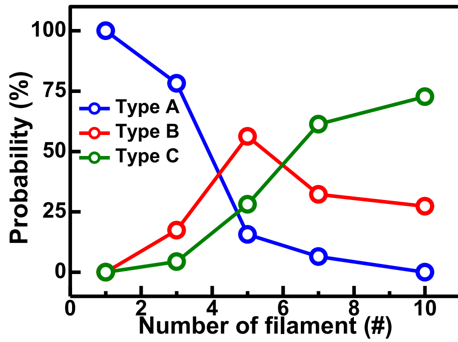

FIGURE 9. Correlation between the number of CFs within 50×50 nm^2, used in the simulations, and the probability of its cell type.

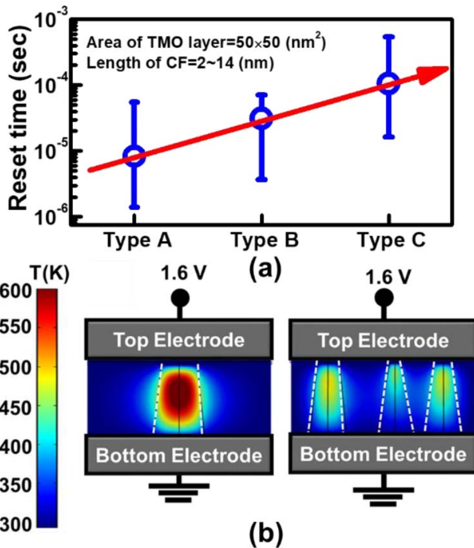

FIGURE 10. (a) Reset time of cells categorized by its LFN signals. (b) Internal temperature profiles of one dominant CF and multiple conductive paths, where location of CFs are labelled by the white dash lines.

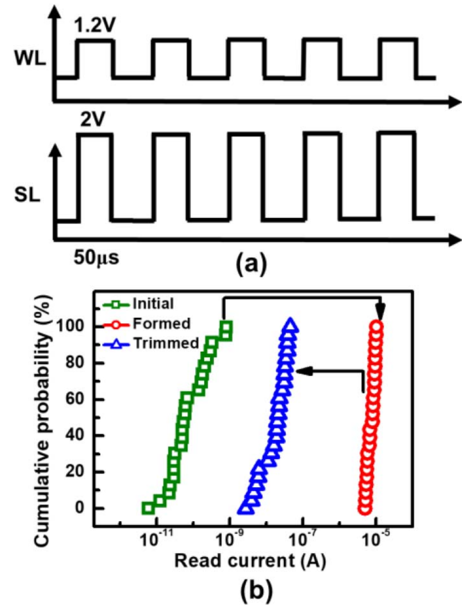

FIGURE 11. (a) Timing and conditions of the trimming process for minimizing unnecessary CF is completed by applying a few short reset pulses at a slightly higher SL voltage. (b) Read current distribution of cells at initial, after forming and trimming, respectively.

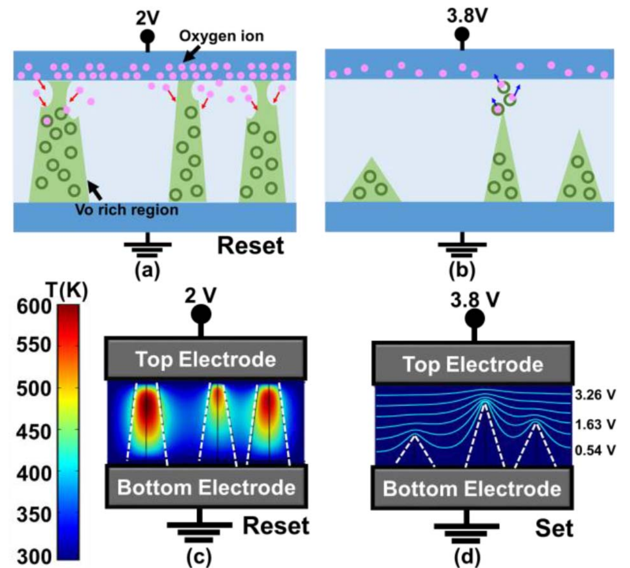

FIGURE 12. (a) Schematic of conductive paths under (a) reset trimming operation and (b) set operation. (c) Simulated internal temperature under 2 V reset trimming voltage. (d) Local enhanced electric field at shortest gap between top electrode and CF for controlling CF generations.

be reduced for improving reset speed. In presented studies [58]–[60], stochastic Vo generation has also been found as a critical problem to reliability and variability. Many studies have shown the control of Vo generation to further obtain single CF for resolving reliability and variability issue. In reference 59, Au-tip is coated on top electrode to concentrated electric field [59]. To confine CF growth, Pt nanocrystal is also embedded with TiO_2 thin film for the same purpose of local enhancement of electric filed [58]. Concentrated electric field at a local region for confining Vo generations can drastically relieved variability problems. Therefore, a new electrical treatment, named as reset trimming operation, proposed in this study is necessary for embedded BCRRAM cells to minimize multiple CFs inside TMO layers. To eliminate redundant CFs, a new reset trimming treatment with conditions, outlined in Figure 11(a), is implemented in pristine cells after forming process to recover them to lower read current levels, as shown in Figure 11(b).

The change of CFs during reset trimming and the following set operation are illustrated in Figure 12(a) and (b), respectively. During trimming reset, the temperature profile derived by joule heating model is shown in Figure 12(c), oxygen ions stored in the top electrode can diffuse back to anneal out a few conductive paths at one time [20], [56], [57]. In the subsequent set operation, based on the reported study in [59], the electric field can be locally enhanced at the narrowest

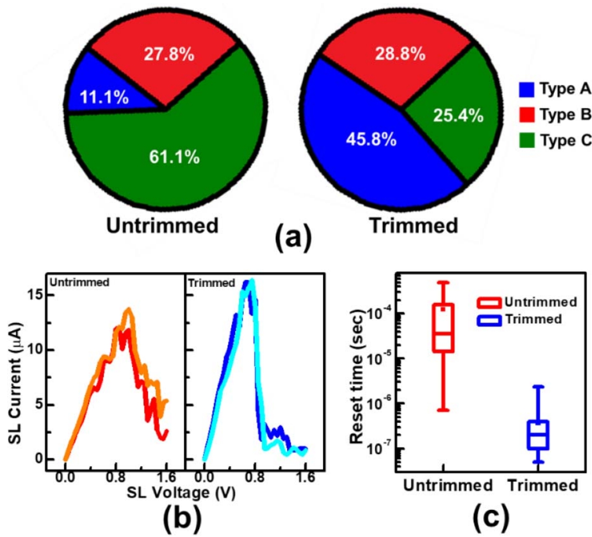

FIGURE 13. **(a) Probability distributions of the three types of cells before and after trimmed process. Higher probability of cells in an array exhibits Type A as a result of reduced unnecessary CFs. (b) Sudden current drops on trimmed cells, while gradual resistance transitions are found on untrimmed cells (c) Comparison of reset time of untrimmed/trimmed cells under $V_{SL} = 1.7V$.**

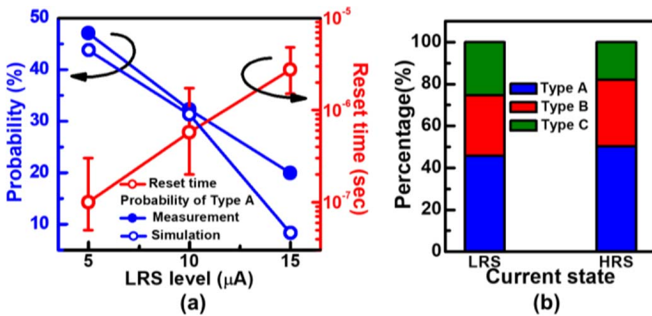

FIGURE 14. **(a) The dependency of measured and simulated LFN signal characteristics of cells and reset efficiency of first cycle on LRS level. Reset efficiency are also found to be inverse proportional to the LRS level. (b) High probability to obtain LFN of Type A in both lower LRS and HRS as a result of fewer conductive paths inside TMO layer.**

gap region, as shown in Figure 12(d), which confines Vo generations at one location, leading to the formation of a single conductive filament.

To investigate effectiveness of the proposed trimming operation, number of cells with different LFNs and reset characteristics before and after such operation are compared in Figure 13(a). As result of reducing redundant CFs inside TMO layer, larger portion of trimmed cells are showing Type A, evidence to less CFs. Besides, as shown in Figure 13(b), sharply current drops during reset process are also obtained in trimmed cells after minimizing redundant tiny paths [46]–[48]. As further demonstrated timing required of first reset operations in Figure 13(c), faster reset speed is obtained after the reset trimming treatment.

In addition to correlate to cells' LFN characteristics, reset operation is found to be closely linked to its LRS resistance

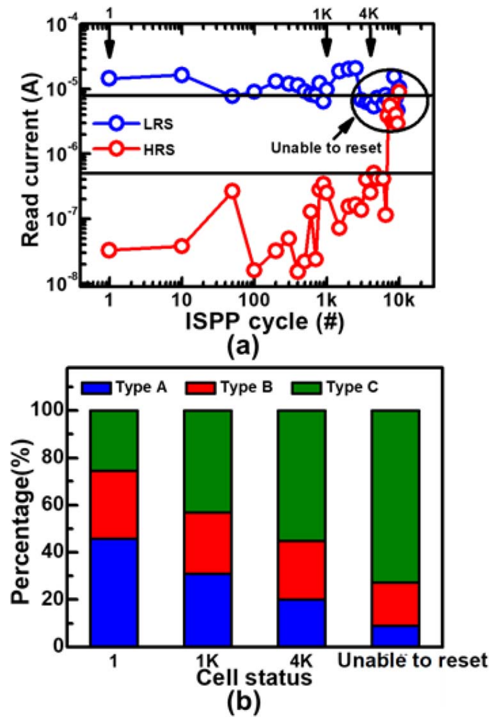

FIGURE 15. **(a) 10K ISPP cycling characteristics of BCRRAM. BCRRAM can keep 10× on/off ratio for 1K cycles, but stuck at LRS after several thousands of cycles. (b) Shift in cells with different LFN signals are found during ISPP cycling tests, which provides a guideline to address endurance failure.**

state. The dependency of portion of type A device and the cell's reset efficiency on LRS level are summarized in Figure 14(a). Reset efficiency are found to be inversely proportional to its LRS level, which further support the conclusions that less numbers of CF improve reset performance. While maintaining the same 10× read ratio, by targeting a low LRS current level, more cells are expected to have only one dominant CF, this can also help promote the reset speed among a group of cells. On the other hand, probabilities of types of LFNs of LRS in 5 μA and HRS 0.5 μA are compared in Figure 14(b). In similar scenario with LRS, devices in HRS with only one trap with shortest distance to electrode have higher probabilities of exhibit Type A LFNs [44].

After obtaining suitable LRS/HRS levels with short pulse, cycling endurance of BCRRAM is examined through an optimized incremental step pulse programming scheme (ISPP) [61]. Cell arrays during cycling test are monitored for investigating the change in the CF topographies. BCRRAM cells can keeps 10× read window for 1K ISPP cycling test, as shown in Fig. 15(a). However, BCRRAM lose their cyclabilities after several thousands of cycles. Data in Figure 15(b), suggests that additional CFs are generated by the set/reset stress, which leads to ultimate reset failure over time and limits its cycling endurance. Endurance of cells, categorized by their types of LFN after trimming, are shown in Figure 16. Keep most of the cells with single main CFs

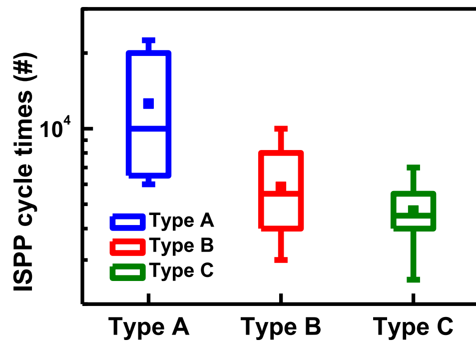

FIGURE 16. Correlation between CF topologies, as categorized by their LFN after trimming, and its maximum cycles are found in a BCRRAM array.

(Type A) during cycling operation can further enhance the overall cyclability of the BCRRAM arrays.

V. CONCLUSION

In this study, cells in a BCRRAM array with large reset efficiency variation are categorized into three groups by its LFN features. These LFN features are found to be directly correlated to the number of CFs in a TMO layer area by Monte Carlo simulation and different kinds of reset characteristics. Cells with slow resets are caused by multiple unnecessary conductive paths generation during forming/set operation, leading to less effective heating of CFs. Here, a trimming operation is proposed for eliminating redundant CFs. Finally, monitoring the stochastic Vo generation during cycling is expected to give raise to new operational schemes in extended cell's cycling lifetime.

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REFERENCES

[1] C. Chou *et al.*, "An N40 256K × 44 embedded RRAM macro with SL-precharge SA and low-voltage current limiter to improve read and write performance," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, 2018, pp. 478–480.

[2] H. W. Pan *et al.*, "1Kbit FinFET dielectric (FIND) RRAM in pure 16nm FinFET CMOS logic process," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Washington, DC, USA, 2015, pp. 1–4.

[3] C. Y. Mei *et al.*, "28-nm 2T high-*K* metal gate embedded RRAM with fully compatible CMOS logic processes," *IEEE Electron Device Lett.*, vol. 34, no. 10, pp. 1253–1255, Oct. 2013.

[4] Y. Huang *et al.*, "A TaOx based threshold switching selector for the RRAM crossbar array memory," in *Proc. 12th Annu. Non Volatile Memory Technol. Symp.*, Singapore, 2012, pp. 85–87.

[5] G. Sassine *et al.*, "Sub-pJ consumption and short latency time in RRAM arrays for high endurance applications," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Burlingame, CA, USA, 2018, pp. P-MY.2-1–P-MY.2-5.

[6] Y. Pan *et al.*, "Material engineering technique for SiOX-based embedded RRAM with CMOS compatible process," in *Proc. 12th Annu. NonVolatile Memory Technol. Symp.*, Singapore, 2012, pp. 91–93.

[7] S. Balatti, S. Ambrogio, D. Ielmini, and D. C. Gilmer, "Variability and failure of set process in HfO2 RRAM," in *Proc. 5th IEEE Int. Memory Workshop*, Monterey, CA, USA, 2013, pp. 38–41.

[8] A. Rubio, M. Escudero, and P. Pouyan, "Reliability issues in RRAM ternary memories affected by variability and aging mechanisms," in *Proc. IEEE 23rd Int. Symp. OnLine Testing Robust Syst. Design (IOLTS)*, Thessaloniki, Greece, 2017, pp. 90–92.

[9] M. B. Gonzalez, J. M. Rafí, O. Beldarrain, M. Zabala, and F. Campabadal, "Analysis of the switching variability in Ni/HfO_2-based RRAM devices," *IEEE Trans. Device Mater. Rel.*, vol. 14, no. 2, pp. 769–771, Jun. 2014.

[10] E. Pérez, A. Grossi, C. Zambelli, P. Olivo, R. Roelofs, and C. Wenger, "Reduction of the cell-to-cell variability in $Hf_{1-x}Al_xO_y$ based RRAM arrays by using program algorithms," *IEEE Electron Device Lett.*, vol. 38, no. 2, pp. 175–178, Feb. 2017.

[11] N. Raghavan, K. L. Pey, W. Liu, X. Wu, X. Li, and M. Bosman, "Evidence for compliance controlled oxygen vacancy and metal filament based resistive switching mechanisms in RRAM," *Microelectron. Eng.*, vol. 88, no. 7, pp. 1124–1128, 2011.

[12] D. Kumar, R. Aluguri, U. Chand, and T. Y. Tseng, "Metal oxide resistive switching memory: Materials, properties and switching mechanisms," *Ceram. Int.*, vol. 43, pp. S547–S556, Aug. 2017.

[13] S. Yu, "Overview of resistive switching memory (RRAM) switching mechanism and device modeling," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Melbourne, VIC, Australia, 2014, pp. 2017–2020.

[14] D. Ielmini, F. Nardi, and C. Cagli, "Universal reset characteristics of unipolar and bipolar metal-oxide RRAM," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3246–3253, Oct. 2011.

[15] Y. S. Zhi *et al.*, "Reversible transition between bipolar and unipolar resistive switching in Cu_2O/Ga_2O_3 binary oxide stacked layer," *AIP Adv.*, vol. 6, no. 1, 2016, Art. no. 015215.

[16] L. Zhu, J. Zhou, Z. Guo, and Z. Sun, "An overview of materials issues in resistive random access memory," *J. Materiomics*, vol. 1, no. 4, pp. 285–295, 2015.

[17] B. Gao *et al.*, "Oxide-based RRAM switching mechanism: A new ion-transport-recombination model," in *Proc. IEEE Int. Electron Devices Meeting*, San Francisco, CA, USA, 2008, pp. 1–4.

[18] F. Nardi, S. Larentis, S. Balatti, D. C. Gilmer, and D. Ielmini, "Resistive switching by voltage-driven ion migration in bipolar RRAM—Part I: Experimental study," *IEEE Trans. Electron Devices*, vol. 59, no. 9, pp. 2461–2467, Sep. 2012.

[19] S. Yu, Y. Wu, and H. S. P. Wong, "Investigating the switching dynamics and multilevel capability of bipolar metal oxide resistive switching memory," *Appl. Phys. Lett.*, vol. 98, no. 10, 2011, Art. no. 103514.

[20] S. Yu and H. P. Wong, "A phenomenological model for the reset mechanism of metal oxide RRAM," *IEEE Electron Device Lett.*, vol. 31, no. 12, pp. 1455–1457, Dec. 2010.

[21] M.-J. Lee *et al.*, "Electrical manipulation of nanofilaments in transition-metal oxides for resistance-based memory," *Nano Lett.*, vol. 9, no. 4, pp. 1476–1481, 2009.

[22] S. Balatti, S. Ambrogio, D. C. Gilmer, and D. Ielmini, "Set variability and failure induced by complementary switching in bipolar RRAM," *IEEE Electron Device Lett.*, vol. 34, no. 7, pp. 861–863, Jul. 2013.

[23] X. Guan, S. Yu, and H. P. Wong, "On the switching parameter variation of metal-oxide RRAM—Part I: Physical modeling and simulation methodology," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 1172–1182, Apr. 2012.

[24] A. Chen and M. Lin, "Variability of resistive switching memories and its impact on crossbar array performance," in *Proc. Int. Rel. Phys. Symp.*, Monterey, CA, USA, 2011, pp. MY.7.1–MY.7.4.

[25] Y. Yang and W. Lu, "Nanoscale resistive switching devices: Mechanisms and modeling," *Nanoscale*, vol. 5, no. 21, pp. 10076–10092, 2013, doi: 10.1039/C3NR03472K.

[26] K. L. Pey, R. Thamankar, M. Sen, M. Bosman, N. Raghavan, and K. Shubhakar, "Understanding the switching mechanism in RRAM using in-situ TEM," in *Proc. IEEE Silicon Nanoelectron. Workshop (SNW)*, Honolulu, HI, USA, 2016, pp. 36–37.

[27] G. Bersuker *et al.*, "Metal oxide RRAM switching mechanism based on conductive filament microscopic properties," in *Proc. Int. Electron Devices Meeting*, San Francisco, CA, USA, 2010, pp. 1–4.

[28] G. Niu *et al.*, "Geometric conductive filament confinement by nanotips for resistive switching of HfO_2-RRAM devices with high performance," *Sci. Rep.*, vol. 6, May 2016, Art. no. 25757.

[29] Z. Chai *et al.*, "RTN-based defect tracking technique: Experimentally probing the spatial and energy profile of the critical filament region and its correlation with HfO2RRAM switching operation and failure mechanism," in *Proc. IEEE Symp. VLSI Technol.*, Honolulu, HI, USA, 2016, pp. 1–2.

[30] S. Ambrogio, S. Balatti, A. Cubeta, A. Calderoni, N. Ramaswamy, and D. Ielmini, "Statistical fluctuations in HfO_x resistive-switching memory: Part II—Random telegraph noise," *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2920–2927, Aug. 2014.
[31] H. Shin and O. Byoungchan, "Characterization of oxide traps by RTN measurement in MOSFETs and memory devices," in *Proc. 17th IEEE Int. Symp. Phys. Fail. Anal. Integr. Circuits*, Singapore, 2010, pp. 1–5.
[32] E. R. Hsieh *et al.*, "The RTN measurement technique on leakage path finding in advanced high-k metal gate CMOS devices," in *Proc. IEEE 22nd Int. Symp. Phys. Fail. Anal. Integr. Circuits*, Hsinchu, Taiwan, 2015, pp. 154–457.
[33] W. C. Shen *et al.*, "High-K metal gate contact RRAM (CRRAM) in pure 28nm CMOS logic process," in *Proc. Int. Electron Devices Meeting*, San Francisco, CA, USA, 2012, pp. 1–4.
[34] Y.-F. Kao, W. C. Zhuang, C.-J. Lin, and Y.-C. King, "A study of the variability in contact resistive random access memory by stochastic vacancy model," *Nanoscale Res. Lett.*, vol. 13, no. 1, p. 213, 2018.
[35] Y. F. Kao, W. T. Hsieh, C. C. Chen, Y.-C. King, and C. J. Lin, "Statistical analysis of the correlations between cell performance and its initial states in contact resistive random access memory cells," *Jpn. J. Appl. Phys.*, vol. 56, no. 4S, 2017, Art. no. 04CE08.
[36] H. Chen, H. Chen, Y. Kao, P. Chen, Y. King, and C. J. Lin, "A new manufacturing method of CMOS logic compatible 1T-CRRAM," in *Proc. Int. Symp. VLSI Technol. Syst. Appl. (VLSI-TSA)*, Hsinchu, Taiwan, 2016, pp. 1–2.
[37] H. Chen, H. H. Chen, Y. King, and C. J. Lin, "Investigation of set/reset operations in CMOS-logic-compatible contact backfilled RRAMs," *IEEE Trans. Device Mater. Rel.*, vol. 16, no. 3, pp. 370–375, Sep. 2016.
[38] B. Butcher *et al.*, "Hot forming to improve memory window and uniformity of low-power HfOx-based RRAMs," in *Proc. 4th IEEE Int. Memory Workshop*, Milan, Italy, 2012, pp. 1–4.
[39] C. Wang, H. Wu, B. Gao, T. Zhang, Y. Yang, and H. Qian, "Conduction mechanisms, dynamics and stability in ReRAMs," *Microelectron. Eng.*, vols. 187–188, pp. 121–133, Feb. 2018.
[40] F. M. Puglisi and P. Pavan, "An investigation on the role of current compliance in HfO2-based RRAM in HRS using RTN and I-V data," in *Proc. 15th Int. Conf. Ultimate Integr. Silicon (ULIS)*, Stockholm, Sweden, 2014, pp. 129–132.
[41] D. Dong *et al.*, "The impact of RTN signal on array level resistance fluctuation of resistive random access memory," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 676–679, May 2018.
[42] F. M. Puglisi, N. Zagni, L. Larcher, and P. Pavan, "Random telegraph noise in resistive random access memories: Compact modeling and advanced circuit design," *IEEE Trans. Electron Devices*, vol. 65, no. 7, pp. 2964–2972, Jul. 2018.
[43] W. Feng, H. Shima, K. Ohmori, and H. Akinaga, "Investigation of switching mechanism in HfOx-ReRAM under low power and conventional operation modes," *Sci. Rep.*, vol. 6, Dec. 2016, Art. no. 39510.
[44] S. Yu, R. Jeyasingh, W. Yi, and H. P. Wong, "Understanding the conduction and switching mechanism of metal oxide RRAM through low frequency noise and AC conductance measurement and analysis," in *Proc. Int. Electron Devices Meeting*, Washington, DC, USA, 2011, pp. 1–4.
[45] Y. H. Tseng, S. Wen Chao, H. Chia-En, L. Chrong Jung, and K. Ya-Chin, "Electron trapping effect on the switching behavior of contact RRAM devices through random telegraph noise analysis," in *Proc. Int. Electron Devices Meeting*, San Francisco, CA, USA, 2010, pp. 1–4.
[46] B. Gao *et al.*, "Identification and application of current compliance failure phenomenon in RRAM device," in *Proc. Int. Symp. VLSI Technol. Syst. Appl.*, Hsinchu, Taiwan, 2010, pp. 144–145.
[47] B. Gao *et al.*, "Unified physical model of bipolar oxide-based resistive switching memory," *IEEE Electron Device Lett.*, vol. 30, no. 12, pp. 1326–1328, Dec. 2009.
[48] P. R. Mickel, A. J. Lohn, and M. J. Marinella, "Detection and characterization of multi-filament evolution during resistive switching," *Appl. Phys. Lett.*, vol. 105, no. 5, 2014, Art. no. 053503.
[49] F. M. Puglisi, L. Larcher, A. Padovani, and P. Pavan, "Anomalous random telegraph noise and temporary phenomena in resistive random access memory," *Solid-State Electron.*, vol. 125, pp. 204–213, Nov. 2016.
[50] S. Guo, R. Wang, D. Mao, Y. Wang, and R. Huang, "Anomalous random telegraph noise in nanoscale transistors as direct evidence of two metastable states of oxide traps," *Sci. Rep.*, vol. 7, no. 1, p. 6239, 2017.
[51] R. Thamankar *et al.*, "Single vacancy defect spectroscopy on HfO2 using random telegraph noise signals from scanning tunneling microscopy," *J. Appl. Phys.*, vol. 119, no. 8, 2016, Art. no. 084304.
[52] J. T. Ryan, A. Matsuda, J. P. Campbell, and K. P. Cheung, "Interface-state capture cross section—Why does it vary so much?" *Appl. Phys. Lett.*, vol. 106, no. 16, 2015, Art. no. 163503.
[53] S. S. Chung and C. M. Chang, "The investigation of capture/emission mechanism in high-*k* gate dielectric soft breakdown by gate current random telegraph noise approach," *Appl. Phys. Lett.*, vol. 93, no. 21, 2008, Art. no. 213502.
[54] R. Chaudhary, R. Mukhiya, G. S. Patel, P. R. Mudimela, and R. Sharma, "Simulation of MOSFET with different dielectric films," in *Proc. Int. Conf. Intell. Circuits Syst. (ICICS)*, Phagwara, India, 2018, pp. 173–176.
[55] M. B. Kleiner, S. A. Kuhn, and W. Weber, "Thermal conductivity measurements of thin silicon dioxide films in integrated circuits," *IEEE Trans. Electron Devices*, vol. 43, no. 9, pp. 1602–1609, Sep. 1996.
[56] U. Russo, D. Ielmini, C. Cagli, and A. L. Lacaita, "Self-accelerated thermal dissolution model for reset programming in unipolar resistive-switching memory (RRAM) devices," *IEEE Trans. Electron Devices*, vol. 56, no. 2, pp. 193–200, Feb. 2009.
[57] U. Russo *et al.*, "Conductive-filament switching analysis and self-accelerated thermal dissolution model for reset in NiO-based RRAM," in *Proc. IEEE Int. Electron Devices Meeting*, Washington, DC, USA, 2007, pp. 775–778.
[58] W.-Y. Chang *et al.*, "Improvement of resistive switching characteristics in TiO_2 thin films with embedded Pt nanocrystals," *Appl. Phys. Lett.*, vol. 95, no. 4, 2009, Art. no. 042104.
[59] V. R. Nallagatla, J. Jo, S. K. Acharya, M. Kim, and C. U. Jung, "Confining vertical conducting filament for reliable resistive switching by using a Au-probe tip as the top electrode for epitaxial brownmillerite oxide memristive device," *Sci. Rep.*, vol. 9, no. 1, p. 1188, 2019.
[60] A. Prakash, J. Park, J. Song, J. Woo, E. Cha, and H. Hwang, "Demonstration of low power 3-bit multilevel cell characteristics in a TaO_x-based RRAM by stack engineering," *IEEE Electron Device Lett.*, vol. 36, no. 1, pp. 32–34, Jan. 2015.
[61] Y. Kao, C. J. Lin, and Y. King, "Stochastic filament formation on the cycling endurance of backfilled contact resistive random access memory cells," in *Proc. Int. Symp. VLSI Technol. Syst. Appl. (VLSI-TSA)*, Hsinchu, Taiwan, 2019, pp. 1–2.