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High $f_{max} \times L_G$ Product of AlGaN/GaN HEMTs on Silicon With Thick Rectangular Gate

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ABSTRACT In this letter, we successfully demonstrated a AlGaN/GaN high-electron mobility transistor on silicon substrate with high product of maximum oscillation frequency (f_{max}) and gate length (L_G) by reducing the gate resistance (R_g) using a thick, high aspect ratio rectangular gate (R-gate) structure with an L_G of 265 nm and thickness of 315 nm which was fabricated using a thick polymethyl methacrylate lift-off process. The maximum drain current is over 1 A/mm, and the peak transconductance is 291 mS/mm. The values of cutoff frequency and f_{max} are 43.7 GHz and 126.5 GHz at a drain voltage (V_d) of 12 V, respectively. R_g is extracted through the small-signal model, and the value is given as 0.21 Ω-mm which is comparable to devices with the T-gate structure. This low R_g results in a high f_{max} and high $f_{max} \times L_G$ product of 33.52 GHz-μm, comparable to previously reported GaN-on-Si transistors for both R-gate and T-gate structures.

INDEX TERMS AlGaN/GaN, high-electron mobility transistor (HEMT), silicon substrate, power-gain cutoff frequency (f_{max}), rectangular gate, $f_{max} \times L_G$.

I. INTRODUCTION

In order to meet the rapidly growing demand for 5th generation communication systems, high performance solid-state power amplifiers (SSPA) are desperately needed. GaN-based high-electron-mobility transistors (HEMT) have high electron saturation velocity, high sheet carrier density, and high breakdown voltage which allow for wide bandwidth and high power operation. In the last decade, the GaN-on-SiC system has achieved remarkable benchmarks such as a record high cutoff frequency (f_T) and a maximum oscillation frequency (f_{max}) of 454 GHz and 455 GHz [1], respectively. These characteristics make GaN HEMTs suitable for use in monolithic microwave integrated circuit (MMIC) applications. However, the development of commercial GaN-on-SiC products is hindered by the high cost of SiC substrates which currently only have a maximum diameter of 6 inches. Therefore, GaN on high resistivity silicon substrates promise an alternative solution for low-cost and large-scale production.

Significant efforts have been made to improve the epitaxial quality of GaN-on-Si, and successful applications such as power switches have been demonstrated in recent years [2]–[4]. However, the development of radio frequency (RF) GaN HEMTs on Si substrates still lags behind the GaN-on-SiC system. The best reported f_T and f_{max} for GaN HEMTs on Si substrates is 250 GHz and 226 GHz, respectively [5], [6].

The physical meaning of f_{max} is the highest frequency at which the device can be regarded as an active device. Therefore, f_{max} is a critical factor for determining the possible operation frequency for SSPA applications. The equation for f_{max} is given as follows:

$$f_{max} = \frac{1}{2} \frac{f_T}{\sqrt{2\pi \cdot f_T \cdot C_{gd}\left(R_g + R_s\right) + \frac{R_g + R_s}{R_{ds}}}} \tag{1}$$

where C_{gd} is gate-to-drain capacitance, R_g is gate resistance, R_s is gate-to-source access resistance, and R_{ds} is

drain-to-source resistance [7]. In order to enhance f_{max}, reducing R_g is one of the solutions according to Eq. (1). The T-gate and Gamma-gate structure were developed to meet the demand for obtaining better current density, linearity, and RF characteristics such as f_{max} by means of reducing R_g. However, the complex fabrication process, lower yield rate, and higher cost of T-gate devices motivate us to find another way of reducing R_g. In this letter, we have demonstrated an AlGaN/GaN-on-Si HEMT which is characterized by a robust, high aspect ratio rectangular gate (R-gate) structure with 265 nm gate length (L_G) and 315 nm thickness. Using this structure, a low R_g of 0.21 Ω-mm can be realized. Based on this result, a high $f_{max} \times L_G$ product can be obtained comparable to GaN-on-Si devices with a T-gate structure.

II. DEVICE FABRICATION

Figure 1(a) exhibits the fabrication process and layer structure of the AlGaN/GaN HEMTs. The epilayers of the AlGaN/GaN heterostructure were grown on a high resistivity (>6 kW-cm) silicon (111) substrate by metal-organic chemical vapor deposition. The heterostructure consists of a 2.5 nm GaN cap layer, a 20 nm $Al_{0.25}Ga_{0.75}N$ barrier layer, a thin AlN interlayer of 1 nm to enhance the carrier mobility [8], a 300 nm unintentionally doped GaN channel layer, and a ~2 mm buffer layer. Hall measurements indicate that the heterostructure has a sheet carrier concentration of 10^{13} cm^{-2} with an electron mobility of 2000 cm^2/Vs and a sheet resistance of 280 W/sq. Device fabrication begins with source and drain Ohmic metallization which is formed by Ti/Al/Ni/Au deposition followed by rapid thermal annealing at 875 °C for 40 s in N_2. A contact resistance of 0.79 Ω-mm was confirmed by transmission line measurements. After the Ohmic metallization, the mesa isolation was implemented by Cl_2/BCl_3 mixed plasma etching. Next, gates were defined by electron-beam lithography using a thick polymethyl methacrylate photoresist. In order to reduce R_g, a thick gate stack (Ni 15 nm/Au 300 nm) was deposited to form a high aspect R-gate structure. Ti/Au contact pads were deposited to increase the contact area. Finally, a standard back-end process was used with deposition of 200 nm SiN film with a dielectric constant of 7.0 and planarization of 900 nm polyimide with a dielectric constant of 3.4 to further reduce the capacitance. After etching some via holes on the source/drain/gate, we deposited a thick Au pad about 1200 nm thick with a common source GSG probing layout for RF measurements. The thickness is designed to resist puncture from the GSG probe and to also be thicker than the depth of the via holes, which are about 1100 nm deep which includes the 200 nm SiN and 900 nm polyimide layers to be etched. The device is characterized with 265 nm L_G and (2 × 10) μm gate width. The source-to-drain distance is 1.86 μm for each device. The L_G and thickness were measured by scanning electron microscopy as shown in Figure 1(b).

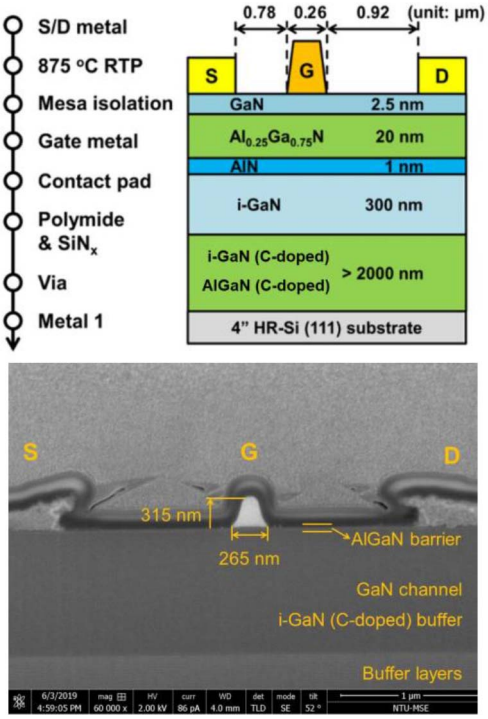

FIGURE 1. (a) The fabrication process and schematic layer structure of the AlGaN/GaN-on-Si HEMT with 265 nm R-gate structure. (b) The scanning electron microscopy (SEM) image of the rectangular gates.

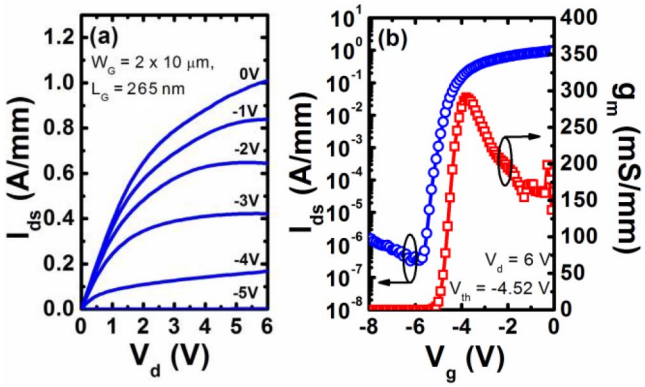

FIGURE 2. Common source DC (a) output characteristics and (b) transfer characteristics of the 265 nm L_G GaN HEMT with 2x10 mm gate width.

III. RESULTS AND DISCUSSION

Figure 2(a) shows the output characteristics of the AlGaN/GaN HEMT. The maximum drain current (I_{ds}) of 1.01A/mm is obtained at $V_g = 0$ V and $V_d = 6$ V, and the ON-resistance (R_{ON}) is 2.45 Ω-mm. These exceptional ON-state characteristics are attributed to the relatively low sheet resistance which leads to a low knee voltage of less than 2 V. Figure 2(b) shows the transfer characteristics with a peak DC transconductance (g_m) of 291 mS/mm at $V_d = 6$ V. The threshold voltage (V_{th}) is −4.52V as extracted by linear extrapolation. The subthreshold swing (SS) of the device is 199 mV/dec, and the ON/OFF ratio is about ~10^6 where the OFF-state current is predominately gate leakage current. This

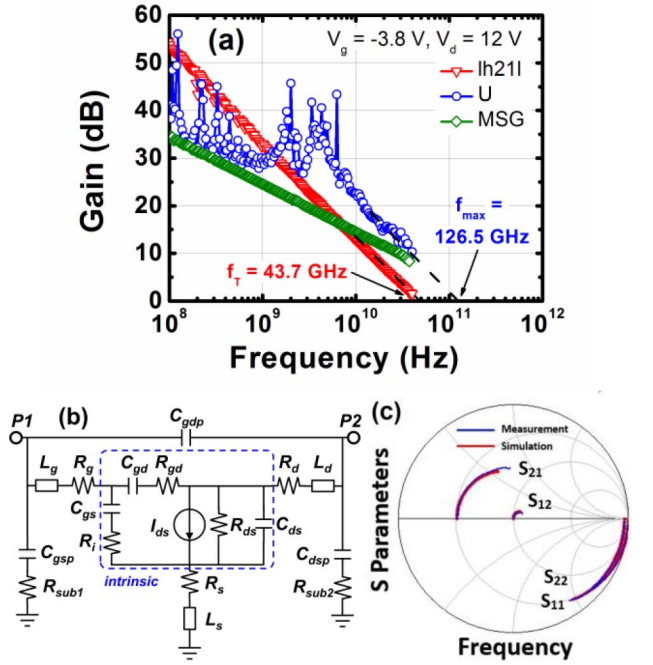

FIGURE 3. (a) De-embedded RF small signal at $V_g = -3.8$ V and $V_d = 12$ V. (b) Small-signal equivalent-circuit of GaN HEMT. (c) Smith chart of the S-parameters.

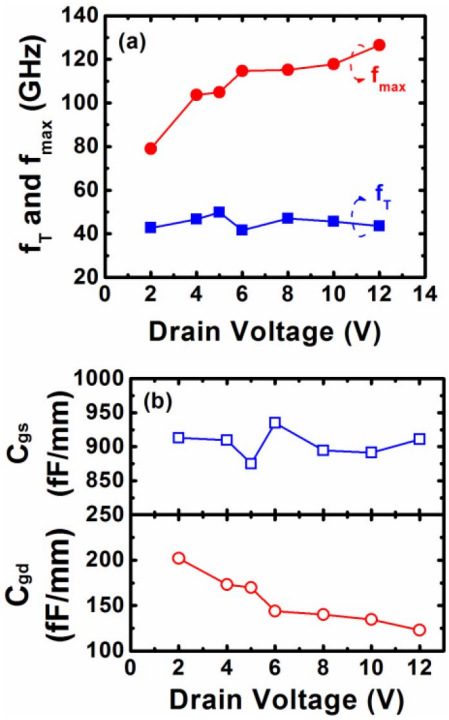

FIGURE 4. (a) f_T and f_{max} as a function of V_d. (b) C_{gd} and C_{gs} as a function of V_d.

leakage issue can be further suppressed through a passivation process since our device is unpassivated.

The S-parameters of the device are measured at a frequency of 0.04-40 GHz using an Agilent N5225A network analyzer. On-wafer open and short calibration is implemented to de-embed parasitic capacitances and inductances of the metal pad during the measurement. Figure 3(a) shows the de-embedded small-signal short-circuit current gain $|h_{21}|$, unilateral gain U, and maximum stable gain (MSG) of the device at a bias point of $V_d = 12$ V and $V_g = -3.8$ V. After subtracting the parasitic effects, the de-embedded f_T and f_{max} is 43.7 GHz and 126.5 GHz, respectively, which are extracted by extrapolating using the slope of −20 dB/dec. The small-signal equivalent-circuit is shown in Figure 3(b) based on the small-signal model [9]. Figure 3(c) exhibits the Smith chart of the measured and simulated S-parameters which indicates high consistency between simulated and measured data. The simulated f_T and f_{max} is given as 43 and 127 GHz, respectively, suggesting a deviation of less than 10%.

Figure 4(a) shows the relationship of f_T and f_{max} versus V_d at $V_g = -3.8$ V. The f_{max} increases with increasing V_d, while f_T is independent of V_d. The gate-to-source capacitance (C_{gs}) and C_{gd} which are extracted from the small-signal model are also shown in Figure 4(b). The value of C_{gs} is relatively stable when varying V_d. C_{gd} is noticeably lower in value than C_{gs} and decreases with increasing V_d. This is because with the increase of V_d, the gate-to-drain depletion region becomes smaller causing C_{gd} to decrease correspondingly. f_T is independent of V_d because f_T is dominated by the relatively large value of C_{gs} according to Equation (2) [7]:

$$f_T = \frac{g_m r_o}{2\pi\left((C_{gs}+C_{gd})\left(r_o+(R_s+R_d)+C_{gd}g_m r_o(R_s+R_d)\right)\right)} \quad (2)$$

On the other hand, f_{max} is only affected by C_{gd}. When C_{gd} decreases, f_{max} becomes higher with increasing V_d.

Table 1 lists the value of each element in the small-signal model. Compared to the references with a T-gate structure [6], [10]–[12], our R-gate device exhibits relatively low gate resistance (R_g). The RF performance is also comparable to the other T-gate GaN-on-Si devices. With further reduction of C_{gs} and C_{gd} through passivation, f_T and f_{max} can be expected to increase. Using the extracted intrinsic g_m ($g_{m,int}$) of 317 mS/mm, the extrinsic g_m ($g_{m,ext}$) can be calculated through the equation $g_{m,ext} = g_{m,int}/(1 + g_{m,int} \times R_s)$, and the calculated value of $g_{m,ext}$ is 256.1 mS/mm which is close to the measured DC g_m of 291 mS/mm.

Figure 5 benchmarks the f_{max} among reported GaN HEMTs on Si substrates with T-gate and R-gate structures. Conventionally, the value of f_T scales with L_G, making the product of f_T and L_G an indication of the performance of RF devices. The value of f_{max}, on the other hand, is able to provide further judgement of RF devices for power applications. To maintain f_{max} while scaling L_g, a reliable gate metal process without sacrificing gate resistance is needed for realizing the performance of our R-gate devices. Because of the low R_g in our R-gate devices, a high

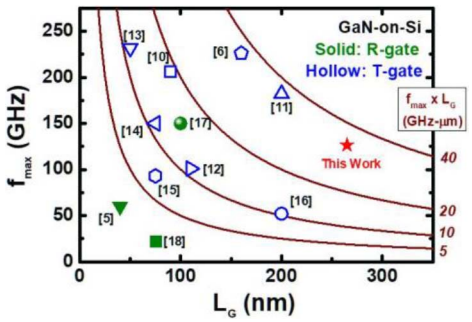

FIGURE 5. Benchmark of f_{max} vs. L_G. The contour lines show the $f_{max} \times L_G$ product of 40, 20, 10, and 5 GHz-mm respectively. This work shows a high $f_{max} \times L_G$ product of 33.52 GHz-μm.

TABLE 1. The value of each element in the small-signal equivalent-circuit.

Reference	[6]	[10]	[11]	[12]	This work
f_T (GHz)	81	100	54	60	43.7
f_{max} (GHz)	198	206	182	101	126.5
C_{gs} (fF/mm)	540	734	853	660	911
C_{gd} (fF/mm)	83	92	33	110	122.8
C_{ds} (fF/mm)	150	41	13	40	233.2
R_i (Ω-mm)	-	0.3	0.45	3.6	0.54
R_{gd} (Ω-mm)	-	190	-	-	2.24
r_o (Ω-mm)	40.1	27	900	35.2	45.7
g_m (mS/mm)	350	627	315	220	317
R_g (Ω-mm)	0.32	0.66	0.75	0.06	0.21
R_s (Ω-mm)	0.75	0.48	0.9	0.98	0.75
R_d (Ω-mm)	0.82	1.09	1.37	1.03	1.01

f_{max} is obtained and is comparable to the devices with a T-gate structure. Our R-gate device also has a high $f_{max} \times L_g$ product over 33.52 GHz-μm which is the highest among reported GaN-on-Si HEMTs with an R-gate structure.

With regards to the scaling issue for a high aspect ratio R-gate with an L_G under 265 nm, a multiple-layer photoresist is necessary for e-beam lithography to obtain a shorter L_G [19]. Meanwhile, a short-time and cold development technique have also been reported [20] as a useful method to fabricate a shorter L_G. We are convinced that the issue of maintaining a high aspect ratio for a sub-250 nm R-gate could hopefully be solved by using these techniques.

IV. CONCLUSION

In conclusion, we successfully demonstrated an AlGaN/GaN HEMT on Si substrate with a high aspect ratio R-gate structure. The maximum drain current is over 1 A/mm, and the DC peak g_m is 291 mS/mm. Because of the thick rectangular gate, R_g can be effectively reduced down to 0.21 Ω-mm. A relatively high f_{max} of 126.5 GHz and high $f_{max} \times L_G$ product of 33.52 GHz-μm were achieved and are comparable to the devices with a T-gate structure.

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