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Effects of Forming Gas Annealing and Channel Dimensions on the Electrical Characteristics of FeFETs and CMOS Inverter

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ABSTRACT In this study, ferroelectric FETs (FeFETs) and CMOS inverters are fabricated and analyzed, exhibiting 13% of 593 devices with sub-60 mV subthreshold swing (SS) at room temperature. Forming gas annealing (FGA) is found to not only enhance ferroelectricity but also significantly improve FeFET electrostatics. The experimental results indicate that FeFET with a narrow width shows weaker ferroelectric properties, and SS of sub-60 mV/dec with I_D change less than two orders of magnitude. However, FeFET with a broad channel width reveals stronger ferroelectric properties, and SS of sub-60 mV/dec is over 2 orders of magnitude of I_d. Finally, typical voltage transfer characteristics (VTCs) of a FeFET CMOS inverter with double sweeps at various V_D from 0.6 to 2 V are demonstrated. The results show that hysteresis in a FeFET CMOS inverter could have both clockwise (CW) and counter-clockwise (CCW) loops.

INDEX TERMS FeFET, forming gas annealing (FGA), steep slop, $HfZrO_2$, ferroelectric.

I. INTRODUCTION

Low power devices with very low supply voltage are attractive for emerging applications, such as high-end computational units or battery-powered portable electronics. To achieve low power consumption, MOSFETs must operate at a small V_D and require lower sub-threshold swing (SS) to achieve the same performance. However, the minimum value of the SS of MOSFET restricted by Boltzmann distribution at room temperature (300K) is 60 mV/dec. To surmount this limitation, an innovative device called ferroelectric FET (also named negative capacitance FET) with SS below 60 mV/dec was developed in recent years.

In 2014, a ferroelectric $HfZrO_2$ layer was induced into a high-K gate dielectric on a planar Si MOSFET [1]. Subsequently, various ferroelectric materials were used in a gate stack to achieve ultra-steep SS [2]–[5]. The Hf-based FeFETs have the advantage of high compatible with current CMOS fabrication, and soon this technique was induced into a FinFET structure [6]–[8].

Unlike conventional planar MOSFETs, 3D FinFET has a fabrication issue about fin sidewall roughness. The fin sidewall roughness would determine the overall performance of the FinFETs, such as V_{TH}, DIBL and SS. For scaled FinFET transistors, a channel width needs shrinking down to the nanoscale to improve the short channel immunity. However, FinFET with a narrow channel width has a serious fin sidewall roughness issue and a higher density of traps (Dit) [9], which could deteriorate SS of ferroelectric FinFET. According to works of literature, FeFETs with a broad channel width often show SS below 60 mV/dec

is over two orders of magnitude of I_D [10]–[14]. However, as a ferroelectric material is applied to nanoscale structures, such as FinFET or nanowire, SS below 60 mV/dec is often under two orders of magnitude of I_D [6]–[7], [15]–[18]. Therefore, a channel dimension may influence on electrical characteristics of FeFETs, resulting in ultra-steep SS. To investigate the effect of channel dimensions on FeFETs, wide (W = 400 nm) and narrow (W = 20 nm) widths are fabricated on a SOI wafer at the same time in this study, respectively. A large number of FeFETs are measured and characterized to discuss the relationship between channel widths and ferroelectricity. The data help us to realize what process issues need to be overcome as a FeFET is shrunk down to the nanoscale regime.

The forming gas annealing process has been proved effective in improving the surface roughness of Si-fin in CMOS FinFETs [19]–[21]. The additional interface trap density caused by etched sidewalls can reduce via hydrogen passivation. Therefore, we use forming gas annealing on the gate stack of FeFET to improve device performance and analyze electrical characteristics further, such as polarization, capacitance, SS, and hysteresis.

Finally, for ultra-low power applications, the effects of FeFETs on the circuit performance require investigating. Previous studies have shown that the VTCs of FeFET inverters can display hysteresis [22]–[24], but the results depend on simulations. Therefore, we fabricate a FeFET CMOS inverter experimentally and analyze the effect of hysteresis on VTCs of a CMOS inverter.

II. DEVICE FABRICATION

Fabrication of the FeFET [15]: Initially, the Si layer of a p-type SOI wafer was thinned down to 20 nm. The active region was defined by e-beam lithography and dry etching processes. After patterning the active regions, the gate stack was formed consisting of a 0.6 nm-thick SiO_2 interfacial layer (IL) and a 5 nm-thick $HfZrO_2$ (HZO) layer with equal amounts of Hf and Zr. An IL is the chemical oxide, which is formed by immersion of Si into a 31% H_2O_2 solution at 100°C for 300s. A HZO layer was deposited by ALD at 250°C. Subsequently; a 50 nm-thick TiN was deposited as the metal gate electrodes. Then, the samples were annealed by rapid thermal annealing (RTA) at 700°C for 30 s to transform the HZO film into the crystallized state with ferroelectric phases. Fig. 1 (a) shows the cross-sectional transmission electron microscope (TEM) image of the FeFET with HZO/metal gate stacks, and the structure is W-gated FinFET. The bottom channel width and fin heights (H_{fin}) are 20 and 25 nm, respectively. High resolution TEM (HRTEM) image in Fig. 1 (b) shows the thickness of the HZO film is 5 nm. After gate patterning, PFET and NFET regions were implanted by BF_2 of 1 x 10^{15} cm^{-2} at 10 keV and phosphorous of 1 x 10^{15} cm^{-2} at 10 keV, respectively. A subsequent S/D activation was performed by microwave annealing (MWA) at 3000W for 300 s to suppress dopant diffusion into channel [25]. After the formation of contact holes and metallization processes, FGA (N_2 95% and H_2 5%) at 400°C for 300 s was executed to eliminate possible defects at material interfaces and ferroelectric grain boundaries.

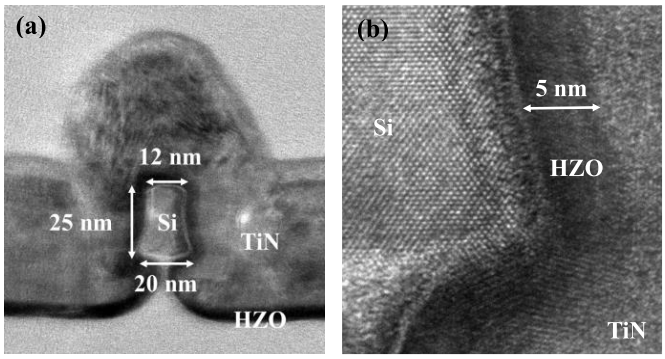

FIGURE 1. (a) Cross-sectional TEM image of a FeFET on SOI. The bottom channel width and fin height are 20 and 25 nm, respectively. (b) HRTEM image showing the 5 nm HZO film.

III. RESULTS AND DISCUSSIONS

A. EFFECT OF FGA ON FEFETS

An interface layer between the ferroelectric layer and the channel is very important in FeFET. Interface treatment could decide a behavior of FeFET, SS is more or less than 60 mV/dec.

Hydrogen and fluorine [26] passivation techniques have been applied on the gate stack widely. To investigate hydrogen forming gas annealing (FGA) effects on ferroelectric-HZO, we fabricated individual samples to measure polarization-voltage (P-V) and capacitance-voltage (C-V) curves with different conditions. For P-V measurement, the samples were fabricated as the same gate stack process on highly doped n-type silicon to form ferroelectric MIS structures ($TiN/HfZrO_2/SiO_2/N^+$). For C-V measurement, p-type silicon was used without additional ions doping. Fig. 2 shows the P-V characteristics of planar ferroelectric capacitors measured at the different process steps to examine the effect of the thermal budget on the ferroelectricity [15]. The area under the gate electrode is 2500 mm^2, and the period time of the P-V loop is 1 ms.

The RTA and MWA processes widen the original linear dielectric P-V characteristics into the counter-clockwise ferroelectric hysteresis loop, indicating the effective phase transition of HZO from the amorphous to crystallized states. After FGA, the larger ferroelectric hysteresis loop is observed, implying that defects in the crystal structure can be passivated or removed by hydrogen. Fig. 3 shows the C-V characteristics of the HZO MOSCAPs before and after FGA at 1 kHz. Note that the hump behavior around V_G of 0 to 1V is mitigated with FGA due to D_{it} passivation. We believe FGA can improve the ferroelectricity of HZO and decrease the density of traps at the interface simultaneously.

For logic FeFETs applications, the large hysteresis is a drawback as devices are operated at high electric field.

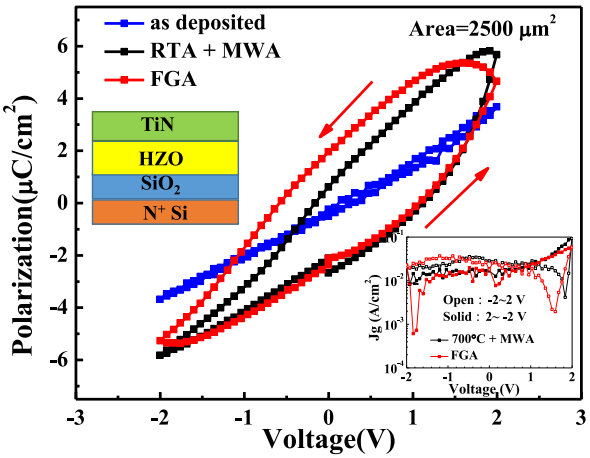

FIGURE 2. P-V characteristics of ferroelectric capacitors with TiN top electrode on an N^+ substrate ($N_d \sim 10^{20}/cm^3$). A thermal annealing facilitates ferroelectric crystallization, and FGA further enhances FE polarization [15]. The inset shows the J_g-V_g characteristic of planar ferroelectric capacitors.

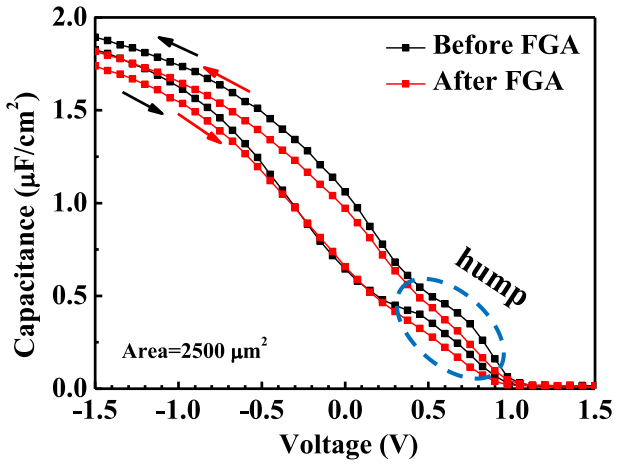

FIGURE 3. C-V characteristics before and after FGA (measured at 1 kHz). The hump behavior around 0 to 1V is mitigated with FGA due to D_{it} passivation.

This issue could be attributed to a quality of ferroelectric dielectric, which is an imperfect polycrystalline layer. Hysteresis could be classified according the threshold voltage (V_{th}) shift, CW and CCW hysteresis. For example, negative ΔV_{th} is CW and positive ΔV_{th} is CCW hysteresis ($\Delta V_{th} = |V_{th.Fwd.}| - |V_{th.Rvs.}|$). CW hysteresis is owing to interface charge-trapping effects, and CCW hysteresis could be attributed to ferroelectric properties [27]. Fig. 4 shows I_D–V_G curves of ferroelectric NFETs before and after FGA. The device is measured with a double sweep at $V_D = 0.1$ V, and the W/L_G is 35 nm/ 400 nm. G_A is defined as a channel area under a gate electrode, including top and both sidewall surfaces ($G_A = W*L_G + 2*H_{Fin}*L_G$). As a result, the FeFET shows charge trapping properties before FGA, and minimum point SS (SS_{min}) is 105 mV/dec at forwarding sweep. After FGA, the hysteresis of FeFETs

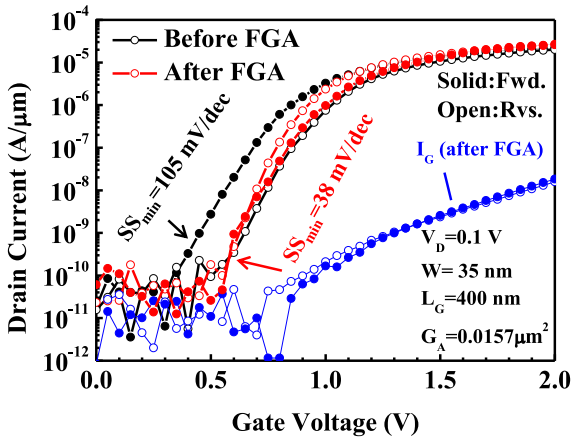

FIGURE 4. I_D–V_G curves of ferroelectric NFETs before and after FGA for forward (Fwd.) and reverse (Rvs.) sweep modes. FGA alleviate D_{it} for NFETs, resulting in significant SS improvement.

behaves ferroelectric properties, and the SS_{min} is improved from 105 mV/dec to 38 mV/dec at forwarding sweep. FGA could mitigate D_{it} at the interface, resulting in stronger ferroelectric properties for the devices.

To analyze FGA effects on the FeFETs, SS values of the NFETs and PFETs are extracted before and after FGA, respectively. The SS extracted as minimum slope above $I_D = 10^{-11}$A. The $I_D - V_G$ curves include forward and reverse sweeps. Fig. 5 show SS and hysteresis distribution of NFETs with (a) forward and (b) reverse sweeps, W/L_G = 20 nm/50 nm and $V_D = 0.1$ V. The result indicates that FGA mitigates Dit, resulting in significant SS improvement at forward and reverse sweeps. Compared with SS and hysteresis distribution before FGA, the devices show a tighter distribution after FGA.

Table 1 summarize the percentage of devices with SS below 60 mV/dec during forward and reverse sweeps, a total 593 FeFETs are measured. The measured devices are with gate lengths ranging from 50 nm to 400 nm and widths ranging from 20 nm to 400 nm. For NFETs, the percentage of working devices with SS below 60 mV/dec increases from 2 % to 13 %. For PFETs, the percentage increases from 4 % to 13 %. It should be noted that among these 593 devices, only 2 devices (< 1%) exhibit SS below 60 mV/dec simultaneously at both forward and reverse sweeping. FeFETs with hydrogen passivation is not sufficient to break through Boltzmann distribution, and SS of FeFETs may be affected by other mechanisms.

B. EFFECT OF CHANNEL DIMENSIONS ON FEFETS

Fig. 6 shows I_D-V_G curves of ferroelectric NFETs with different channel widths at $V_D = 0.1$ V. There are two types of hysteresis found obviously, CW hysteresis for 20 nm channel width and CCW hysteresis for W = 400 nm. Significant interface charge-trapping effects are found as the device dimension shrunk to W = 20 nm. This could be ascribed to the potential etch damages along the fin sidewalls. On the

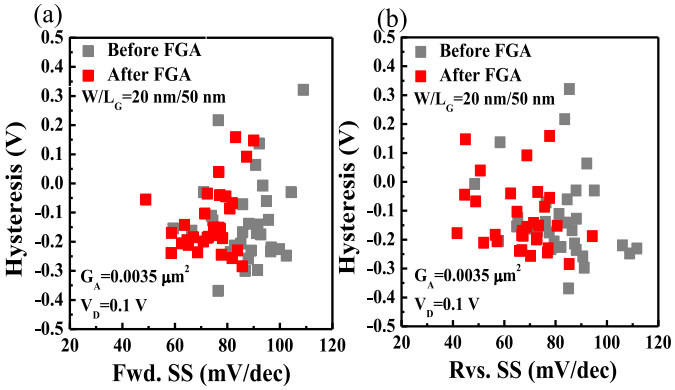

FIGURE 5. NFETs SS and hysteresis distributions before and after FGA with W/L_G = 20 nm/50 nm at V_D = 0.1 V. SS are extracted during (a) forward and (b) reverse sweeps.

TABLE 1. Summary of the percentage of devices with SS below 60 mV/dec during forward and reverse sweeps. The data is from 593 working devices. W = 20 nm, 35 nm and 400 nm.

	FGA	SS<60 mV/dec (L=50nm, 90nm, 400nm)			
		W=20	W=35	W=400	Total
NFETs	Before	1%	0%	1%	2%
	After	5%	4%	4%	13%
PFETs	Before	1%	3%	1%	4%
	After	6%	6%	1%	13%

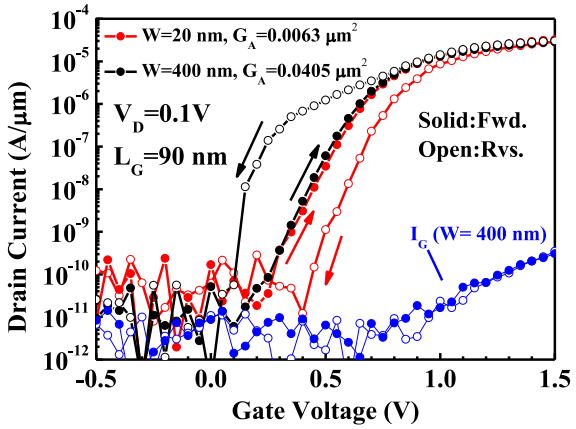

FIGURE 6. I_D-V_G curves of ferroelectric -FETs with different channel widths at V_D = 0.1 V. Two types of hysteresis are found, CW hysteresis for 20 nm channel width and CCW hysteresis for W = 400 nm.

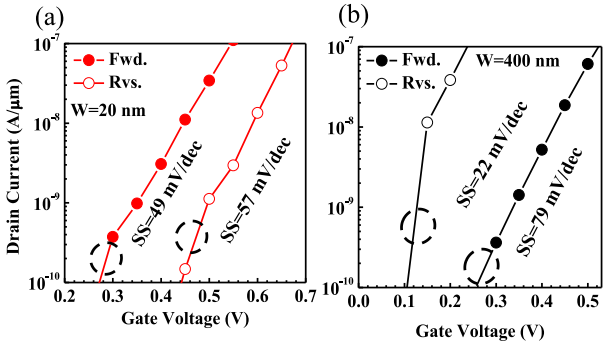

FIGURE 7. Zoom-in $I_D - V_G$ curves of (a) FeFET with W/L_G = 20 nm/90 nm and (b) FeFET with W/L_G = 400 nm/ 90 nm.

other hand, stronger ferroelectric properties are shown on the large device dimension (W = 400 nm), which is consistent with other FeFETs papers [10]–[14]. Fig. 7 shows the enlarged $I_D - V_G$ curves of Fig. 6, which is conducive to realizing the effect of device dimension shrinking from 400 nm to 20 nm. Note that although the device with a small dimension shows charge-trapping effects, the SS with sub-60 mV/dec is also occurred from 10^{-9}∼10^{-10} A/mm (Fig. 7 (a)). Therefore, the sub-60mV/dec SS is not compensated by traps. The SS_{min} is 49 mV/dec at forwarding sweep and 57 mV/dec at the reverse sweep. We believe the combination of charge-trapping effects and ferroelectric properties limit SS with sub-60 mV/dec only in 1∼2 orders of current magnitudes. For such kind of FeFETs, SS_{avg} is 102 mV/dec, and SS_{avg} is only 77 mV/dec at the reverse sweep. SS_{avg} indicates the average SS in the range of I_D from 10^{-10} to 10^{-8} A/mm. Fig. 7 (b) is an example that NFET has stronger ferroelectric properties, the SS_{min} and SS_{avg} at reverse sweep are only 22 mV/dec The current at reverse sweep drops down sharply from 10^{-8} to 10^{-10} A/mm when sweeping range of V_G is only 0.04 V. The SS_{avg} with sub-60 mV/dec is over 2 orders of current magnitudes.

A few FeFETs with W = 20 nm show ferroelectric properties in the measured data. Fig. 8 depicts hysteresis distribution for NFETs and PFETs with W = 20 nm, 35nm, and 400 nm. In both NFETs and PFETs, most devices with narrow widths (W = 20 nm and W = 35 nm) show negative hysteresis, and devices with W = 400 nm prefer to show positive hysteresis. It is true that weaker ferroelectricity domains at small device dimensions regardless of the gate length. Ferroelectric properties depend on a channel dimension strongly, which may limit the development of FeFETs scaling.

The result can be attributed to that the different channel width has a different interface trap density. From the TEM image (Fig. 1), the area of the top surface is smaller than the area of both sidewall surfaces. The fin sidewall surface quality will dominate the performance of FinFET. Compared to the top surface, the interface trap density is expected to be higher on the sidewalls due to possible dry etching damages [28]. This is a reason why FeFETs show stronger charge trapping properties as devices shrink to W = 20 nm. However, for the device with W = 400 nm, the area portion of the sidewall surface is much smaller than the top surface. Charge trapping properties influence FeFETs slightly and the magnitude of polarization may be similar to the experimental P-V data from the MOSCAPs (Fig. 2). However, a device with strong ferroelectric properties does not ensure SS of FeFET is below 60 mV/dec The SS of FeFET is affected by many factors, such as the interface D_{it}, oxide quality, capacitance matching, the magnitude of polarization

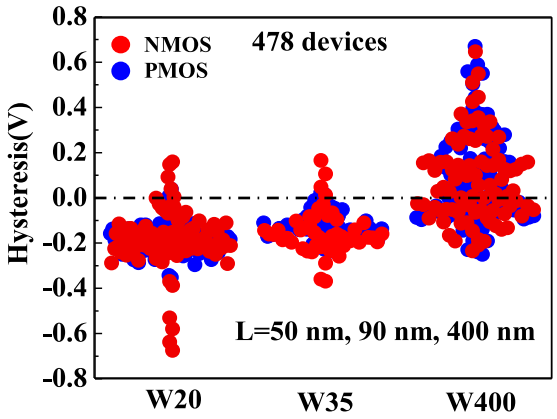

FIGURE 8. Hysteresis distribution for NFETs and PFETs at 3 design widths, W = 20 nm, 35 nm and 400 nm. The devices with a wide channel width show more prominent ferroelectric (positive) hysteresis regardless of gate length (L = 50 nm, 90 nm, 400 nm).

TABLE 2. Summary of the percentage of devices with positive hysteresis, which indicates ferroelectric properties.

	FGA	Devices with Ferroelectric Hysteresis
NFET	Before	16%
	After	21%
PFET	Before	17%
	After	19%

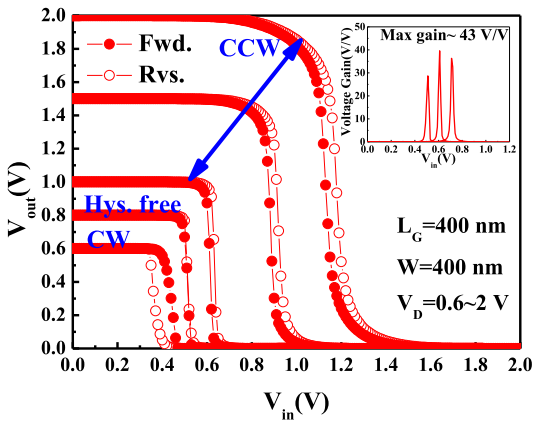

FIGURE 9. V_{out} versus V_{in} of the FeFET CMOS inverter with W/L_G = 400 nm/400 nm at various V_D from 0.6 V to 2 V. The FeFET CMOS inveter display hysteresis in a different direction as V_{in} is increased. A maximum gain about 43 V/V is achieved at V_D = 1 V as shown in the inset.

and sweeping speed [29]. Only these factors harmonize with each other well, SS below 60mV/dec could be achieved.

Here we propose some techniques to improve the performance of FeFETs, especially for the scalability of FinFETs. The ferroelectric dielectric is full of oxygen vacancies in the oxide and traps in the interface, causing the degradation of ferroelectric properties [30]. To obtain high-performance FeFET, oxygen vacancies and interface traps need reducing. Therefore, the robustness of fin sidewalls is very critical for FinFET structure, lithography, and dry etching processes should take care to reduce additional sidewall roughness and damages. The hydrogen passivation technique is an effective way to reduce interface trap density. We analyze how many FeFETs with ferroelectric properties after FGA. The results are summarized in Table 2, showing that the percentage of working devices with ferroelectric properties enhancement of up to 21 % and 19% for NFETs and PFETs, respectively. The ferroelectric properties here are defined as the CCW hysteresis in the FeFET.

C. CHARACTERIZATION OF A FEFET INVERTER

We demonstrate a FeFET CMOS inverter to understand how to utilize FeFETs in the circuits. Fig. 9 illustrates typical VTCs of a FeFET inverter with double sweeps at various V_D from 0.6 to 2 V. A maximum gain about 43 V/V is achieved at $V_D = 1$ V, as shown in the inset. Previous studies show that inverters constructed on FeFETs usually exhibit CW VTC hysteresis [22]–[24]. It should be noted that the hysteresis loop of our FeFET inverter shows the dependence of V_{in} and V_D. CW VTC hysteresis is found at $V_D = 0.6$ V while CCW VTC hysteresis at higher V_D. To investigate the mechanism, the $I_D - V_G$ curves of the CMOS N/PFETs at different V_D and V_G are thus further analyzed. Figure 10 (a) shows the transfer characteristics of N/P-FeFETs in a CMOS inverter at V_G sweep of ± 0.6 V, and V_D is also 0.6 V, which can explain why VTC hysteresis display a CW direction at a low applied voltage in Fig. 9. The PFET shows the charge-trapping dominated properties, and the NFET is almost hysteresis-free. The I_D of the PFET at forwarding sweep is higher than reverse sweep, accounting for the CMOS inverter with CW VTC hysteresis (Fig. 9). In Fig. 10(b), the NFET and PFET are almost hysteresis-free at $V_G = \pm 0.8$ V, and the VTC hysteresis is thus behaving as a conventional FinFET inverter (hysteresis free in Fig. 9). As V_D and V_G sweep from 0.6 V to 2 V, hysteresis of VTCs changes from CW to CCW. Fig. 10(c) shows the transfer curves of NFET and PFET at $V_G = \pm 2$ V, and $V_D = \pm 0.1$ V. Both of the NFET and PFET show strong ferroelectric properties at a low V_D. However, ferroelectric properties in FeFET depend on V_G and V_D in the MFIS structure. Fig. 10(d) shows transfer curves at high drain voltage, $V_D = \pm 2$V. The PFET still shows ferroelectric properties, but NFET shows slight charge-trapping properties at $V_D = 2$ V. This is why a FeFET inverter shows hysteresis in a CCW direction at $V_{in} = 2$ V. Therefore, hysteresis in a FeFET CMOS inverter could have both CW and CCW loops, depending on V_G and V_D applied. This should be considered for FeFET-based inverter applications.

IV. CONCLUSION

FeFETs with wide and narrow widths are fabricated on the same SOI wafer for this study. Ferroelectric properties are dependent on dimensions of channel width strongly. The FeFETs with a narrow channel width show more charge-trapping dominated properties, while the devices with a broad

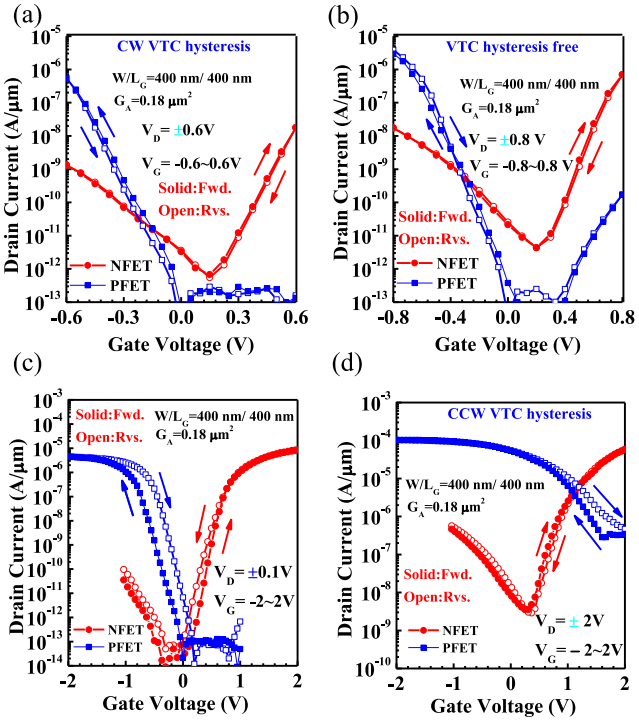

FIGURE 10. The transfer characteristics of FeFETs in a CMOS inverter at different V_G and V_D. (a) $V_G = -0.6 \sim 0.6$V and $V_D = \pm 0.6$ V, (b) $V_G = -0.8 \sim 0.8$ V and $V_D = \pm 0.8$ V, (c) $V_G = -2 \sim 2$ V and $V_D = \pm 0.1$ V, (d) $V_G = -2 \sim 2$ V and $V_D = \pm 2$ V. Ferroelectric properties in FeFET depend on V_G and V_D in the MFIS structure.

channel width exhibit stronger ferroelectric properties. To obtain high-performance FeFET, lithography and dry etching processes should take care to reduce additional fin sidewalls roughness and damages. By applying a FGA treatment, the ferroelectricity of HZO is improved, and the density of traps is decreased at the interface simultaneously. For NFETs and PFETs, the percentage of working devices with SS below 60 mV/dec is increased after FGA. Finally, a FeFET CMOS inverter is fabricated and reveal ferroelectric VTC at $V_D = 0.6$ V. As a FeFET inverter is operated in a circuit, VTC hysteresis is varied at different V_{in}, and V_D should be also considered.

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