Received 17 January 2020; revised 7 March 2020; accepted 3 April 2020. Date of publication 8 April 2020;
date of current version 28 April 2020. The review of this article was arranged by Editor P. Pavan.

Digital Object Identifier 10.1109/JEDS.2020.2986231

Dimension Scaling Effects on Conduction and Low Frequency Noise Characteristics of ITO-Stabilized ZnO Thin Film Transistors

YUAN LIU [1] (Senior Member, IEEE), YU-XUAN HUANG [1], SUNBIN DENG [2], MAN WONG [2] (Senior Member, IEEE), HOI-SING KWOK [2] (Life Fellow, IEEE), AND RONGSHENG CHEN [3] (Senior Member, IEEE)

1 School of Automation, Guangdong University of Technology, Guangzhou 510006, China
2 State Key Laboratory on Advanced Displays and Optoelectronics Technologies, Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong
3 School of Microelectronics, South China University of Technology, Guangzhou 510610, China

CORRESPONDING AUTHOR: R. CHEN (e-mail: chenrs@scut.edu.cn)

This work was supported by the Science and Technology Program of Guangdong under Grant 2019B010145001, Grant 2019A1515012127, and Grant 2020B010170002, in part by the International Cooperation Program of Guangdong under Grant 2018A050506044, in part by the International Science and Technology Cooperation Program of Guangzhou under Grant 201807010006, and in part by the Opening Fund of Key Laboratory of Silicon Device Technology under Grant KLSDTJJ2018-6.

ABSTRACT Conduction characteristics and low frequency noises in ITO-stabilized ZnO thin film transistors (TFTs) with constant channel width (W=50 μm) and different channel lengths (L=5, 10, 25, 50 and 100 μm) are measured and analysis. Firstly, dependences of threshold voltage and field effect mobility on channel length are examined. With decreasing channel length, the threshold voltage shifts to the negative direction which may attribute to carrier diffusion from source/drain to the intrinsic device channel. In addition, significant degradation of field effect mobility is observed in short channel device which are induced by the presence of series contact resistance. The value of contact resistance has also been extracted. Secondly, the drain current noise power spectral densities (S_{ID}) are measured at varied effective gate voltages. The measured noises follow a $1/f^{\gamma}$ and γ is about -1.1. Moreover, the normalized noises (S_{ID}/I_{ds}) are dependent linearly on the inverse of channel length and the slope is about -0.75. Finally, the dominant mechanism of low frequency noise in ITO-stabilized ZnO thin film transistor are examined. The slope of normalized noise against effective gate voltage are extracted, which are varied from -1.03 to -1.84 with decreasing channel length and thus it indicates that ITO-stabilized ZnO TFTs varied from bulk dominated devices to interface dominated devices. By using of ΔN-$\Delta\mu$ model, the normalized noises are simulated by considering of contact resistance. Several noise parameters (flat-band voltage noise spectral density, etc) are extracted and analysis.

INDEX TERMS ITO-stabilized ZnO, thin film transistor, low frequency noise, channel length, threshold voltage, field effect mobility.

I. INTRODUCTION

As switching elements for addressing the pixel circuit [1], Sn-doped indium-zinc-oxide (IZO) thin-film transistors (TFTs) exhibit high mobility (even over 50 cm^2/Vs) and low off current (less than 10^{-13} A) [1], [2], which can meet the requirements of next generation high vision with a pixel resolution of 8k×4k and a lower charged time per unit frame (less than 1.2 μs) [3], [4]. The best performance of oxide TFTs can be obtained at the boundary between the amorphous and crystalline phases [5]–[7]. Therefore, in these Sn-doped IZO TFTs, a number of nanocrystals are embedded in the amorphous matrix and formed hybrid-phase microstructure to achieve the best performance [3], [7]. Compared to the pristine polycrystalline ZnO, it is believed that the microstructure together with the material composition can result to thin films with lower grain boundary and deep defect

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

density inside. Thus, the conduction and noise performance of hybrid-phase Sn-doped IZO thin film transistors may be differ to existing amorphous or polycrystalline thin film transistors.

Low frequency noise (LFN) is a key parameter for analog and RF applications [8]–[10], and it sets the lower limit of the signal that can be processed and detected in the subsequent circuits and modules [11]. Moreover, LFN may up-convert to high frequencies and then become to a source of phase noise, which may adversely affect the application of devices in RF fields [8], [12]. The source and dominant mechanism of LFNs in metal oxide TFTs have been examined by many groups [9], [13]–[15]. Due to localized states existed in the active channel, the noise levels in these devices are always higher than that in MOSFETs [9], [13].

To integrate more functions on the same substrate, the channel length of devices should be reduced from typical values of L=10 μm to L=1-2 μm, or less [12], [16]. Thence, contact resistance and short channel effects may affect device performance and there should be controlled for proper operation of these devices [17]–[20]. Up to now, the effects of channel length on conduction performance have been examined [16], [17], [20]. However, the dimension scaling effects on LFN of Sn-doped IZO TFTs has less been reported. Thus, it is valuable to study the variation of low frequency noise with the decrement of channel length.

In this work, dimension scaling effect on conduction and noise performance of ITO-stabilized ZnO TFTs are investigated with channel lengths down to 5 μm. Firstly, the electrical parameters are extracted and the variations in device conduction performance due to short channel effects are discussed. Secondly, low frequency noise are measured in these devices. The source and dominant mechanism of LFN with varied channel length are examined. Moreover, the effects of contact resistance on LFN have also been discussed. Several noise parameters (such as flat-band voltage noise power spectral density, etc.) are extracted, and then LFN have been simulated by use of ΔN-$\Delta\mu$ model.

II. DEVICE STRUCTURE AND I-V CHARACTERISTICS

Fig. 1 shows the cross-section view of top gate ITO-stabilized ZnO TFTs used in this work. Thermally oxidized SiO_2 of 500 nm thick was coated on 4-inch circular glass wafers, followed by the formation of ITO source/drain electrodes. A active layer (50 nm-thick) was then co-sputtered and patterned into active islands by wet etching. During deposition, the oxygen partial pressure ratio ($O_2/(Ar+O_2)$) and DC/RF sputtering power combination adopted were 40% and 120/150 W, respectively. Subsequently, 150 nm-thick SiO_2 was deposited by PECVD as a gate dielectric layer. A 100 nm-thick ITO layer was then sputtered and patterned as gate electrodes. The devices were then annealed at 573 K in air. In the last, the devices were passivated by 300 nm-thick SiO_2 using PECVD, followed by the definition of contact holes and test pads. The experiment details have been reported previously [3], [7], [21].

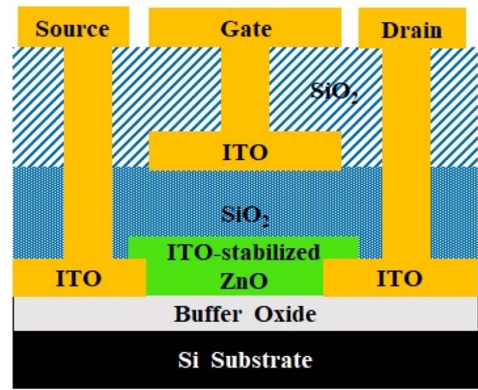


FIGURE 1. Cross-section view of top gate ITO-stabilized ZnO TFTs.

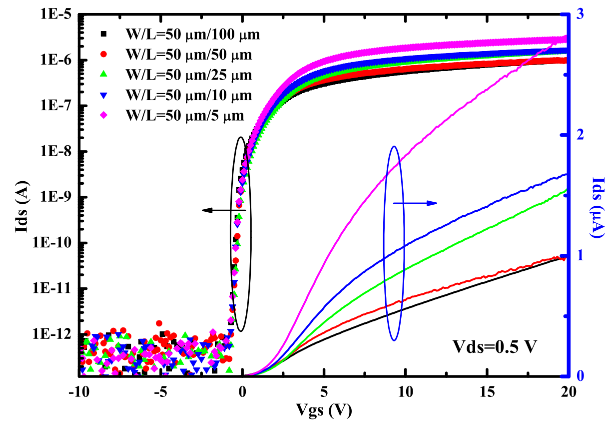


FIGURE 2. Transfer characteristics in top gate ITO-stabilized ZnO TFTs with varied channel lengths.

By use of Agilent B1500, the transfer curves ($I_{ds}-V_{gs}$) of ITO-stabilized ZnO TFTs (with W=50 μm and different channel lengths) are measured, as shown in Fig. 2. The extracted threshold voltage (V_{th}), field effect mobility (μ_{eff}) and sub-threshold swing (SS) are given in Table 1. The threshold voltages were extracted by use of linear extrapolation method, and the field effect mobility were calculated in the ohmic region when $V_{gs}-V_{th}=5V$.

As shown in Table 1, when channel length is less than 25 μm, the extracted threshold voltage may decrease with channel length decreases. This phenomena is also observed in the short channel amorphous IGZO TFTs [22]. As reported by Kang DH [22], due to carrier diffusion from source/drain regions to the active channel, the Fermi level may shift towards the conduction band with the decrement of channel length, which leads to the negative shift of V_{th} [22]. In addition, SS keeps nearly constant with the decrement of channel length.

The degradation of field effect mobility in short channel devices may dominate by the contact resistance [12], [17]. Unlike conventional MOSFETs, ITO-stabilized ZnO TFTs do not have a stable doped source/drain regions. A weak ohmic contact may exist caused by the mismatch between the work functions of the active region and the electrode. Thus,

TABLE 1. Conduction and noise parameters in the hybrid-phase Microstructural ITO-Stabilized ZnO TFTs with different gate lengths.

W	50				
L (μm)	100	50	25	10	5
$V_{th}(V)$	0.92	1.15	1.41	1.37	1.28
μ (cm^2/Vs)	12.39	7.65	5.15	2.61	2.17
SS (V/dec)	0.197	0.186	0.181	0.187	0.193
S_{Vfb} (V^2/Hz)	1.15×10^{-8}	2.2×10^{-8}	4.5×10^{-8}	7.5×10^{-8}	1.4×10^{-7}
S_{Rsd} (Ω^2/Hz)	1400	750	350	300	300

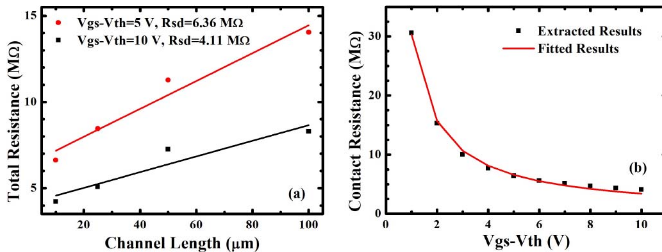


FIGURE 3. (a) Calculated total resistance versus channel length, (b) Extracted contact resistance versus $V_{gs} - V_{th}$ in ITO-stabilized ZnO TFTs.

the contacts may play a dominant role in short devices, which caused mobility decreases with the decrement of channel lengths [12], [17].

The calculated total resistance versus channel length are plotted in the Fig. 3(a). Based on transmission line method [12], [23], the calculated total resistance is close to the value of contact resistance when the channel length approximated to 0. Therefore, the value of contact resistance can be extracted by use of linear extrapolation. When $V_{ds} = 0.5$ V, the calculated contact resistances in the linear region at V_{gs}-$V_{th} = 5$ V are about 6.36 $M\Omega$. Moreover, the extracted resistance varies with $V_{gs} - V_{th}$ which follows an empirical expression $R_{sd} = R_{sd0}(V_{gs} - V_{th})^{-\beta}$ [12], [19]. In this paper, R_{sd0} is about 3.03 $M\Omega$ and β is about 0.95.

III. LOW FREQUENCY NOISE

The typical drain current noise power spectral densities (S_{ID}) versus frequency (f) are measured at different gate voltages (V_{gs}) in the ITO-stabilized ZnO TFTs with W/L=50 μm/100 μm. As shown in Fig. 4, S_{ID} follow a $1/f^{\gamma}$ law and γ is about -1.1. It suggests the flicker noise is the main noise source of LFN which is results by fluctuations of the interfacial trapped charges. The deviation from 1 of γ indicates that the vertical distribution of trap density is nonuniform in the gate insulator [9], [24]. $\gamma > 1$ is occupied when the oxide trap density is lower close to the SiO_2/channel interface than that in the interior of the gate insulator. In addition, the value of γ is also related to the localized state density and its energy distribution in the band-gap (characteristic temperature) [10].

In order to study the effect of variation of channel length on LFN, the noises have been measured at different drain current on five devices with W=50 μm and L=100, 50, 25, 10, 5 μm. The dependence of S_{ID} on I_{ds} of above devices are plotted in the Fig. 5. As shown in the Fig. 5, the measured noise increases with decreasing channel length. The

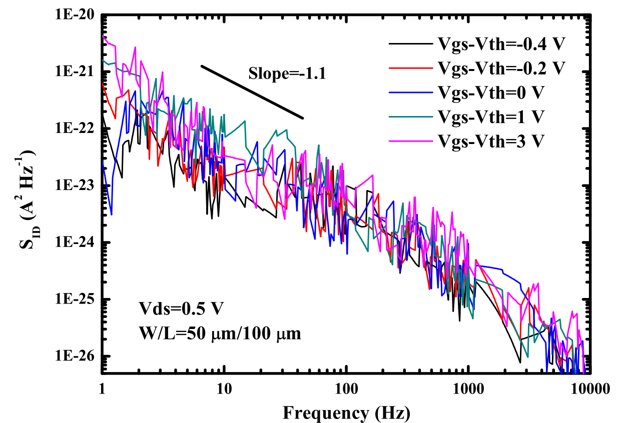


FIGURE 4. Measured drain current noises (S_{ID}) versus frequency in the ITO-stabilized ZnO TFTs.

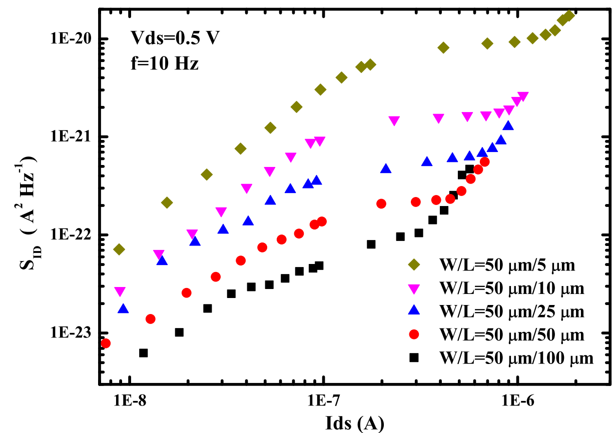


FIGURE 5. Measured noises versus drain current in the ITO-stabilized ZnO TFTs.

measured noise in the smallest device is more than two order of magnitude higher than that of the largest one.

As shown in Fig. 6, the normalized noise is inversely proportional to the channel length and the slope in a dual-log plot is about -0.75. This phenomena further confirms that the observed low frequency noise in the ITO-stabilized ZnO TFTs is flicker noise. However, differ to that observed in the IGZO TFTs [13], the contribution from TFT series contact resistance cannot be ignored which may results to the variation of field effect mobility and thus the variation of normalized noise. Therefore, the slope of noise versus channel length may deviate from -1.

There are two classic model used for the description of low frequency noise: carrier number fluctuation (ΔN) theory

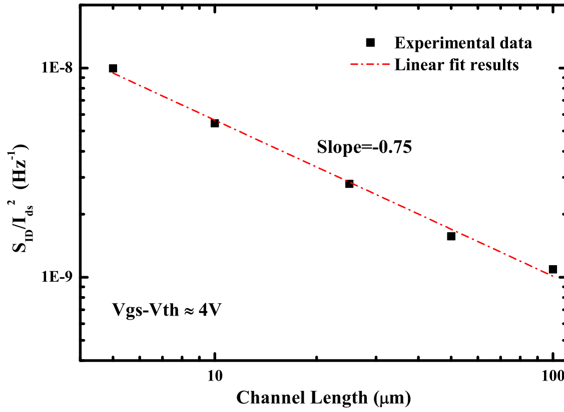


FIGURE 6. Normalized drain current noise (f=10 Hz) versus channel length. Dashed line is the best linear fit to the experiment data.

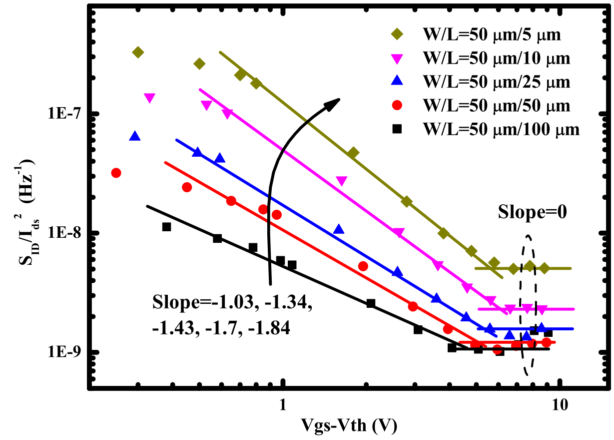


FIGURE 7. Normalized drain current noise versus $V_{gs} - V_{th}$ in the ITO-stabilized ZnO TFTs with different channel lengths (f=10 Hz).

and mobility fluctuation ($\Delta\mu$) theory. In the ΔN theory, the drain current fluctuations are caused by the interfacial charges' fluctuations, which are due to the trapping and de-trapping processes of free carriers into border traps and localized states. Based on ΔN theory, the normalized current noise (S_{ID}/I_{ds}^2) in the ohmic region is a function of $1/(V_{gs} - V_{th})^2$ [13]. In contrast to ΔN theory, according to Hooge's $\Delta\mu$ theory [25], 1/f noise may originate from noise in lattice scattering, which in turn results to random mobility fluctuation. Based on $\Delta\mu$ theory, the normalized current noise in the ohmic region is a function of $1/(V_{gs} - V_{th})$ [13], [25].

To examine the main mechanism of LFN in the above threshold region, the dependence of S_{ID}/I_{ds}^2 on $V_{gs} - V_{th}$ are extracted at $V_{ds} = 0.5$ V and f=10 Hz. As plotted in Fig. 7, the extracted power law coefficients of $log(S_{ID}/I_{ds}^2)$ versus $log(V_{gs} - V_{th})$ are in the range of -1.03 and -1.84. Thus, the long channel devices are dominated by $\Delta\mu$ theory and the short channel devices are dominated by ΔN theory.

As shown in Fig. 7, the slope of S_I/I_d^2 against $V_{gs} - V_{th}$ varied from -1.03 to -1.84, which may due to the variation of the origin of LFN [26]–[28]. In the long channel devices, the presence of clusters and localized states may push the bulk effect noise to be the predominant origin of the whole noise, and the mobility fluctuation is the main mechanism. However, with decreasing channel length, the quality of the interface between insulator/channel is critical. Thus, the fluctuation induced by trapping/emission of free carriers near the oxide/channel interface becomes more important [28]. Therefore, ITO-stabilized ZnO TFTs varied from bulk dominated devices to interface dominated devices with the decrement of channel length, and it may result to the variation of the slope of S_I/I_d^2 against $V_{gs} - V_{th}$.

As discussed above, the slopes of S_{ID}/I_{ds}^2 against $V_{gs} - V_{th}$ of our devices are between -1 and -2, thus LFN can be simulated by using carrier number with correlated mobility fluctuations (ΔN-$\Delta\mu$) model [28]–[30]. Based on ΔN-$\Delta\mu$ model, the interfacial charges fluctuation results to a supplementary change of the mobility, and then induces an extra drain current fluctuation. Thus, S_{ID}/I_{ds}^2 can be calculated by [28]–[30]

$$\frac{S_{ID}}{I_{ds}^2} = \left(1 \pm \alpha_c \mu_{eff} C_{ox} I_{ds}/g_m\right)\left(\frac{g_m}{I_{ds}}\right)^2 \cdot S_{vfb} \tag{1}$$

where α_c is a fitting parameter relate to the coulomb scattering. A low value of α_c means less sensitivity of the mobility to the insulator charge [9], [29]. S_{vfb} is the flat-band voltage noise power spectral density which can be expressed by [30]

$$S_{vfb} = \frac{q^2 KT\lambda N_t}{WLC_{ox}^2 f^{\gamma}} \tag{2}$$

where λ is the tunneling attenuation coefficient, which is about 0.1 nm for SiO_2. N_t is the trap density near the SiO_2/channel interface.

As proposed by Ghibaudo *et al.* and Boutchacha *et al.* [29], [31], the gate voltage noise spectral density (S_{vg}) in the linear region can be expressed by:

$$S_{vg} = \frac{S_{ID}}{g_m^2} = S_{vfb}\left[1 \pm \alpha_c \mu_{eff} C_{ox}\left(V_{gs} - V_{th}\right)\right]^2 \tag{3}$$

Variations of S_{vg} with $V_{gs} - V_{th}$ in ITO-stabilized ZnO TFTs are plotted in Fig. 8. In the above threshold region, S_{vg} are varying superlinear with $V_{gs} - V_{th}$. In addition, the variation slopes of S_{vg} with $V_{gs} - V_{th}$ are dependent on the channel length [29], [31]. Thus, the variation rate may increase with decreasing channel length. Similar phenomena are also been observed in MOSFETs [29], [31] and poly-Si TFTs [12].

In order to find the value of α_c and S_{vfb} in the Eq. (3), follows the extraction method proposed by Boutchacha *et al.* [31], the variations of $S_{vg}^{1/2}$ as a function of $V_{gs} - V_{th}$ are plotted in Fig. 9. In the above threshold region, $S_{vg}^{1/2}$ changes linearly with $V_{gs} - V_{th}$. Based on Eq. (3) and Fig. 9, the extracted S_{Vfb} are about 1.15×10^{-8} V^2/Hz (L=100 μm), 2.2×10^{-8} V^2/Hz (L=50 μm), 4.5×10^{-8} V^2/Hz (L=25 μm), 7.5×10^{-8} V^2/Hz (L=10 μm), 1.4×10^{-7} V^2/Hz (L=5 μm), respectively. The value

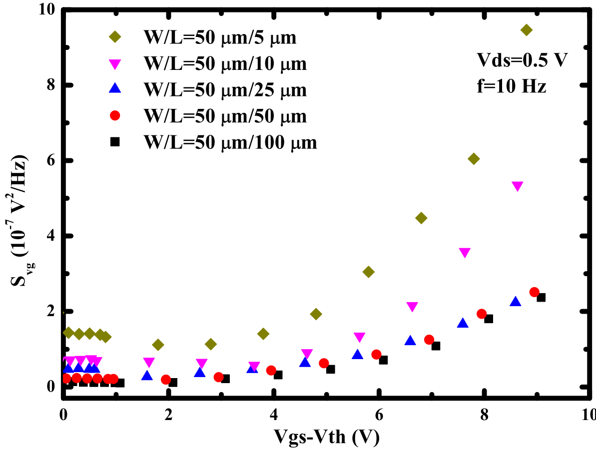


FIGURE 8. Variation of the gate voltage noise (S_{vg}) with $V_{gs} - V_{th}$ in ITO-stabilized ZnO TFTs.

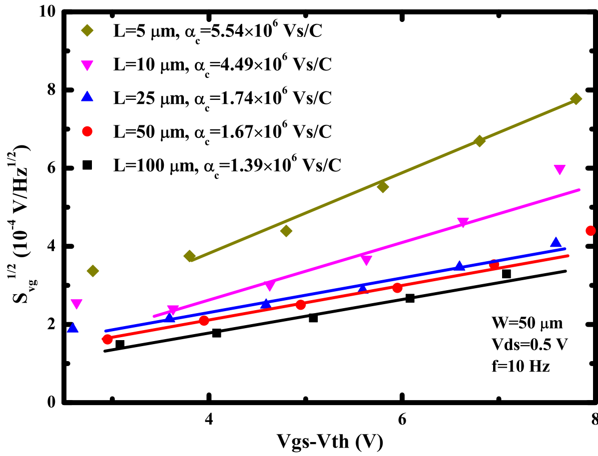


FIGURE 9. Variation of $S_{Vg}^{1/2}$ with $V_{gs} - V_{th}$ in ITO-stabilized ZnO TFTs. The continuous lines are fit to (1) $\alpha_c = 1.39 \times 10^6 Vs/C$ (L=100 μm); (2) $\alpha_c = 1.67 \times 10^6 Vs/C$ (L=50 μm); (3) $\alpha_c = 1.74 \times 10^6 Vs/C$ (L=25 μm); (4) $\alpha_c = 4.49 \times 10^6 Vs/C$ (L=10 μm); (5) $\alpha_c = 5.54 \times 10^6 Vs/C$ (L=5 μm).

of S_{vfb} approximately linear increases with the decrement of channel length, which is similar to the prediction of Eq. (2). Moreover, based on Eq. (2), the calculated N_t of our devices are in the range of $2.79 \times 10^{18} cm^{-3}eV^{-1}$ to $4.58 \times 10^{18} cm^{-3}eV^{-1}$.

According to Eq. (3), the scattering parameters α_c can be extracted from the slopes of $S_{vg}^{1/2}$-$V_{gs} - V_{th}$ curves in the above threshold region, and their values are in the range of 1.37×10^6 and 5.54×10^6 Vs/C. As discussed above, the dominant mechanism of noise may vary from mobility fluctuation to carrier number fluctuation, and α_c should be decreased with decreasing channel length. However, the extracted values of α_c from Fig. 9 are inconsistent with these predictions which may cause by the effect of contact resistance. At higher current intensities, contact resistance play an important role both in conduction and noise characteristics, especially in short channel devices. Therefore, the extracted α_c from Fig. 9 are dependent on contact resistance rather

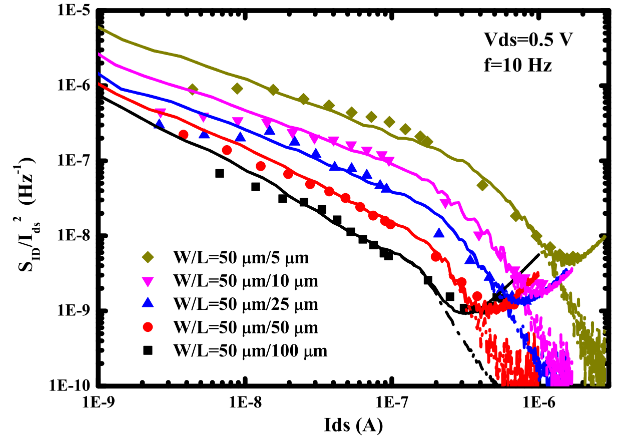


FIGURE 10. Normalized noises versus current in the ohmic region (f=10 Hz). (Dots: Measured results, Dash Lines: Without contact resistance, Solid Lines: With contact resistance.)

than channel resistance. This phenomenon is more significant in short channel devices and induce to the increment of α_c with decreasing channel length. A more correct value of α_c should be extracted in lower gate voltages with lower current intensities. Thence, the value of α_c used in following calculations is assumed to be 0.

The normalized drain current noises versus drain current in ITO-stabilized ZnO TFTs are shown in Fig. 10. By using of ΔN-$\Delta\mu$ model, the measured noise can be simulated, as shown by dash lines in Fig. 10. The simulated results are in good agreements with the measured noise under low drain current intensities. However, under higher drain current intensities, discrepancies occur between measured results and simulated results, which may cause by the contact resistance noise.

The channel and contact are both contribute to LFN. Thus, the total noises include channel noise and contact noise [12], [23], [32]. As reported [12], [23], [32], the measured noises are dominated by the channel under low current intensities and dominated by the contact under high current intensities. By consider of contact resistance, the noise can be expressed by [12], [23], [32]

$$\frac{S_{ID,R}}{I_{ds}^2} = \frac{S_{ID}}{I_{ds}^2} + \left(\frac{I_{ds}}{V_{ds}}\right)^2 \frac{S_{Rsd}}{R_{sd}^2} R_{sd}^2 \tag{4}$$

here S_{Rsd}/R_{sd}^2 is the normalized noise of contact resistance. By using of Eq. (4), the measured noise can be well approximated under high currents, as shown by solid lines in Fig. 10.

As shown in Fig. 10, the total resistance and related noise are determined by the contact resistance under high current intensities, therefore the total resistance can be approximated by:

$$\frac{S_{ID,R}}{I_{ds}^2} \approx \frac{S_{Rsd}}{R_{sd}^2} \propto \left(V_{gs} - V_{th}\right)^0 \tag{5}$$

Based on Eq. (5), under high current and high gate voltages, the normalized noise is unsensitive to the gate voltages, therefore the slope of normalized noise versus gate voltages is nearly zero, as shown in Fig. 7.

Moreover, the contact noise can be simulated by an empirical model [23], [29]

$$S_{Rsd}/R_{sd}^2 = \alpha_H/WLfN \propto 1/I_{ds} \propto L \quad (6)$$

Based on Eq. (6), S_{Rsd}/R_{sd}^2 may decrease with the decrement of channel length, which is consistent with the extraction results in the long channel devices (L>10 μm), as shown in Table 1. Similar results have also been observed in OTFTs [23] and Poly-Si TFTs [12].

IV. CONCLUSION

Dimension scaling effects on I-V and low frequency noise in ITO-stabilized ZnO TFTs are investigated. The dependence of threshold voltage and field effect mobility on channel length are studied. The carrier diffusion from source/drain to the channel may induce to the negative shift of threshold voltage, and the presence of series contact resistance may result to the degradation of field effect mobility. Moreover, measured noises follow a $1/f^\gamma$ type spectrum. The measured noises indicate that LFN are well interpreted by carrier number with correlated mobility fluctuations model added with access resistance fluctuation at higher current intensities.

REFERENCES

[1] E. Fukumoto *et al.*, "High-mobility oxide TFT for circuit integration of AMOLEDs," *J. Soc. Inf. Display*, vol. 19, no. 12, pp. 867–872, Dec. 2011, doi: 10.1889/JSID19.12.867.

[2] J. H. Song, K. S. Kim, Y. G. Mo, R. Choi, and J. K. Jeong, "Achieving high field-effect mobility exceeding 50 cm2/Vs in In-Zn-Sn-O thin film transistors," *IEEE Electron Device Lett.*, vol. 35, no. 8, pp. 853–855, Aug. 2014, doi: 10.1109/LED.2014.2329892.

[3] S. Deng *et al.*, "Investigation of high-performance ITO-Stabilized ZnO TFTs with hybrid-phase microstructural channels," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3174–3182, Aug. 2017, doi: 10.1109/TED.2017.2711199.

[4] T. Arai and T. Sasaoka, "49.1: Invited Paper: Emergent oxide TFT technologies for next-generation AM-OLED displays," in *SID Symp. Dig. Techn. Papers*, vol. 42, no. 1, pp. 710–713, 2011, doi: 10.1889/1.3621424.

[5] E. Lee, T. Kim, A. Benayad, H. Kim, S. Jeon, and G. S. Park, "Ar plasma treated ZnON transistor for future thin film electronics," *Appl. Phys. Lett.*, vol. 107, no. 12, Sep. 2015, Art. no. 122105, doi: 10.1063/1.4930827.

[6] J. S. Park, K. Kim, Y. G. Park, Y. G. Mo, H. D. Kim, and J. K. Jeong, "Novel ZrInZnO thin-film transistor with excellent stability," *Adv. Mater.*, vol. 21, no. 3, pp. 329–333, 2009, doi: 10.1002/adma.200802246.

[7] S. Deng *et al.*, "High-performance staggered top-gate thin-film transistors with hybrid-phase microstructural ITO-stabilized ZnO channels," *Appl. Phys. Lett.*, vol. 109, no. 18, Oct. 2016, Art. no. 182105, doi: 10.1063/1.4966900.

[8] A. Jerng and C. G. Sodini, "The impact of devices type and size on phase mechanisms," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 360–369, Feb. 2005, doi: 10.1109/JSSC.2004.841035.

[9] Y. Liu, H. He, R. Chen, Y. F. En, B. Li, and Y. Q. Chen, "Analysis and simulation of low-frequency noise in indium-zinc-oxide thin-film transistors," *IEEE J. Electron Device Soc.*, vol. 6, no. 1, pp. 271–279, 2018, doi: 10.1109/JEDS.2018.2800049.

[10] C. T. Angelis, C. A. Dimitriadis, F. V. Farmakis, J. Brini, G. Kamarinos, and M. Miyasaka, "Dimension scaling of low frequency noise in the drain current of polycrystalline silicon thin-film transistors," *J. Appl. Phys.*, vol. 86, no. 12, pp. 7083–7086, Dec. 1999, doi: 10.1063/1.371721.

[11] T. Noulis, S. Siskos, and G. Sarrabayrouse, "Analysis and selection criteria of BSIM4 flicker noise simulation models," *Int. J. Circuits Theory Appl.*, vol. 36, no. 7, pp. 813–823, Oct. 2008, doi: 10.1002/cta.461.

[12] Y. Liu *et al.*, "Scaling down effect on low frequency noise in polycrystalline silicon thin-film transistors," *IEEE J. Electron Device Soc.*, vol. 7, no. 1, pp. 203–209, 2019, doi: 10.1109/JEDS.2018.2890737.

[13] T. C. Fung, G. Baek, and J. Kanicki, "Low frequency noise in long channel amorphous In-Ga-Zn-O thin film transistors," *J. Appl. Phys.*, vol. 108, no. 7, Oct. 2010, Art. no. 074518, doi: 10.1063/1.3490193.

[14] D. Wan *et al.*, "Low-frequency noise in high-mobility a-InGaZnO/InSnO nanowire composite thin-film transistors," *IEEE Electron Device Lett.*, vol. 38, no. 11, pp. 1540–1542, Nov. 2017, doi: 10.1109/LED.2017.2757144.

[15] C. Y. Jeong, J. H. Lee, Y. J. Choi, C. W. Lee, S. H. Song, and H. I. Kwon, "Low-frequency noise properties in p-type SnO thin-film transistors," *J. Nonosci. Nanotechnol.*, vol. 16, no. 11, pp. 11381–11385, Nov. 2016, doi: 10.1166/jnn.2016.13513.

[16] G. Fortunato, A. Valletta, P. Gaucci, L. Mariucci, and S. D. Brotherton, "Short channel effects in polysilicon thin film transistors," *Thin Solid Films*, vol. 487, no. 1-2, pp. 221–226, Sep. 2005, doi: 10.1016/j.tsf.2005.01.069.

[17] N. V. Duy *et al.*, "Effect of series resistance on field effect mobility at varying channel lengths and investigation into the enhancement of source/drain metallized thin-film transistor characteristics," *Jpn. J. Appl. Phys.*, vol. 50, no. 2, Feb. 2011, Art. no. 024101, doi: 10.1143/JJAP.50.024101.

[18] G. Giusi *et al.*, "Correlated mobility fluctuations and contact effects in p-type organic thin-film transistors," *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 1239–1245, Mar. 2016, doi: 10.1109/TED.2016.2518305.

[19] Y. Xu *et al.*, "Extraction of low-frequency noise in contact resistance of organic field-effect transistors," *Appl. Phys. Lett.*, vol. 97, no. 3, Jul. 2010, Art. no. 033503, doi: 10.1063/1.3467057.

[20] A. Valletta, G. Fortunato, L. Mariucci, P. Barquinha, R. Martins, and E. Fortunato, "Contact effects in amorphous InGaZnO thin film transistors," *J. Disp. Technol.*, vol. 10, no. 11, pp. 956–961, Nov. 2014, doi: 10.1109/JDT.2014.2328376.

[21] Y. Liu, S. Deng, R. Chen, B. Li, Y. F. En, and Y. Chen, "Low frequency noise in the hybrid-phase-microstructure ITO-stabilized ZnO thin film transistors," *IEEE Electron Device Lett.*, vol. 39, no. 2, pp. 200–203, Feb. 2018, doi: 10.1109/LED.2017.2784844.

[22] D. H. Kang, J. U. Han, M. Mativenga, S. H. Ha, and J. Jang, "Threshold voltage dependence on channel length in amorphous-indium-gallium-zinc-oxide thin-film transistors," *Appl. Phys. Lett.*, vol. 102, no. 8, pp. 083508, Feb. 2013, doi: 10.1063/1.4793996.

[23] Y. Xu, T. Minari, K. Tsukagoshi, J. Chroboczek, F. Balestra, and G. Ghibaudo, "Origin of low-frequency noise in pentacene field-effect transistors," *Solid-State Electron.*, vol. 61, no. 1, pp. 106–110, Feb. 2011, doi: 10.1016/j.sse.2011.01.002.

[24] R. Jayaraman and C. G. Sodini, "A 1/f noise technique to extract the oxide trap density near the conduction band edge of silicon," *IEEE Trans. Electron Devices*, vol. 36, no. 9, pp. 1773–1782, Sep. 1989, doi: 10.1109/16.34242.

[25] F. N. Hooge, "1/f noise sources," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 1926–1935, Nov. 1994, doi: 10.1109/16.333808.

[26] J. Rhayem, M. Valenza, D. Riguad, M. Szydlo, and H. Lebrun, "1/f noise investigations in small channel length amorphous silicon thin film transistors" *J. Appl. Phys.*, vol. 83, no. 7, pp. 3660–3667, Apr. 1998, doi: 10.1063/1.366586.

[27] K.-S. Jeong *et al.*, "Crystal quality effect on low-frequency noise in ZnO TFTs," *IEEE Electron Device Lett.*, vol. 32, no. 12, pp. 1701–1703, Dec. 2011, doi: 10.1109/LED.2011.2167312.

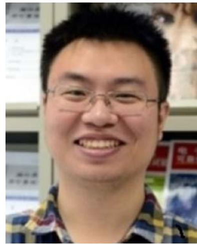
[28] D. Riguad, M. Valenza, and J. Rhayem, "Low frequency noise in thin film transistors" *IET. Proc. Circuits Devices Syst.*, vol. 149, no. 1, pp. 75–82, Feb. 2002, doi: 10.1049/ip-eds:20020063.

[29] G. Ghibaudo, O. Roux, C. Nguyenduc, F. Balestra, and J. Brini, "Improved analysis of low frequency noise in field-effect MOS transistors" *Phys. Status Solidi A*, vol. 124, no. 2, pp. 571–581, Apr. 1991, doi: 10.1002/pssa.2211240225.

[30] C. A. Dimitriadis, J. Brini, and G. Kamarinos, "Origin of low-frequency noise in polycrystalline silicon thin-film transistors," *Thin Solid Films*, vol. 427, no. 1-2, pp. 113–116, Mar. 2003, doi: 10.1016/S0040-6090(02)01153-7.

[31] T. Boutchacha, G. Ghibaudo, and B. Belmekki, "Study of low frequency noise in the 0.18 μm silicon CMOS transistors," in *Proc. Int. Conf. Microelectron. Test Struct.*, 1999, pp. 84–88, doi: 10.1109/Icmts.1999.766221.

[32] H. He, X. Zheng, and S. Zhang, "Above-threshold 1/f noise expression for amorphous InGaZnO thin film transistors considering series resistance," *IEEE Electron Device Lett.*, vol. 36, no. 10, pp. 1056–1058, Oct. 2015, doi: 10.1109/LED.2015.2469723.



YUAN LIU (Senior Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from the South China University of Technology, Guangzhou, China, in 2004 and 2009, respectively.

From 2011 to 2017, he was a Senior Engineer with China Electronic Product Reliability and Environmental Testing Research Institute. Since 2018, he has been an Associate Professor with the School of Automation, Guangdong University of Technology. His research include characterization, modeling, and reliability of semiconductor devices.

YU-XUAN HUANG received the B.S. degree from the Nanyang Institute of Technology in 2019. She is currently pursuing the M.S. degree in control engineering with the Guangdong University of Technology.

Her research interests are in the characterization and reliability of semiconductor devices.

SUNBIN DENG received the B.S. degree in optical information science and technology from the Huazhong University of Science and Technology, Wuhan, China, in 2014. He is currently pursuing the Ph.D. degree with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong.

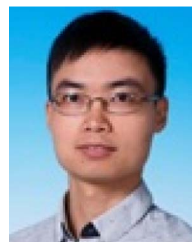
His current research interests include poly-Si, metal-oxide, and novel material thin-film transistors.

MAN WONG (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the Center for Integrated Systems, Stanford University, Palo Alto, CA, USA.

In 1992, he joined the Department of Electrical and Electronic Engineering, Hong Kong University of Science and Technology, Hong Kong, as a Faculty Member.

HOI-SING KWOK (Life Fellow, IEEE) received the Ph.D. degree in applied physics from Harvard University, Cambridge, MA, USA, in 1978.

In 1992, he joined the Hong Kong University of Science and Technology, Hong Kong, where he is currently the Director of the Center for Display Research and the State Key Laboratory on Advanced Displays and Optoelectronics Technologies.



RONGSHENG CHEN (Senior Member, IEEE) received the Ph.D. degree from the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong, in 2013.

His current research interests include novel compound thin-film transistors based on ZnO, IGZO, GaN, and their application in active matrix displays.