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Improvement in Electrical Characteristics of ZnSnO/Si Bilayer TFET by W/Al_2O_3 Gate Stack

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ABSTRACT We have examined impacts of gate insulator (Al_2O_3 or HfO_2) and gate electrode (TiN or W) on electrical performance of ZnSnO/Si bilayer tunneling fieldeffect transistors (TFETs). It is found from the capacitance-voltage (*C*-*V*) characteristics that the W gate is effective to reduce the counter-clockwise hysteresis. Additionally, the optimal temperature of post-metallization annealing (PMA) is different for each gate stack, and this optimization is critically important for the high ON-state current (I_{ON}) and steep ON/OFF switching. The W/Al_2O_3/ZnSnO/Si bilayer TFET provides the hysteresis-free steep ON/OFF switching with the minimum sub-threshold swing (*SS*) of 65.4 mV/dec. and average *SS* of 72.0 mV/dec. in a gate-voltage swing of 0.3 V, which are 19% and 18% lower than the control TiN/Al_2O_3/ZnSnO/Si bilayer TFET. When the gate stack is replaced by W/HfO_2/Al_2O_3, the TFET exhibits less steep ON/OFF switching in spite of thinning capacitance equivalent thickness (CET) from 5.9 and 2.3 nm. These results indicate the importance of improvement in the gate stack quality on the sub-threshold characteristics of the bilayer TFETs.

INDEX TERMS Bilayer, gate stack, TFET, sub-threshold, ZnSnO.

I. INTRODUCTION

In order to increase ON-state current (I_{ON}) of tunneling field-effect transistors (TFETs) without increasing the OFF-state leakage current (I_{OFF}), a hetero tunneling junction with type-II energy band alignment is promising because of the reduced effective tunneling barrier height [1]–[12]. Various semiconductor materials such as III-V [1]–[8], Ge/Si [9], [10], and 2D materials [11], [12] have been introduced to increase I_{ON}. Additionally, a bilayer structure is another attractive approach to reduction in sub-threshold swing (*SS*) and increase in I_{ON} thanks to uniform band-to-band tunneling (BTBT) over an entire region of the tunneling junction [12]–[16]. Recently, we have proposed a bilayer TFET structure composed of the hetero-tunneling junction of an n-type oxide semiconductor (n-OS) and a p-type group-IV semiconductor (p-IV), which can realize the above two approaches at the same time [17]. Device simulation has predicted that the extremely-small *SS* of as small as $\sim$1 mV/dec. can be expected in the proposed n-OS/p-IV bilayer TFET [18].

We have also experimentally demonstrated the TFET operation by utilizing ZnO/Si, ZnO/Ge [19], and ZnSnO/Si [20] bilayer TFET devices with a TiN/Al_2O_3 gate stack, where it has been confirmed that the source-to-drain current is dominated by tunneling current [19]. However, the minimum *SS* values experimentally achieved so far have been 71 mV/dec. and 81 mV/dec. for the ZnO/Si and ZnSnO/Si bilayer TFETs, respectively, which are much higher than those with the simulated results. Also, a large hysteresis has been observed in the transfer characteristics of the ZnO/Si bilayer TFET, which is another obstacle for reduction of the supply voltage. One of possible reasons of these undesired electrical characteristics of the experimentally fabricated bilayer TFETs are poor qualities of the metal/insulator/OS gate stack structures.

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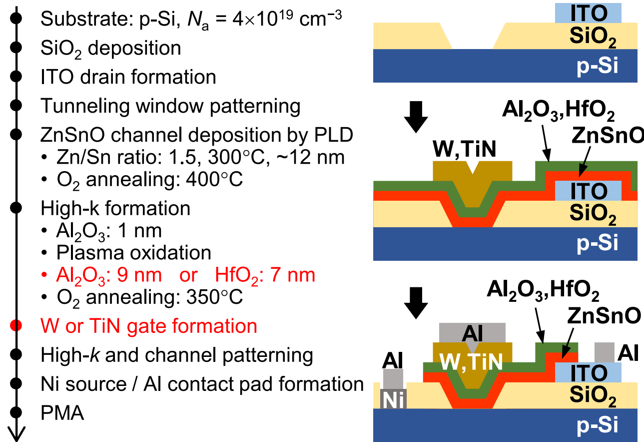

FIGURE 1. ZnSnO/Si TFET device fabrication flow and cross sectional illustration of the bilayer TFET structure.

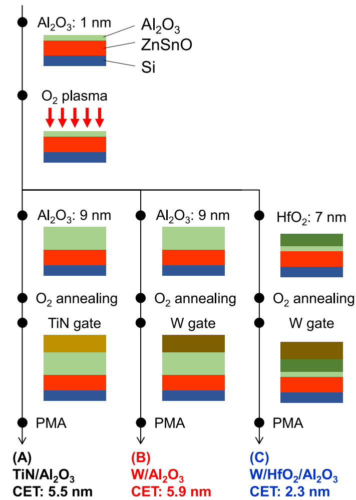

FIGURE 2. Detailed process flow for metal/high-*k*/ZnSnO gate stacks. Three types of gate stacks of TiN/Al_2O_3, W/Al_2O_3, and W/HfO_2/Al_2O_3 were examined.

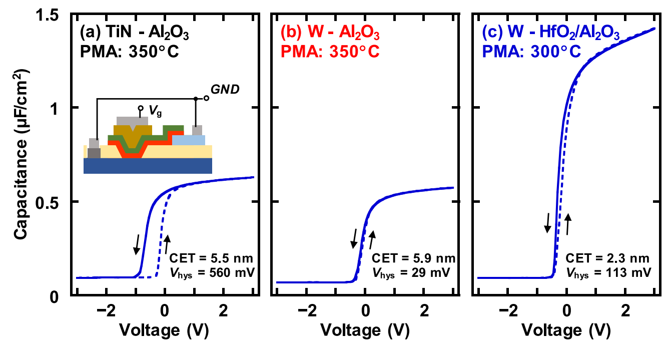

FIGURE 3. *C-V* characteristics of (a) TiN/Al_2O_3, (b) W/Al_2O_3, and (c) W/HfO_2/Al_2O_3 gate stacks. Bilayer TFET structure was used also for *C-V* measurement, and both source and drain electrodes were grounded. Measurement frequency was 1 kHz.

In general, it has been reported mainly through results of device simulation that the influence of interface states on sub-threshold characteristics of TFETs is small, since the surface potential modulation during the ON/OFF operation of TFETs and resulting amounts of trapped or de-trapped charges are relatively small [21]–[23]. On the other hand, drastic degradation of *SS* with a high interface state density has been experimentally reported [24], suggesting the trap-assisted tunneling via defects at high-*k*/channel interfaces. It should be noted, particularly in the OS/IV material system, that defect states in the gate stacks could be sensitive to the gate metal/gate insulator materials and the process conditions, because the oxygen concentration in OS drastically changes the characteristics [25], [26]. In this study, therefore, we have examined the impact of the gate electrode and the gate insulator on the electrical performance, particularly on the sub-threshold characteristics, of ZnSnO/Si bilayer TFETs.

II. DEVICE FABRICATION PROCESS

N-ZnSnO/p-Si bilayer TFETs with various gate stacks were fabricated, according to the process flow shown in Fig. 1. The TFETs were fabricated on a p^+-Si(100) substrate with an impurity concentration of 4×10^{19} cm^{-3}. Note that this p^+-Si substrate works as the source region and this source impurity concentration of middle of 10^{19} cm^{-3} is the optimum to realize steep sub-threshold characteristics while keeping the large ON/OFF current ratio [19]. An SiO_2 passivation layer and an In-Sn-O (ITO) buried drain electrode were formed by plasma-enhanced chemical vapor deposition and sputtering, respectively, and a window for the tunneling junction was formed by chemical etching using BHF. Then, the amorphous ZnSnO channel layer was deposited by pulsed laser deposition (PLD) in an O_2 partial pressure of $\sim 10^{-3}$ Pa. Both the deposition temperature and the Zn/Sn ratio in the sintered PLD target of ZnSnO were carefully controlled to be 300° C and 1.5, respectively, in order to realize high thickness uniformity [20].

Subsequently, the gate stacks were formed as follows (Fig. 2). For all the samples, 1 nm-thick Al_2O_3 was deposited by atomic layer deposition (ALD) at 200° C, followed by plasma oxidation to reduce the interface state density at the Al_2O_3/ZnSnO interface [25]. Successively, 9 nm-thick Al_2O_3 or 7 nm-thick HfO_2 layer was deposited by ALD at 200° C, followed by annealing at 350° C in O_2 ambient. After that, the W gate electrode was formed by sputtering. The TiN gate was also used in comparison. Consequently, three types of gate stacks, TiN/Al_2O_3, W/Al_2O_3 and W/HfO_2/Al_2O_3, were prepared and compared. Finally, the Ni source was formed and post metallization annealing (PMA) was carried out in N_2 ambient for all samples.

III. RESULTS AND DISCUSSION

First, we evaluated the gate stack quality from capacitance voltage (*C-V*) characteristics, as shown in Fig. 3. The bilayer TFET devices after PMA were used also for this *C-V* measurement, where the source and drain were grounded and the gate bias was controlled. The importance

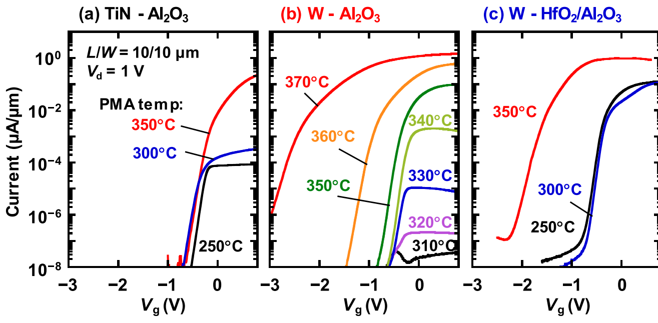

FIGURE 4. I_d-V_g characteristics of bilayer TFETs with (a) TiN/Al_2O_3, (b) W/Al_2O_3, and (c) W/HfO_2/Al_2O_3 gate stacks after PMA at various temperatures.

of PMA temperature (T_{PMA}) optimization will be introduced later in detail. In the control TiN/Al_2O_3 gate stack, large counter-clockwise hysteresis is observed. The existence of any mobile ions in gate insulator and/or ZnSnO channel layer [27], [28] or hole injection from gate electrode into the gate insulator [29] are suggested. This hysteresis is drastically reduced by using the W gate for both Al_2O_3 and HfO_2/Al_2O_3 samples, indicating the superiority of the W gate. The hysteresis voltage widths (V_{hys}) of the TiN/Al_2O_3, W/Al_2O_3 and W/HfO_2/Al_2O_3 gate stacks are 560, 29, and 113 mV, respectively, even for the 3-time higher maximum capacitance of W/HfO_2/Al_2O_3. Here, the capacitance equivalent thicknesses (CET) are 5.5, 5.9, and 2.3 nm for the TiN/Al_2O_3, W/Al_2O_3 and W/HfO_2/Al_2O_3 gate stacks, respectively. Also we have confirmed from TCAD simulation [30] that relatively-thick channels and gate oxides hardly degrade the minimum *SS* value of 1-2 mV/dec [18].

Second, we have carefully investigated the impact of T_{PMA} for each sample. Figures 4(a)-4(c) show the drain current (I_d) - gate voltage (V_g) characteristics of the bilayer TFET with the three different gate stacks, after PMA at various temperatures in a range from 250 to 370° C. It can be observed that the impacts of T_{PMA} on the electrical characteristics of TFETs such as I_{ON} and sub-threshold characteristics are largely different among the three different gate stacks.

Figs. 5(a) and 5(b) show the changes in I_{ON} and the maximum I_d ratio over a V_g swing of 0.3 V, respectively, as a function of T_{PMA}. Here, the maximum I_d ratio over the V_g swing of 0.3 V denotes the steepness of I_d in the sub-threshold region. Also, I_{ON} is defined as I_d at V_g of 0.8 V for all the gate stacks. Generally, T_{PMA} increases I_{ON} for all the gate stacks. Here, the T_{PMA} dependence of I_{ON} is largest for the W/Al_2O_3 gate stacks. Also, the threshold voltage shifts toward the negative V_g side with increasing T_{PMA}, as shown in Fig. 4. One possible reason to cause these two changes is the increase in electron concentrations in the n-type ZnSnO channel layers and the resulting increase in channel conductivity. It is known that oxygen interstitials form deep-level traps in Zn-based oxides [31]–[33], which reduce the electron concentration. Thus, the reduction in the oxygen concentration due to oxygen subtraction by the gate

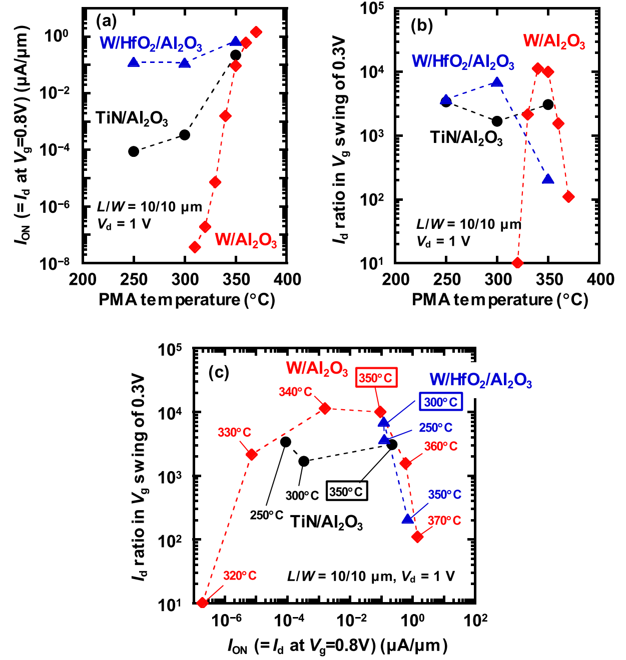

FIGURE 5. (a) I_{ON} (defined as I_d at V_g of 0.8 V) and (b) maximum I_d ratio at V_g swing of 0.3 V as a function of T_{PMA}, respectively. (c) relationship between I_{ON} and the maximum I_d ratio. The optimal T_{PMA} for each sample with realizing relatively high I_{ON} and I_d ratio is surrounded by rectangle.

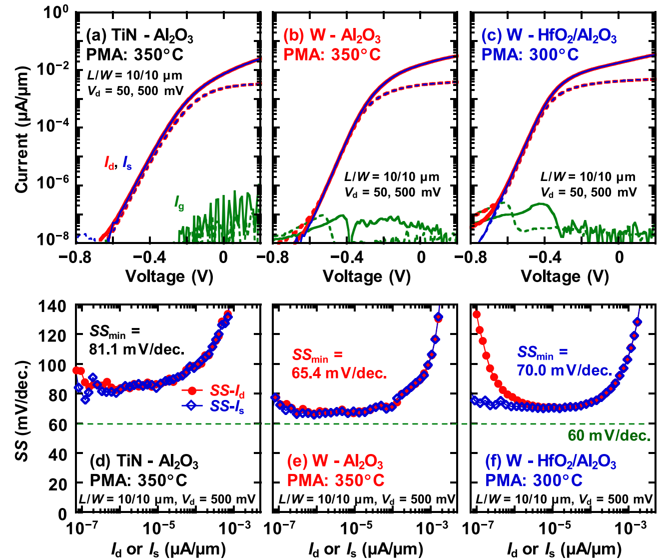

FIGURE 6. [(a)-(c)] I_d-V_g characteristics, and [(d)-(f)] *SS*-I_d and *SS*-I_s characteristics of ZnSnO/Si bilayer TFET measured at room temperature. Single V_g sweep was from positive to negative. Gate stacks are [(a),(d)] TiN/Al_2O_3, [(b),(e)] W/Al_2O_3, and [(c),(f)] W/HfO_2/Al_2O_3, respectively. The SS_{min} value was extracted from *SS*-I_d characteristics.

metal during PMA could effectively increase the electron carrier concentration in the ZnSnO channels. Here, different gate metals and high-*k* gate insulators could modulate oxygen subtraction and oxygen diffusivity in the insulators, leading to the different sensitivity of T_{PMA} on I_d. Further studies are still needed to understand the physical reason.

In contrast, the T_{PMA} dependence of the I_d ratio in the V_g swing of 0.3 V is more complicated. The I_d ratio is almost flat for the TiN/Al_2O_3 gate stack. On the other hand, the T_{PMA} dependence of the I_d ratio of the W/Al_2O_3 gate stack has a very narrow peak at T_{PMA} of around 340-350° C. The I_d ratio of the W/HfO_2/Al_2O_3 also has a wider peak at 300° C, and the I_d ratio drops at T_{PMA} higher than 300° C.

The relationship between I_{ON} and the maximum I_d ratio is plotted in Fig. 5(c) in order to find the optimum T_{PMA}. It can be judged that 350, 350, and 300° C is the best T_{PMA} for the TiN/Al_2O_3, W/Al_2O_3, and the W/HfO_2/Al_2O_3 gate stacks, respectively, in terms of high I_{ON}, high I_d ratio and the resulting steep sub-threshold characteristics. It is observed, on the other hand, that the I_{ON} level at the optimal T_{PMA} is in the same level among all the samples, suggesting that ZnSnO channel quality with the different gate stacks is similar at the optimum T_{PMA}.

Next, the sub-threshold characteristics of the fabricated three bilayer TFETs after PMA at the optimal T_{PMA} are quantitatively evaluated. Figures 6(a)–6(c) show the I_d-V_g characteristics of the ZnSnO/Si bilayer TFETs with the three different gate stacks measured at room temperature. Also, Figs. 6(d)-6(f) show the corresponding *SS*-I_s and *SS*-I_d characteristics. The minimum *SS* value (SS_{min}) of 65.4 mV/dec. has been realized in the TFET with the W/Al_2O_3 gate stack. This is the lowest value obtained in n-OS/p-IV bilayer TFETs so far. Also, this low *SS* value is realized in a wide I_d range of approximately three orders. Here, there is almost no difference between *SS* values estimated from I_d and I_s over the wide current range, because the gate leakage current (I_g) of the W/Al_2O_3 gate stack is sufficiently low. The low I_{OFF} of 1×10^{-8} μA/μm and the large I_{ON}/I_{OFF} of 3×10^6 are very attractive as a steep-slope transistor. It is also found that the present W/Al_2O_3 TFET can realize the almost hysteresis-free sub-threshold characteristics with drain voltage (V_d) from 50 mV to 1 V and the well-behaved output characteristics, as shown in Figs. 7(a) and 7(b), respectively. On the other hand, SS_{min} of 70.0 mV/dec. in the W/HfO_2/Al_2O_3 TFET is a little higher than that in the W/Al_2O_3 one, although the CET value of W/HfO_2/Al_2O_3 is roughly 1/3. Additionally, in the I_d region lower than 10^{-6} μA/μm, *SS* estimated from I_d is higher than that from I_s, attributed to higher I_g of the W/HfO_2/Al_2O_3 gate stack in this region.

These results indicate that the sub-threshold characteristics of the ZnSnO/Si bilayer TFET is very sensitive to the choice of the gate stack materials, even at the optimum T_{PMA}. As discussed in the previous paragraph, the film quality of the ZnSnO channel layers could be comparable among all the samples at the optimum T_{PMA}. These facts indicate that the change in the *SS* values of the TFETs could originate from the defect density at the high-*k*/ZnSnO interface and that the interfacial structure is not the same among the different gate insulators and the gate metals. Such a difference in the interfacial defect density could be caused by any interfacial chemical reactions during deposition processes of gate insulators and/or gate metals with different chemical characteristics.

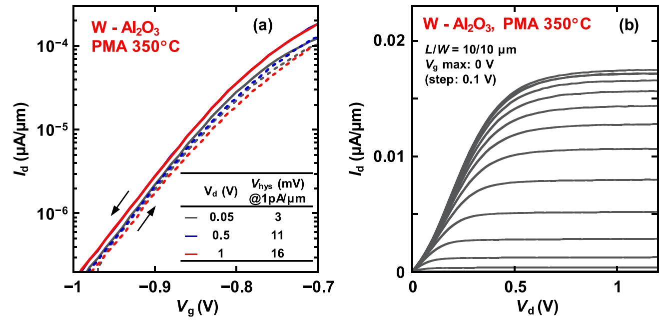

FIGURE 7. (a) Double sweep I_d-V_g characteristics with various V_d and (b) I_d-V_d characteristics of ZnSnO/Si bilayer TFET with W/Al_2O_3 gate stack measured at room temperature.

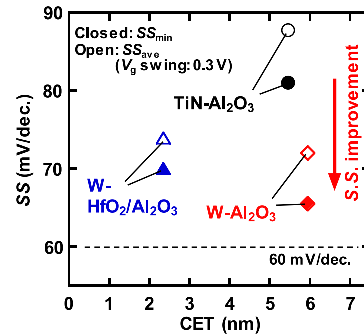

FIGURE 8. Relationship between CET and *SS* of ZnSnO/Si bilayer TFET with various gate stacks.

Finally, the impacts of the present gate metals and gate insulators are summarized. Figure 8 shows the relationship between CET and minimum/average *SS* values. A V_g swing of 0.3 V was assumed to estimate the average SS value (SS_{ave}). The W/Al_2O_3 gate is the most effective for improvement of not only SS_{min} but also SS_{ave} of the ZnSnO/Si TFET. SS_{min} and SS_{ave} of 65.4 and 72.0 mV/dec., respectively, have been achieved. These values are 19% and 18% lower than those of the TFET with the control TiN/Al_2O_3 gate stack. In addition to the steep sub-threshold characteristics, the hysteresis-free characteristics of this W/Al_2O_3/ZnSnO/Si bilayer TFET are attractive for low-power switching devices. On the other hand, the SiO_2 interfacial layer formed at the ZnSnO/Si interface [20] may limit the I_{ON} for all the TFETs, hence further process developments for suppressing the formation of the interfacial layers are expected to improve the TFET performances.

IV. CONCLUSION

We examined the impact of the gate insulator and the gate electrode on the sub-threshold characteristics of the ZnSnO/Si bilayer TFETs. In order to realize both high I_{ON} and steep ON/OFF switching, the careful optimization of T_{PMA} is essential and the optimization temperature is not the same for all the gate stacks. After this optimization, the W/Al_2O_3 gate stack has been found to realize the hysteresis-free I_d-V_g characteristics with SS_{min} of 65.4 mV/dec. and SS_{ave} of 72.0 mV/dec. over a V_g swing

of 0.3 V. As a result, the reduction in both SS_{min} and SS_{ave} by approximately 20% has been realized in the W/Al_2O_3 gate stack in comparison with the control TiN/Al_2O_3 gate stack. The present result has revealed that the improvement of the gate stack quality is more effective in realizing both low SS and low I_{OFF} than EOT scaling.

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