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Traps Around Ge Schottky Junction Interface: Quantitative Characterization and Impact on the Electrical Properties of Ge MOS Devices

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ABSTRACT This paper proposes and develops a new technique based on low temperature conductance method to quantitatively evaluate the trap densities around NiGe/Ge Schottky junction interface and their time constants. It is found that the Schottky barrier height (SBH) in the NiGe/Ge junction is related with these junction traps. Additionally, the traps around junction interface could strongly affect the electrical properties of Ge MOSFETs, especially the OFF-state currents.

INDEX TERMS Germanium, Schottky junction, traps around junction interface, low temperature conductance method.

I. INTRODUCTION

Ge has been attracting a lot of interests as the channel material for future CMOS technology, owing to its high bulk mobility [1]. Much attentions have been focused on the research of the Ge MOS interface and its impact on device performance [2]–[6]. However, the problem for Ge junctions is still lack of mechanism study. In general, the electrical properties of both conventional p-n junctions and Schottky junctions are susceptible to the degradation of junction interface quality. It is mainly due to the existence of impurity energy levels induced by the traps around junction interface, which gives rise to the birth of generation-recombination (G-R) centers [7]. The generation current via G-R centers could cause a deviation of the junction electrical property from the ideal when the junction is reversely biased. This component of junction leakage currents is strongly dependent on the electric field intensity. It may deteriorate the OFF-state performance of short-channel devices, because the high electric fields can be expected in short-channel devices, owing to the high substrate-doping levels typically used to control the short channel effects (SCE) [8]. Nevertheless, the generation current in the depletion region is less dominant for Ge junctions, especially for the Ge junctions with deep-level G-R centers [7], [9], [10]. The currents derived from the transition of electrons from the valence to the conduction band through these deep-level G-R centers, which is called trap assisted tunneling (TAT) current, become more important in the source and drain (S/D) junctions of Ge devices [9], [10]. These TAT currents are introduced by traps around junction interface, and strongly electric field dependent. Therefore, this component current would be especially remarkable in the Ge junctions due to the small bandgap (E_g) of Ge. As shown in Fig. 1, these junction traps induced TAT current is an important part of the gate induced drain leakage (GIDL) in the Ge MOSFET, which could result in the severe degradation for the OFF-state behaviors with downscaling the equivalent oxide thickness (EOT) [11], [12]. On the other hand, in Ge TFETs, the TAT currents would also significantly deteriorate the subthreshold characteristics by shielding the band-to-band tunneling (BTBT) currents [13]. These raised concerns may counteract the advantages of Ge in the application of device fabrication.

In order to overcome these limitations in Ge devices, the properties of traps around junction interface and their impacts on device performance should be investigated elaborately. It is well known that the formation of the highly doped Ge S/D

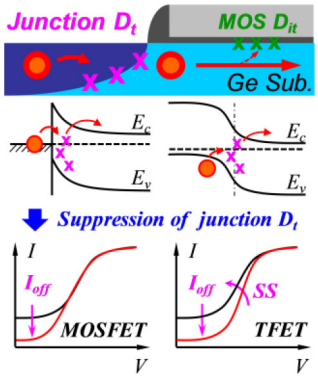

FIGURE 1. The schematic diagram of traps around Ge junction interface and their impacts on device performance.

junctions by using the traditional ion implantation technique is difficult, attributable to the low solubility and large diffusion coefficient of dopants in Ge [14], [15]. Alternatively, the metal/Ge Schottky junctions have been proposed for the fabrication of Ge MOSFETs due to the advantages of atomically sharp interface and extremely low resistance reported in the previous studies [16], [17]. Although the Ge Schottky junction is immune to the implantation damage induced junction traps, the metal induced gap states (MIGSs) are common around the metal/Ge interface. These MIGSs, which can be considered as traps around junction interface, could not only control the Schottky barrier height (SBH) but also introduce the TAT currents [18]. According to the research results by [19], [20], the strong Fermi level pinning (FLP) derived from MIGSs is always close to the valance band edge of Ge and blocks the formation of Ge Schottky junctions with large SBHs for both electron and hole. Therefore, the comprehensive understanding of these junction traps, especially in the Ge Schottky junction, is of great importance.

Several characterization techniques have been proposed for the quantitative estimation of traps around the metal/semiconductor interface [20]–[24]. Cowley and Sze [21] and Nishimura *et al.* [20] calculated the junction interface traps by using the relationship between SBH and metal work function when various kinds of metals are deposited on the semiconductor substrate. This method can only give the trap density information around the position of Fermi level pinning at junction interface. Considering the energy distribution, the C-V technique has been used to measure the density distribution of interface traps [22]–[24]. The difference of capacitive responses between low and high frequencies can be used to extract the Schottky junction interface trap density. However, this measurement technique may mislead the result by imperfect back-contacts and minority-carrier injection [18], [25]. To take the issue into account, this paper proposes and develops a new technique based on conventional low temperature conductance method to quantitatively evaluate the energy distribution of trap densities around the NiGe/Ge Schottky junction interface (D_t) and their time constants (τ). It can effectively avoid the influence from the minority carrier effect, because the measurement is always performed when the junction is in depletion and there is no minority carriers from the bulk semiconductor in this situation [26]. Through the characterizations of D_t distribution and the fast I-V measurements, it is confirmed that the SBHs in the NiGe/Ge junctions are related with D_t, and both D_t and τ strongly affect the OFF-state characteristics of Ge MOSFETs.

This paper is organized as follows: after a description of the fabrication process and the characterization technique for traps around Schottky junction interface in Section II, the detailed procedure is given by extracting the D_t and τ distribution of a NiGe/n-Ge junction in Section III-A. The validity of this technique is demonstrated by the impacts of D_t and τ on the performance of Ge MOSFETs with different NiGe S/D junctions in Sections III-B and III-C, respectively. Finally, conclusions are given in Section IV.

II. EXPERIMENTS AND MEASUREMENTS

A. JUNCTION AND DEVICE FABRICATION

After RCA cleaning of the n-Ge substrate ($N_D = \sim 7 \times 10^{14}$ cm^{-3}), active area was patterned and evaporated nickel (~30 nm) was deposited. The NiGe/n-Ge Schottky junction was subsequently formed by annealing at 400° C in the N_2 atmosphere for 5 min. This junction is selected as the control sample to expound the D_t and τ extraction technique proposed in this study. Another three sets of NiGe/n-Ge Schottky junctions and their corresponding Ge MOSFETs with NiGe S/D are utilized to demonstrate the validity of this characterization technique. Similar junction process was performed, except the annealing condition. The rapid thermal annealing (RTA) of 200, 300 and 400° C in the N_2 atmosphere for 1 min were used for the fabrication of three different junctions, respectively. These junctions featuring different leakage currents are used to investigate the relationship between D_t and SBHs. Ge pMOSFETs with these S/D junctions were also achieved by gate-first process. Following pre-cleaning of Ge wafer and definition of active area, the Al_2O_3 (5 nm)/GeO_x (~1 nm) gate stack was deposited by atomic layer deposition (ALD) and in-situ ozone post oxidation (OPO) at 300° C [2]. The metallic NiGe S/D were formed by the same annealing conditions mentioned above. These Ge pMOSFETs with metallic NiGe S/D are for the feasibility demonstration of this characterization technique.

B. MEASUREMENT SETUP AND PRINCIPLE

Figure 2(a) shows the measurement setup of this characterization technique for traps around junction interface. The Schottky junction is reversely biased with the voltage of V_r at low temperature. A series of sine waves with different frequencies ranging from 1 kHz to 1 MHz and the same amplitude of 20 mV were added on the V_r. Finally, the functions of depletion capacitance (C_d) and parallel conductance (G_p) in the NiGe/n-Ge junction as the changing frequencies

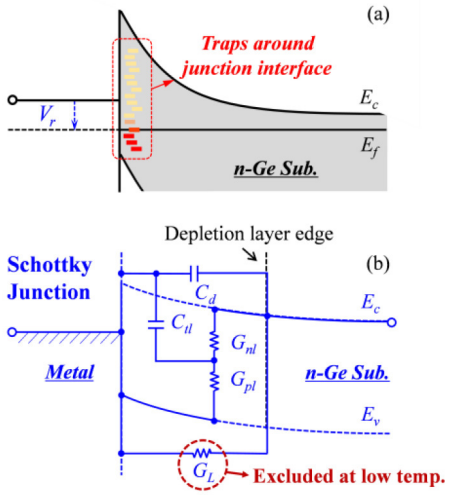

FIGURE 2. **(a) Measurement configuration for the characterization of traps around metal/n-Ge Schottky junction interface; (b) band diagram of the metal/n-Ge Schottky junction and the corresponding equivalent circuit with single energy level traps.**

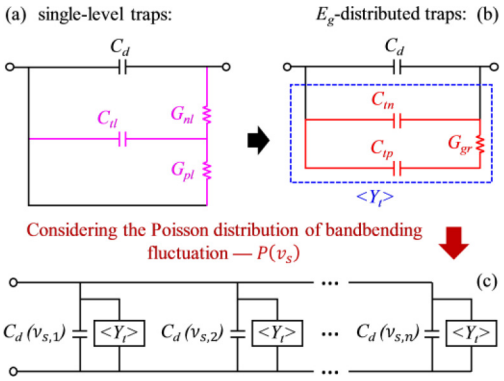

FIGURE 3. **The equivalent circuits of a Schottky junction with single-level traps (a), with a distribution of single-level traps (b), and with the consideration of band bending fluctuation (c).**

could be measured at a certain voltage, which are used for the quantitative extraction of D_t and τ. Typically, the measured D_t should include the traps within depletion region, including interface and near-interface traps, according to the conductance method's principle. However, due to the direct contact of semiconductor with metal, most interface trap response may be screened by electrons from the metal. Therefore, near-interface traps will be dominant in the measurement result.

Figure 2(b) presents the detailed measurement principle, which are similar with the traditional conductance method for extraction of MOS interface traps [26], [27]. This schematic diagram shows the band diagram of a reversely biased NiGe/n-Ge junction and the corresponding equivalent circuit contributed by single-level traps. Here, the traps are marked not exactly at the junction interface in Fig. 2(b), suggesting that near-interface traps are mainly measured. However, compared with that for a MOS capacitor [26], there is no oxide capacitance (C_{ox}) but the leakage conductance (G_L) in the equivalent circuit. The G_L is derived from the carrier thermal injection induced junction leakage currents. It may shield the conductance of traps, which is the same as the case for the conductance measurement in the MOS structure with extremely thin EOT [26]. Fortunately, these junction leakage currents are strongly temperature dependent and could be completely suppressed at low temperature. Therefore, the G_L can be excluded at low temperature and the equivalent circuit becomes that shown in Fig. 3(a). This equivalent circuit is related to the measured admittance from the conductance method [26], where C_{tl} is the capacitance for a certain level trap, and G_{nl}^{-1} and G_{pl}^{-1} are the electron and hole capture resistances by traps, and the l-value is the index of each trap level. This equivalent circuit is the same with that for a MOS capacitor, which means the low temperature conductance method is also applicable for the characterization of traps around Schottky junction interface.

Nevertheless, single-level traps are not observed in reality. What is observed are many trap levels so closely spaced in energy over the Ge E_g that they cannot be distinguished in the measurements as separate levels. Consequently, the equivalent circuit of the Schottky junction with a distribution of trap levels can be obtained by parallelly combining branch circuits of single-level traps. After simplifying this parallel circuit by a $Y-\Delta$ transformation, the equivalent circuit in Fig. 3(a) for single-level traps becomes the equivalent circuit in Fig. 3(b) for a distribution of trap levels, where G_{gr} is the G-R conductance caused by the interaction between traps and carriers, and C_{tn} and C_{tp} are G-R capacitances for electron and hole. Here, G_{gr}, C_{tn} and C_{tp} can be all expressed as the function of the trap capacitance (C_t), τ and the angular frequency (ω), which is similar as the situation for a MOS capacitor and described in detail in [26]. The $<Y_t>$ in Fig. 3(b) represents the total admittance of traps around junction interface. Therefore, the admittance for conductance measurement in the reversely biased Schottky junction can be defined to be

$$Y_s = j\omega C_p + G_p \tag{1}$$

with

$$C_p = C_d + C_t(\omega\tau)^{-1}tan^{-1}(\omega\tau) \tag{2}$$

$$\frac{G_p}{\omega} = C_t(2\omega\tau)^{-1}\ln\left[1+(\omega\tau)^2\right] \tag{3}$$

where C_t is equal to qD_t, and ω is proportional to the measurement frequency (f). And τ is labeled as τ_n and τ_p for the capture time of electron and hole, respectively. Here,

$$\tau_n = \frac{1}{c_n N_d}\exp(-v_s) \tag{4}$$

$$\tau_p = \frac{1}{c_p N_a}\exp(v_s) \tag{5}$$

where c_n and c_p are the electron and hole capture probabilities, and N_d and N_a are the donor and acceptor densities, and v_s is the energy band bending at the junction interface.

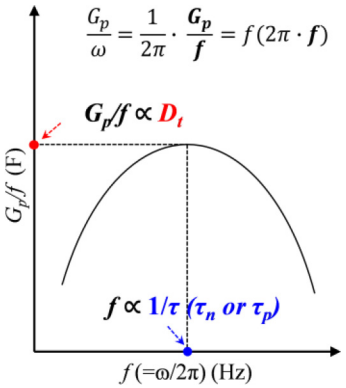

FIGURE 4. An example of the conductance curve for Schottky junctions for D_t and τ extraction.

However, a random distribution of discrete charges at the NiGe/Ge interface makes the situation become complicated and causes a deviation of this model from the ideal. This phenomenon results in the localized charge nonuniformities and the band bending fluctuation over the interfacial plane. It can be treated by considering the Gaussian distribution of band bending fluctuation ($P(\upsilon_s)$), as shown in Fig. 3(c). The whole junction area can be divided into patches with different band bending, which are described as parallel branches of C_d and $<Y_{it}>$ in the circuit. The symbol, $\upsilon_{s,n}$, distinguishes these different patches with each other. Finally, the conductive response of traps around Schottky junction interface becomes

$$\frac{G_p}{\omega} = \int_{-\infty}^{+\infty} C_t (2\omega\tau)^{-1} \ln\left[1 + (\omega\tau)^2\right] P(\upsilon_s) d\upsilon_s \qquad (6)$$

with

$$P(\upsilon_s) = (2\pi\sigma_s^2)^{-1/2} \exp\left[-\frac{(\upsilon_s - \overline{\upsilon_s})^2}{2\sigma_s^2}\right] \qquad (7)$$

where σ_s^2 is the variance of band bending, and $\overline{\upsilon_s}$ is the mean value of band bending. According to Equations (6) and (7), there are two steps needed to obtain the D_t and τ as a functions of Ge defect energy level by the low temperature conductance method. Step 1 is measuring the junction conductance as functions of frequency and bias voltage and extracting the D_t and τ as a function of bias voltage by fitting with the theoretical model of Equation (6). Step 2 is measuring a $C-f$ curve as a function of bias voltage to extract the junction interface υ_s as a function of bias voltage. Figure 4 shows a typical curve of G_p/f versus log frequency at the fixed V_r in the step 1 of this procedure. As depicted in this schematic diagram, the peak of G_p/f gives the information of D_t at one trap level, while the corresponding frequency provides the information of τ (τ_n or τ_p). In the step 2, the junction interface υ_s is determined by its mathematical relationship with the measured junction capacitance, C_p [7], where C_p is approximately equal to C_d when the frequency is high enough. Combining these two steps, the trap properties around Schottky junction interface (D_t and τ) as a function of energy within E_g can be quantitatively extracted by using the low temperature conductance method.

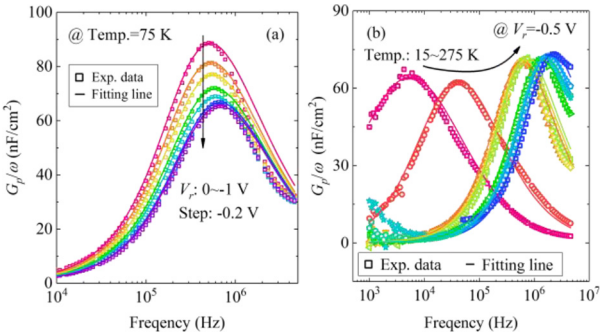

FIGURE 5. Experimental data and fitting results of the conductance curve taken from a NiGe/Ge Schottky junction at different V_r (a) and different temperatures (b).

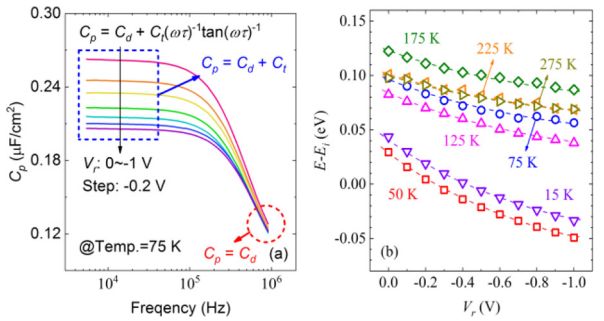

FIGURE 6. (a) Capacitance measurement of the reversely biased Schottky junction at 75 K; (b) The E-E_i distribution as the changing V_r at different temperatures calculated from the measured C_p.

III. THE CHARACTERIZATION FOR PROPERTIES OF TRAP AROUND JUNCTION INTERFACE

A. MEASUREMENT RESULTS

Figures 5(a) and (b) plot the measurement results of G_p/ω as a function of log frequency at different biases and temperatures, respectively, for the control sample. It is found that the G_p/ω peaks measured at 75 K exhibit decreased peak values with the increased V_r. Meanwhile, the peak frequency values measured at the V_r of -0.5 V increase with increasing the measurement temperature. These experimental data match very well with the theoretically calculated fitting lines from Equation (6), which is favorable for the extraction of D_t and τ. This phenomenon also indicates the availability of this technique for trap characterization around Schottky junction interface. Figure 6(a) shows a set of C_p-f curves as a function of V_r at 75 K. It is observed that, at low frequency, traps around junction interface immediately change occupancy in response to the ac voltage. Then, from Equation (2), $C_p = C_d + C_{it}$. As the frequency increases, these traps no longer change occupancy immediately in response to the ac voltage, but lag behind. Then C_p decreases with increasing frequency until, at very large values of frequency, trap occupancy changes very little in response to the ac voltage, that is, $C_p = C_d$. According to this principle, the energy level

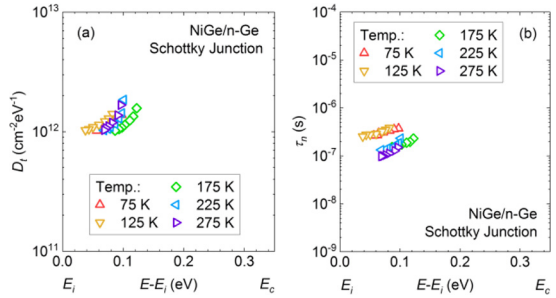

FIGURE 7. The energy distribution of D_t (a) and τ (b) in a NiGe/nGe Schottky junction.

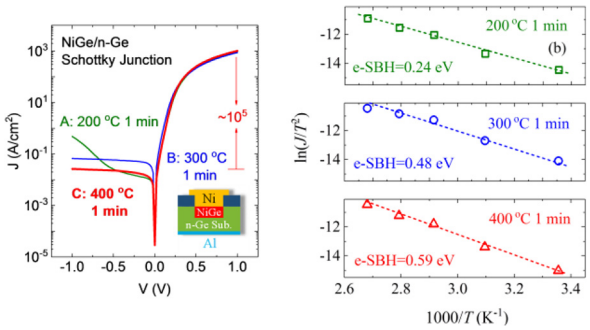

FIGURE 8. The normal electrical properties of the NiGe/n-Ge Schottky junctions formed by different RTA conditions, including *J-V* curves (a) and SBHs for electron (b).

distribution at different V_r and temperature can be deduced by the relationship between $\upsilon_s$and C_p at a high frequency, as shown in Fig. 6(b). The C_p-f measurement at different temperatures facilitates the energy distribution extension of E-E_i from -0.05 to 0.13 eV, due to the variation of E_c and E_v in Ge with the changing temperature. Finally, integrating the measurement results in Figs. 5 and 6, the D_t and τ distribution across E_g in the NiGe/n-Ge Schottky junction were successfully characterized and presented in Figs. 7(a) and (b), respectively. It is found that deeper energy level corresponds to smaller D_t, which is similar with the interface trap distribution for a MOS capacitor. The D_t for the NiGe/n-Ge junction with the electron SBH (e-SBH) of 0.3 eV is $\sim 10^{12}$ cm^{-2}eV^{-1}. This value is much smaller than that measured around the charge neutral level (CNL) reported in [20]. It may be because most of junction interface traps, which are screened by direct metal contact, cannot be detected by the conductance method. The τ_n of $\sim 10^{-7}$ s suggests that the carrier transportation in the reversely biased NiGe/n-Ge junction can be free of trapping effect if the measurement speed is up to 10 Mhz, and the junction leakage currents by G-R centers, especially for the TAT component, can be sufficiently suppressed.

B. DEMONSTRATION OF THE VALIDITY FOR D_T EXTRACTION

In order to verify the feasibility of this technique, the D_t distributions across Ge E_g for junctions with different annealing processes were quantitatively extracted. Figures 8(a) and (b) present the normal electrical properties of these NiGe/n-Ge junctions. It is found in Fig. 8(a) that the junction formed by RTA at 400° C for 1 min exhibits the significantly suppressed junction leakage currents compared with the other junctions, and an ON/OFF ratio of $\sim 10^5$. The e-SBHs of these junctions are evaluated from the reverse bias currents taken at different temperatures, using the Arrhenius plot method [28], as shown in Fig. 8(b). Considering the barrier lowering induced SBH reduction, a small voltage ($V_r = -0.5$) was selected for the extraction of SBHs. Several smaller voltages were also examined to eliminate this error. According to the band alignment between NiGe and Ge [29], the ideal contact of NiGe/n-Ge should be a Schottky junction with e-SBH of $\sim$1 eV. However, the significant linear $ln(J/T^2)$-$(1/T)$ relationships reveal the e-SBHs of 0.24 and 0.48 eV for the junctions fabricated by 1-min RTA at 200 and 300° C, respectively, attributable to the FLP caused by MIGSs. On the other hand, the junction processed by RTA of 400° C for 1 min shows an e-SBH of 0.59 eV, which is due to the reduced FLP by suppression of MIGSs at this annealing condition. These phenomena indicate that the FLP is expected to be caused by the thermal reaction generated traps around junction interface. To further understand the relationship between these traps and the Schottky junction performance, the D_t distributions of these junctions are measured and shown in Fig. 9(a). It is obvious that the D_t of $\sim 3 \times 10^{12}$ cm^{-2}eV^{-1} is revealed for the junction formed by RTA at 200° C for 1 min, which is larger than those of other junctions by nearly one order of magnitude. It can be ascribed to the less crystallization of NiGe grains at low temperature, introducing much more grain and grain boundary traps, and thus the increased D_t [30], [31]. For the junctions fabricated by RTA of 300 and 400° C for 1 min, the D_t, distributed around E_f, is much lower while the electrical properties are better behaved, suggesting that the reduced D_t is responsible for the superior junction performance. This relationship illustrates a great dependence of FLP effect upon the traps around Ge Schottky junction interface. Figure 9(b) summarizes the D_t at E_f of these NiGe/n-Ge Schottky junctions with different SBHs. It is found that a lower D_t at E_f

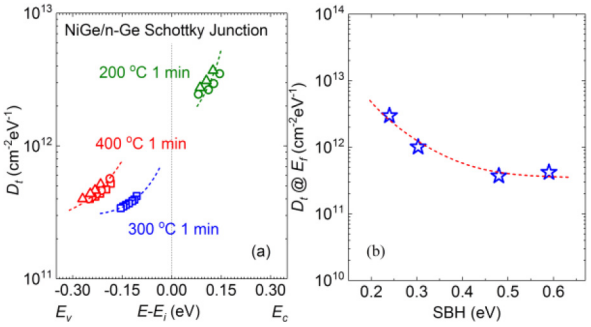

FIGURE 9. (a) D_t of the NiGe/n-Ge Schottky junctions fabricated by using different RTA temperature; (b) the function of the D_t at E_f for different NiGe/n-Ge Schottky junctions as their varying SBHs.

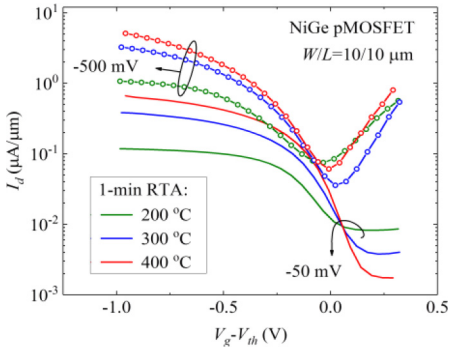

FIGURE 10. The $I_d - V_g$ curves of Ge pMOSFETs fabricated with different NiGe S/D junctions.

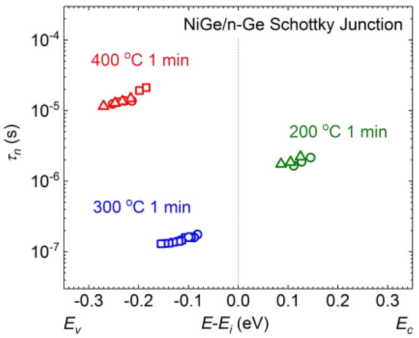

FIGURE 11. The τ_n distribution across the E_g of Ge for the NiGe/n-Ge schottky junctions fabricated by using different RTA conditions.

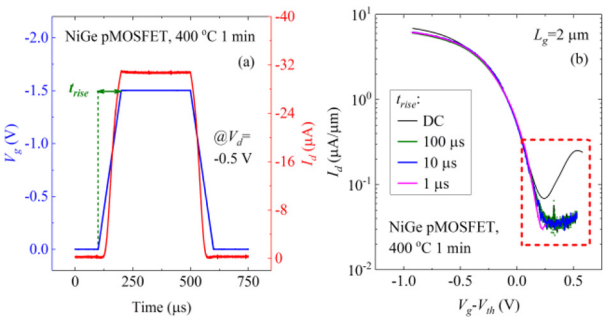

FIGURE 12. (a) The waveforms for the applied V_g and measured I_d traced by SPIV method using Agilent B1530; (b) The $I_d - V_g$ curves of the 400° C NiGe S/D pMOSFET with t_{rise} ranging from 100 μs to 1 μs.

contributes a larger SBH, which is coincide with the phenomenon of MIGSs reduction induced FLP alleviation [32]. This result provides the experimental support for FLP effect in Ge Schottky junction. The accordance with theoretical understanding also reveals the feasibility of low temperature conductance method for the characterization of traps around Schottky junction interface. Here, the D_t in the junctions formed at 300 and 400° C are almost the same. It may be because these measured traps are both caused more by the intrinsic property of bulk Ge. The impact of D_t distribution on device performance is also investigated to further demonstrate the validity of this technique. The normal electrical properties, I_d-V_g, of Ge MOSFETs by using the above junctions are presented in Fig. 10. It is found that the NiGe S/D junctions with reduced D_t facilitate the suppression of OFF-state currents at $V_d = -50$ mV in Ge MOSFETs, thanks to the enhancement of e-SBH and the alleviation of TAT [33], [34]. Whereas, for the case at $V_d = -500$ mV, the difference of the leakage currents for these three devices becomes smaller. It is because that the BTBT induced GIDL currents begin to dominate in the OFF-state as increasing the voltage from gate to drain [33]. Therefore, as the downing scaling of the supply voltage (V_{dd}) for the application with low power consumption, the impact of traps around junction interface on the OFF-state performance will become more and more important in Ge MOSFETs [35]. Here, the boost of ON-state currents in Fig. 10 can be attributed to the increased e-SBH, since the SBH of hole (h-SBH) is decreased, and thus the contact resistance is lowered when Ge pMOSFET is turn on. And also, the MOS interface quality and the subthreshold swing (SS) behavior are improved by the high temperature annealing of NiGe formation after gate stake formation. This junction trap characterization method could provide a guideline for the future junction formation technique in the Ge devices. However, only a portion of traps around junction interface (near-interface traps mostly) are measured from the conductance method although still indicating some reasonable trends. Comprehensive estimation of junction interface traps should be further investigated.

C. VERIFICATION OF THE τ-DEPENDENCE FOR TRAPS AROUND JUNCTION INTERFACE

Figure 11 shows the measured τ_n of these different NiGe/n-Ge junctions. It is normally observed that the τ_n becomes larger when is larger (i.e., $E - E_i$ gets closer to E_v) for the junctions formed at 300 and 400° C. However, the τ_n of the junction formed at 200° C shows a slightly larger value. One possible reason is the different spatial position of these measured traps. Since the conductance method will include all the trap response within the depletion region, the traps in the junctions formed at 300 and 400° C may be located far more than those in the junction formed at 200° C. Therefore, $E - E_i$ may be further to E_v for the traps in the junction formed at 200° C, thus higher capture time constant. These traps located near the interface are more likely to be caused by the disorder-induced interface states. Due to higher D_t in the junction formed at 200° C, as shown in Fig. 9(a), traps closed to junction interface are much easier to be detected. Fast I-V measurements are carried out for the verification of τ-dependence in these junction traps. The $I_d - V_g$ curves of the Ge MOSFET using different measurement speeds were successfully extracted at $V_d = -500$ mV. Figure 12(a) gives an example of the fast I-V measurement by using the commercial semiconductor parameter analyzer for the 400° C NiGe pMOSFET: the V_g waveform was applied with the rise time (t_{rise}) of 100 μs and the measured I_d was traced by single pulsed I-V (SPIV) method. Figure 12(b) shows

that trapping free characteristics are obtained when measuring from DC to 1 μs. On one hand, the difference with SS behaviors at different measurement speeds is neglectable due to the well-passivated MOS interface by OPO [2]. On the other hand, the TAT currents are significantly suppressed with the suppression of junction traps under the fast I-V measurement, resulting in the decreased OFF-state currents. Therefore, it is necessary to introduce the suitable junction formation technique for the fabrication of devices with less junction traps in the future application of Ge MOSFETs. Furthermore, this measurement result also indicates the credible evaluation of traps around Shottky junction interface by using the low temperature conductance method.

IV. CONCLUSION

In this study, the low temperature conductance method has been applied for the extraction of traps around Ge Schottky junction interface. The densities of these traps (D_t) and their time constants (τ) distributed over the bandgap of Ge were quantitatively characterized by using this technique. It has been confirmed that the Schottky barrier heights (SBHs) of Ge Schottky junctions are related with traps around junction interface. This phenomenon conforms well to the Fermi level pinning (FLP) effect, which is caused by metal induced gap states (MIGSs). With the suppression of these junction traps, the OFF-state currents in Ge MOSFETs with NiGe S/D could be obviously reduced due to the enhancement of SBHs and the elimination of trap assisted tunneling (TAT) currents. Therefore, the junction interface engineering should be of great importance for realizing high performance Ge MOSFETs, especially at the technology node of sub-10 nm.

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