Received 26 February 2020; accepted 8 March 2020. Date of publication 18 March 2020; date of current version 7 April 2020.
The review of this paper was arranged by Editor C. C. McAndrew.

Digital Object Identifier 10.1109/JEDS.2020.2981607

Effect of Substrate Choice on Transient Performance of Lateral GaN FETs

MICHAEL R. HONTZ [1,2] (Member, IEEE), RONGMING CHU [3,4] (Senior Member, IEEE), AND RAGHAV KHANNA [1] (Member, IEEE)

1 Department of Electrical Engineering and Computer Science, University of Toledo, Toledo, OH 43606, USA
2 Automation and Controls Research and Development, Naval Surface Warfare Center Philadelphia Division, Philadelphia, PA 19112, USA
3 Microelectronics Laboratory, HRL Laboratories, Malibu, CA 90265, USA
4 Electrical Engineering and Computer Science Department, Pennsylvania State University, State College, PA 16802, USA

CORRESPONDING AUTHOR: M. R. HONTZ (e-mail: michael.r.hontz1@navy.mil)

This work was supported in part by the U.S. Office of Naval Research under Grant N00014-18-1-2676 and was approved for public release under DCN#43-6352-20.

ABSTRACT This brief presents a study on the effect of substrate choice on the performance of lateral GaN transistors. This is accomplished using a previously calibrated TCAD model of the device which was used to investigate the effect of substrate choice on capacitance-voltage characteristics of the device. It is shown in simulation that C_{GD} and C_{DS} have a demonstrable dependence on substrate selection and is consistent with expectations regarding the substrate materials conductivity. The device model was then used in transient simulation where the choice of substrate was shown to noticeably affect the model's turn-on and turn-off energy.

INDEX TERMS Power transistors, Gallium compounds, semiconductor device modeling.

I. INTRODUCTION

Accurate modeling of power semiconductors is an important tool to facilitate achievement of design goals in fabrication. This process is especially attractive for next-generation gallium nitride (GaN) devices which possess specific material characteristics that can be emphasized to make them particularly beneficial for power electronic applications [1]–[3]. However, the relative immaturity of GaN (compared to silicon (Si)) processing makes experimental fabrication studies prohibitively expensive. TCAD simulation software can be used to simulate devices that are not currently available [4], which reduces the need for costly fabrication studies.

This brief utilizes an empirically validated TCAD model in Sentaurus TCAD of a fabricated GaN lateral FET to investigate the effect of substrate materials on the switching performance of the device. The device in question is similar in structure to the devices reported in [5] and [6]. This TCAD model was developed to accurately match IV and CV characterization data of a fabricated device and is described in detail in [7]. The calibrated forward and CV curves of this TCAD model are shown in Fig. 1 and Fig. 2 respectively.

Previous works have investigated the impact on device performance arising from different substrate thickness or cuts [8], as well as termination types [9] for a given substrate material. This work, instead, focuses on the prefabrication decision of selecting a suitable substrate for one's device based on performance considerations which should be balanced against initial substrate production costs.

The remainder of this brief is organized as follows: Section II describes the effect of substrate selection on C_{DS} and C_{GD} of the device as well as their dependence on V_{DS}. Section III discusses the effect of substrate selection on switching characteristics using a transient simulation at different bias conditions. Section IV offers concluding remarks and a discussion of future research directions.

II. EFFECT OF SUBSTRATE SELCTION ON C_{GD} AND C_{DS}

The investigation of substrate selection was confined to three of the most prevalent options available commercially: silicon (Si), sapphire (Al_2O_3), and semi-insulating bulk GaN. Although other substrates are also of interest to the community (e.g., SiC), the three chosen here to represent a realistic

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

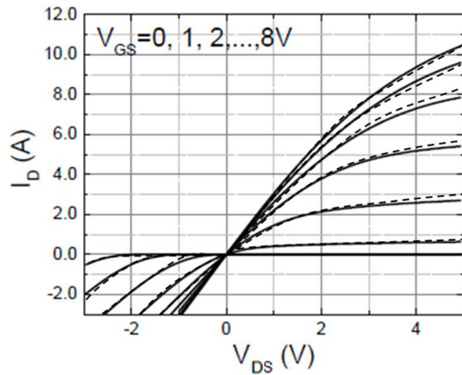

FIGURE 1. Forward curves of recessed gate GaN FET with experimental data (solid) and TCAD simulation (dashed). Simulation performed at $V_{GS} = 0, 1, \ldots, 8$ V.

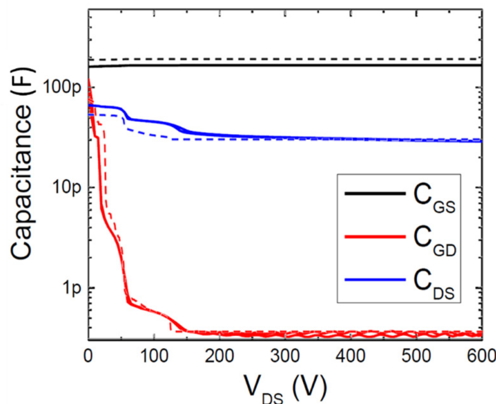

FIGURE 2. *CV* curves with experimental data (solid), and TCAD simulation (dashed) for the recessed gate FET. Note that C_{GD} is subject to a measurement limit of approximately 400 fF.

set that a designer would consider in terms of cost and feasibility.

Each material has a particular set of advantages. Si substrates are relatively inexpensive, and can leverage mature Si semiconductor technology, but suffer from a large thermal and lattice mismatch with GaN which can lead to high defect densities and wafer cracking [10]. GaN epitaxial layers grown on GaN substrates exhibit low defect density (homoepitaxy) and do not suffer from thermal expansion issues but are still only available in relatively small sizes and therefore are expensive per wafer area [11]. Sapphire occupies a middle ground between GaN and Si, in terms of cost, defect densities, and the risk of thermal cracking [12].

To ascertain the effect, if any, of substrate selection on CV characteristics of the device, the recessed gate device described in [7] was simulated with each of the three chosen substrates. A cross-section of this device with capacitances of interest is shown in Fig. 3. The Si substrate in this work is a p-type wafer at 10^{17} cm^{-3} grown using the Czochralski process as described in [6] and as used in the fitting described in [7]. As the Si substrate of the device is 100 μm thick (not shown in Fig. 3 for aesthetic reasons), both the sapphire and GaN substrates were also simulated at this thickness for consistency purposes. In all cases, the substrates of the devices were source connected and grounded. Traps were simulated at the SiN/AlGaN interface and at the gate contact to achieve depletion as descried in [7].

The effect of the substrate on C_{GS} was found to be minimal as C_{GS} has very little dependence on V_{DS}. The effect of substrate selection on C_{GD} and C_{DS} was more pronounced. In Fig. 4, there is a clear difference in the values of C_{DS} for the recessed gate device at high V_{DS} bias. At high bias, there is an approximately 75% and 85% reduction in C_{DS} for the sapphire and GaN substrates respectively as compared to the Si substrate. This implies that at high bias, the choice of substrate can have a substantial effect on the switching performance of the device. Similar trends are observed for C_{GD} as shown in Fig. 5, which shows a 63% reduction for the sapphire substrate and a 90% reduction for the GaN substrate at high V_{DS} bias. Although the magnitudes of the reduction between C_{DS} and C_{GD} are different, the *percentage* decrease in each quantity is similar relative to the Si substrate.

During events with high frequency content (e.g., switching), the conductivity of the substrate material will cause it to act as a "parallel" capacitor to C_{GD} and C_{DS}. This is shown physically in Fig. 3, in which the overall capacitances of these contacts are implicitly a function of the terminal capacitances with coupling through the substrate. Therefore, as the terminals' geometry and spacing effect on these quantities decreases with increasing voltage, the substrate capacitances begin to dominate the total C_{DS} and C_{GD}, becoming pronounced at high V_{DS} bias. This explanation is supported by an analytical model for coupling of substrate capacitance to terminal capacitances of a HEMT device as proposed in [13], in which the substrate is modeled as a "back field plate" type structure which modulates the small-signal response of the device. It is reasonable then to assume that the differences in conductivity and permittivity between substrates provides sufficient causal explanation for the observed trends. This is further reinforced by Fig. 6 which shows electric field as a function of vertical depth at 600 V drain-source bias. The large increase in electric field concentrated at the substrate junction at 100 μm corresponds directly to the substrates effect on the device's overall capacitance.

Directly understanding the effect of this decrease in capacitance can be assessed by the output charge, Q_{OSS}, which can be calculated as

$$Q_{OSS} = \int_0^{V_{bias}} (C_{DS} + C_{GD}) dV_{DS} \quad (1)$$

where V_{bias} is the applied DC bias voltage from drain to source. The quantity, Q_{OSS} then represents the necessary charge that must be supplied in order to turn a device on or off. Since C_{DS} and C_{GD} are V_{DS}-dependent, Q_{OSS} thus quantifies how any change in CV affects switching energy.

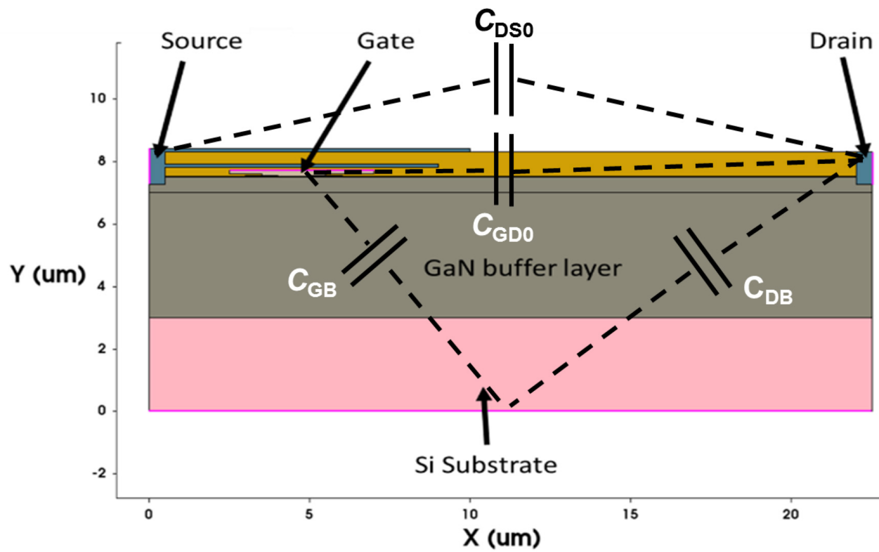

FIGURE 3. Physical layout of capacitances in transistor. The overall C_{DS} is a parallel combination of C_{DS0} and C_{DB} because of the source connected substrate. C_{GD} is a parallel combination of C_{GD0} and the series combination of C_{DB} and C_{GB}.

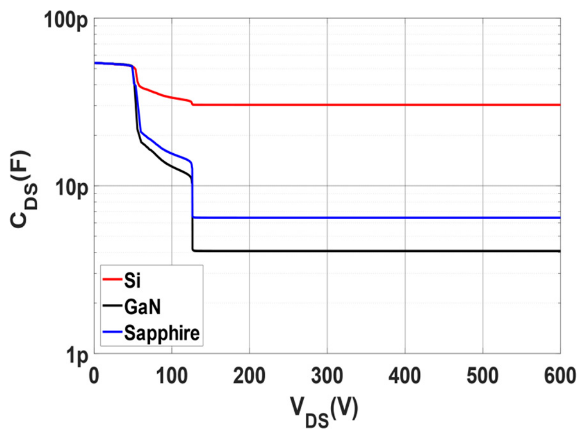

FIGURE 4. TCAD simulation of recessed gate FET for C_{DS} versus V_{DS} with different substrates.

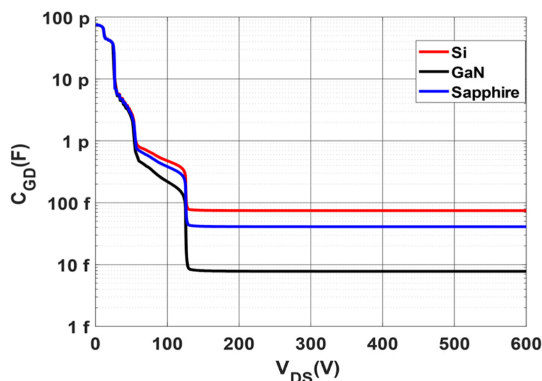

FIGURE 5. TCAD simulation of recessed gate FET for C_{GD} versus V_{DS} with different substrates.

The results shown in Fig. 4 and 5 then will by (1) show a distinct decrease in Q_{OSS} for the device with GaN and Al_2O_3 substrates.

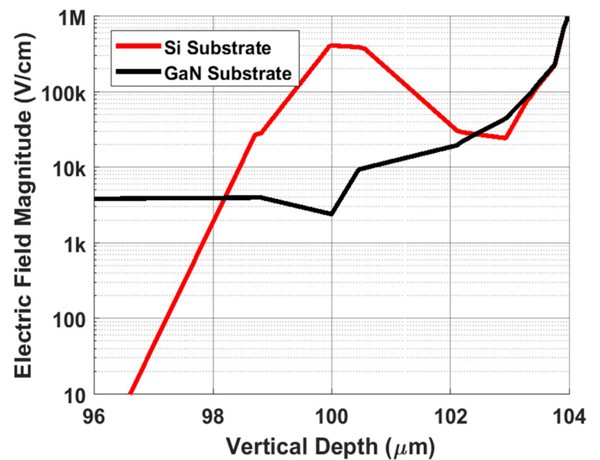

FIGURE 6. Comparison of electric field magnitude as a function of vertical depth. Note junction line of device for substrate is at 100 μm.

With these observed changes in the CV characteristics and output charge based on substrates, the same device can be subjected to transient analysis in order to assess the total impact of such differences on the switching capabilities of the device under test.

III. EFFECT OF SUBSTRATE SELECTION ON TRANSIENT PERFORMANCE

To assess the impact of the shifts in capacitances due to substrate material variation, a transient simulation of the device was performed. Both inductive and resistive load tests were performed. The schematic for the resistive load test is shown in Fig. 7 with the inductive load test merely substituting an inductor for the resistor. Each of these bias circuits were simulated with a gate resistance, R_G, of 1 Ω and 5 Ω. Both bias circuits were used to establish the effect on switching performance due to the substrate selection independent of the

TABLE 1. Simulated switching energies for devices with each substrate.

	Resistive Load				Inductive Load			
	$R_g = 1\,\Omega$		$R_g = 5\,\Omega$		$R_g = 1\,\Omega$		$R_g = 5\,\Omega$	
Substrate Material	E_{ON} (μJ)	E_{OFF} (μJ)	E_{ON} (μJ)	E_{OFF} (μJ)	E_{ON} (μJ)	E_{OFF} (μJ)	E_{ON} (μJ)	E_{OFF} (μJ)
Silicon	0.66	0.35	3.25	1.60	1.94	0.96	7.51	4.06
GaN	0.28	0.14	1.32	0.64	0.81	0.39	3.14	1.68
Sapphire	0.31	0.16	1.52	0.75	0.93	0.47	3.57	2.03

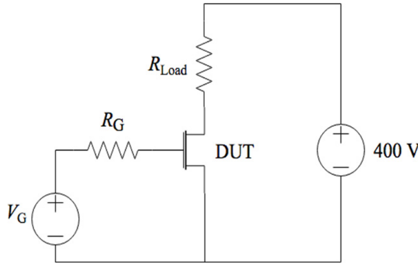

FIGURE 7. Bias circuit for resistive load transient simulations.

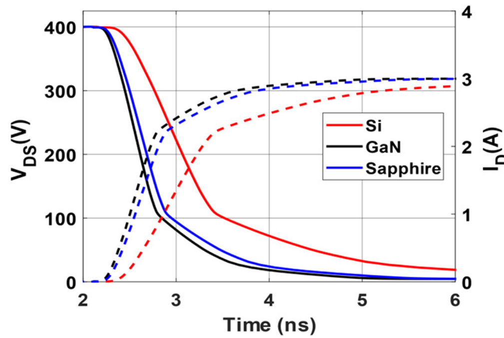

FIGURE 8. Comparison of turn-on edges for the recessed gate GaN FET for a 400-V, 3-A application with a resistive load and an R_G of 1 Ω. Solid lines are voltage waveforms and dashed lines are current waveforms.

loading of the device. Additionally, no parasitic inductances were added to the device in these simulations. While parasitic inductances arising from packaging of a device are known to influence the switching capabilities of GaN devices, they were omitted here so as to isolate only the performance of the device under test.

The turn-on edge for the GaN device is shown in Fig. 8 and the turn-off edge in Fig. 9 for a 400-V, 3-A application with a resistive load and an R_G of 1 Ω. Fig. 8 shows a significant increase in slew rate for each substrate choice corresponding to the reduction in capacitance discussed in Section II. This is primarily attributable to the decrease in total Q_{OSS} charge for each substrate at 400 V drain-source bias.

The turn-on energy, E_{ON} of each test as well as the turn-off energy E_{OFF} was then calculated. The results of these calculations for both the resistive load as well as the inductive load for each substrate choice are summarized in Table I for an R_G of 1 Ω and an R_G of 5 Ω. The entries of Table I reflect the findings of Section II, which is that a reduction in the capacitance based on substrate selection lead to a corresponding decrease in switching energy. Modern

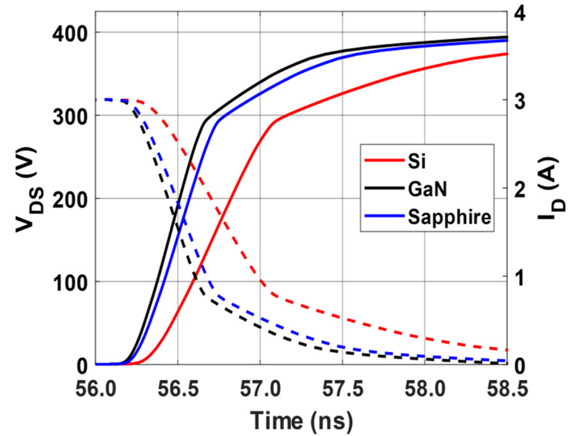

FIGURE 9. Comparison of turn-off edges for the recessed gate GaN FET for a 400-V, 3-A application with a resistive load and an R_G of 1 Ω. Solid lines are voltage waveforms and dashed lines are current waveforms.

power electronic converters based on GaN transistors routinely switch at frequencies of 1 MHz or more. Consequently, the small differences in switching energy in Table I will become substantial differences in losses over the lifetime of such a part.

IV. CONCLUSION

This brief presented an assessment of the effect substrate selection has on switching performance of a lateral GaN FET. A previously developed model [7] was utilized to first investigate the effect of substrate on the voltage-dependent C_{GD} and C_{DS} characteristics of the device. It was found that the choice of substrate led to a significant difference in C_{GD} and C_{DS} for the device at high V_{DS} bias which led to a significant decrease in Q_{OSS}. The switching energy of these devices under various load conditions was then evaluated based on this change in capacitance. This transient study demonstrated that there are potential switching loss benefits based on which substrate is selected, specifically the use of GaN and Sapphire substrates over Si. These considerations of improved performance by the reduction of substrate coupling capacitances should be weighed against the fabrication complexity and cost when selecting a substrate material and process. That is, one should not only look at the increased cost of using GaN or sapphire substrates in a production design of a given lateral GaN power transistor, but also consider the improved performance one should expect electrically if these substrates are used.

REFERENCES

[1] X. C. Huang, Q. Li, Z. Y. Liu, and F. C. Lee, "Analytical loss model of high voltage GaN HEMT in cascode configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2208–2219, May 2014.

[2] W. Zhang, F. Wang, D. J. Costinett, L. M. Tolbert, and B. J. Blalock, "Investigation of gallium nitride devices in high-frequency LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 571–583, Jan. 2017.

[3] M. Rodriguez, Y. Zhang, and D. Maksimovic, "High frequency PWM buck converters using GaN-on-SiC HEMTs," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2462–2473, May 2014.

[4] Z. Li and T. P. Chow, "Design and simulation of 5–20-kV GaN enhancement-mode vertical superjunction HEMT," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3230–3237, Oct. 2013.

[5] R. Chu *et al.*, "Normally-off GaN-on-Si transistors enabling nanosecond power switching at one kilowatt," in *Proc. Device Res. Conf.*, Notre Dame, IN, USA, Jun. 2013, pp. 199–200.

[6] R. Chu *et al.*, "1200-V normally-off GaN-on-Si field-effect transistors with low dynamic on-resistance," *IEEE Electron Device Lett.*, vol. 32, no. 5, pp. 632–634, May 2011.

[7] M. R. Hontz, R. Chu, and R. Khanna, "TCAD modeling of a lateral GaN HEMT using empirical data," in *Proc. IEEE Appl. Power Electron. Conf.*, San Antonio, TX, USA, Mar. 2018, pp. 244–248.

[8] M. Borga *et al.*, "Impact of the substrate and buffer design on the performance of GaN on Si power HEMTs," *Microelectron. Rel.*, vols. 88–90, pp. 584–588, Sep. 2018.

[9] S. Moench *et al.*, "Effect of substrate termination on switching loss and switching time using 600 V GaN-on-Si HEMTs with integrated gate driver in half-bridges," in *Proc. IEEE 5th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Albuquerque, NM, USA, 2017, pp. 257–264.

[10] M. Ishida, T. Ueda, T. Tanaka, and D. Ueda, "GaN on Si technologies for power switching devices," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3053–3059, Oct. 2013.

[11] T. J. Anderson *et al.*, "Effect of reduced extended defect density in MOCVD grown AlGaN/GaN HEMTs on native GaN substrates," *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 28–30, Jan. 2016.

[12] T. Paskova, D. A. Hanser, and K. R. Evans, "GaN substrates for III-Nitride devices," *Proc. IEEE*, vol. 98, no. 7, pp. 1324–1338, Jul. 2010.

[13] S. A. Ahsan, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "Analysis and modeling of cross-coupling and substrate capacitances in GaN HEMTs for power-electronic applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 816–823, Mar. 2017.