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Analysis on Temperature Dependence of Hot Carrier Degradation by Mechanism Separation

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ABSTRACT Temperature dependence under various HCD conditions was analyzed in 14 nm node FinFETs. Unlike oxide traps, interface traps show different temperature dependence depending on HCD voltage conditions. Therefore, the interface traps were separated into three components and the temperature dependence was analyzed for each component. Multiple particle process (MP) and Field enhanced thermal degradation process (FP) have a constant temperature dependence regardless of voltage conditions. On the other hand, the temperature dependence of Single particle process (SP) varies depending on the voltage condition because SP is affected by scattering. However, the components of the interface traps in at nominal operating voltage changes since self-heating effect is different comparing the accelerated voltage. Therefore, we predicted the ratio of each component under nominal operating condition.

INDEX TERMS Hot carrier degradation, interface trap, temperature dependence, self-heating.

I. INTRODUCTION

Hot carrier degradation (HCD) is a phenomenon that degrades performances due to the generation of defects at the Si/gate dielectric interface or inside the gate dielectric material [1]. Therefore, HCD is one of the representative issues of reliability and has been studied for decades. In general, HCD predict lifetime through acceleration in the worst case. In long channel device, HCD was most deteriorated under the condition of $V_{GS} = V_{DS}/2$ where impact ionization (I.I.) is the peak and low temperature [2]. However, as high-k layers have been applied as devices have been scaled down, pre-existing traps rapidly have been increased to show high degradation when $V_{GS} = V_{DS}$ and in high temperature [3]. Therefore, voltage and temperature are important factors in determining hot carrier degradation.

In the past, measurement of HCD was based on long-channel devices and HCD was explained as follows based on measurements; carriers with energy of over 3.7 eV break the Si-H bonds and generate interface traps [4], [5]. Therefore, the maximum electric field was considered the most significant cause of HCD. However, because HCD kept occurring in low operation voltage HCD could not be explained in short channel devices [6]. Therefore, further studies have described HCD at low operating voltages through a new theory, the energy exchange mechanism [7], [8]. Various studies have been conducted on HCD of short/long channel nMOSFETs by ViennaSHE with energy driven model by T. Grasser. As the device scaled down, however, the carrier energy-based approach became complicated and difficult. Therefore, recent HCD studies of FinFET devices predict lifetime through simple compact modeling based on measurements [9], [10]. In addition, as the channel thickness decreases, the self-heating effect becomes more severe and the influence of temperature on HCD increases [11]. However, few studies analyze HCD through fundamental physical mechanisms, and many researches are focused on empirical modeling based on measurement. In addition, since the application of the GAA structure is expected in sub-5 nm nodes, it is crucial to understand the temperature dependence of HCD based on physical theories in FinFETs, which is a basic 3D structure. However, it is very difficult to analyze the temperature dependence of HCD because there are many mechanisms for HCD,

Therefore, in this paper, we analyzed the temperature dependence by separating the mechanisms of HCD and the

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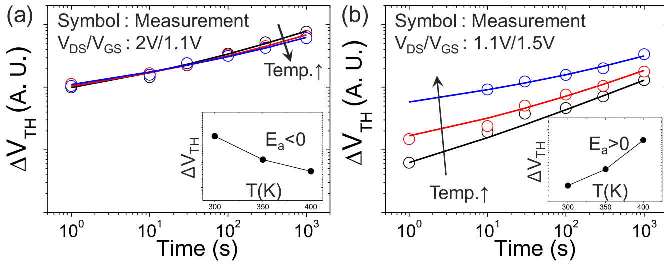

FIGURE 1. Temperature dependence of HCD according to two voltage conditions (a) V_{DS}/V_{GS} = 2V/1.1V (b) V_{DS}/V_{GS} = 1.1V/1.5V.

overall temperature dependence through the ratio of each mechanism.

II. EXPERIMENT

14 nm node bulk FinFETs have been utilized in this study with high-*k*/metal-gate processes. The measurements have been performed in various voltage and temperature conditions. Variability is an important issue in 14 nm node devices. We have conducted 4 measurements in each HCD condition to investigate the general temperature dependency and selected the measurement result among the 4 measurements which was closest to the mean value. Also, measurements were conducted within one wafer to maximally suppress the variability between the devices and devices that showed similar V_{TH}/on-current through I-V characteristic were used to measure the HCD. Because the variation between devices decreases as the number of Fins increases in FinFETs, 4-Fin devices with relatively low variation were used in this study [12].

Figure 1 shows the temperature dependence of HCD according to two voltage conditions. Measurements have been performed in temperature conditions of 300, 350, and 400 K. Degradation decreases as the temperature increases in the high drain voltage condition (2V/1.1V) and degradation increases as the temperature increases in the high gate voltage condition (1.1V/1.5V). Since there are various mechanisms for generating HCD, it is necessary to understand the temperature dependence of each mechanism in order to clearly analyze these results. Generally, oxide traps (trapping) increase as temperature increases [13]. Therefore, if there is only a tendency for the interface trap to decrease with temperature, the opposite temperature dependence can be explained simply by the combination of oxide trap and interface trap that varies with voltage conditions. Therefore, V_{TH} shift caused by oxide trap (ΔV_{OT}) and interface trap (ΔV_{IT}) was separated using Subthreshold swing (S.S.).

Generally, interface traps are formed with specific distributions within the bandgap [14]. Therefore, as V_{GS} increases, S.S. changes due to the increase of interface traps involved in V_{TH} shift. Also, the interface traps act as scattering centers, causing additional on-current degradation (Fig. 2(a)). However, because oxide traps are generated at a constant level within the band gap, only the V_{TH} shift occurs. Therefore, the ΔV_{IT} and ΔV_{OT} components were separated

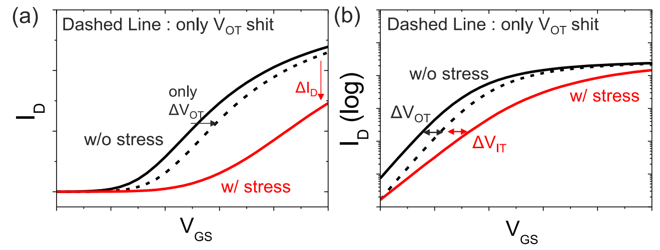

FIGURE 2. (a) Additional on-current degradation (ΔI_D) due to interface traps (b) ΔV_{TH} and ΔV_{OT} component separation using total V_{TH} shift and SS.

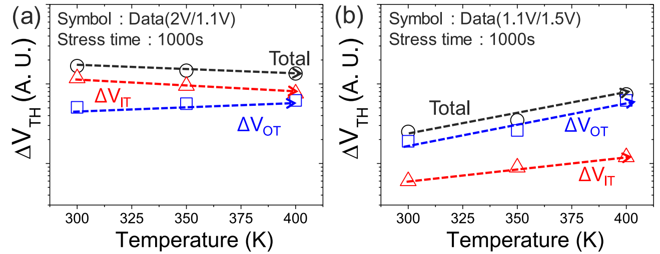

FIGURE 3. Temperature dependence of ΔV_{OT} and ΔV_{IT} according to two voltage conditions (a) V_{DS}/V_{GS} = 2 V/1.1 V (b) V_{DS}/V_{GS} = 1.1 V/1.5 V.

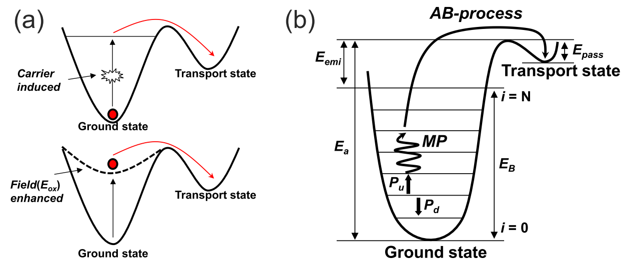

FIGURE 4. (a) Mechanisms of interface trap generation due to carrier collision and thermal degradation (b) Schematic of truncated harmonics expansion model.

based on the off current of the stressed I-V curve as shown in Figure 2(b).

Figure 3 shows the ΔV_{OT} and ΔV_{IT} components with temperature at each acceleration condition. As mentioned above, ΔV_{OT} increased as the temperature increased in both voltage conditions. On the other hand, ΔV_{IT} has different temperature dependences under two voltage conditions. Because these results mean that the temperature dependence of each mechanism for generating interface traps is different, additional analysis is needed to understand the overall temperature dependence. Therefore, in this paper, the interface trap was separated into three mechanisms and the temperature dependence of each mechanism was analyzed.

III. SIMULATION

A. PHYSICAL THEORY

Figure 4 (a) shows the mechanism of interface trap generation. Generation of interface traps is divided into components due to carrier collision and components due to the field enhanced thermal degradation [15]. First, the mechanisms

TABLE 1. The equations for each mechanism of interface trap generation.

Field-enhanced thermal degradation			
Density	$N_{IT,FP} = N_0\left[1-\exp\left(-\kappa_{FP}t\right)\right]$	***Reaction rate***	$\kappa_{FP} = v_{FP}e^{-E_{FP}/kT},\ \ E_{FP} = E_{FP0} - pE_{OX}$
Single Particle / Multiple Particle			
Density	$N_{IT,SP} = N_0\left[1-\exp\left(-\kappa_{SP}t\right)\right],\ \ N_{IT,MP} = P_{MP}N_0\left[\frac{P_{emi}}{P_{pass}}\left(\frac{P_u}{P_d}\right)^N\left(1-\exp\left(-P_{emi}t\right)\right)\right]^{1/2}$		
Reaction rate	$\kappa_{SP} = \int_{E_{SP}}^{\infty} f(E)g(E)v(E)\sigma_{SP}(E)dE,\ \ \kappa_{MP} = \int_{E_{MP}}^{\infty} f(E)g(E)v(E)\sigma_{MP}(E)dE$		
Probability	$P_u = \kappa_{ph}e^{-E_{ph}/kT} + \kappa_{MP}(E_{MP}),\ \ P_d = \kappa_{ph} + \kappa_{MP}(E_{MP})$		

due to carrier collision are classified into two components. Single-particle process (SP) forms Si-H bond dissociation due to the interaction of carriers with high energy. Low energy carriers release hydrogen into the transport state at the last bonded level through multiple collisions. This process is referred to as the multiple-particle process (MP). The two mechanisms are described as the truncated harmonics expansion model (Fig. 4(b)) [16]. It is significant to consider various scattering mechanisms where energy is exchanged because degradation is determined by the carrier energy. Second, the field enhanced thermal degradation process (FP) is a mechanism that generates Si-H bond dissociation by ambient thermal energy only. In particular, the oxide field reduces the activation energy required for transition to the transport state. Therefore, FP increases as temperature and oxide field increase.

In this study, Synopsys Sentaurus TCAD simulation was used [17]. TCAD simulation can solve the Boltzmann transport equation (BTE) through the Spherical harmonics expansion method to calculate the energy of each carrier. In addition, since the truncated harmonics expansion model is applied, interface trap generation due to carrier collision based on carrier energy can be accurately implemented. Also, FP was applied to the simulation with the stretched exponential model which the equation considers the oxide field and temperature. The equation of this model can be expressed as a carrier acceleration integral (AI) and the AI defines the Si–H bond dissociation rate using the carrier energy distribution function (EDF). The density of N_{IT} is determined by the reaction rate and the bond rate is applied to the reaction rate to account for the discrete activation energy.

Table 1 shows the equations of each mechanism [18]. As mentioned above, because the SP and MP mechanisms are determined by the carrier energy, EDF is very important in HCD modeling. This EDF can be obtained by solving the BTE.

$$-\nabla\cdot\left[\frac{v(E)}{3}\tau(E)g(E)\nabla f(E)\right] = g(E)s(E) \tag{1}$$

In the process of calculating the BTE, the EDF is expressed as $f(E)$. In addition, $v(E)$, $g(E)$, $\tau(E)$, and $s(E)$ represent the velocity, density of state, total scattering rate, and in-elastic scattering rate, respectively.

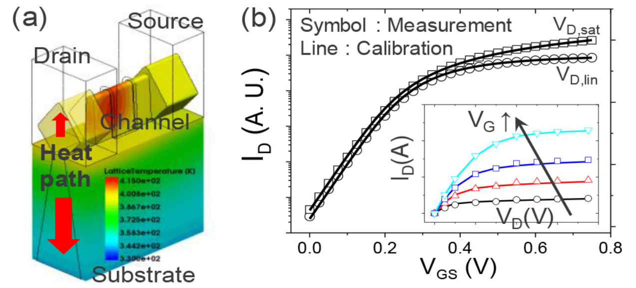

FIGURE 5. (a) FinFET device designed through the TCAD simulation tool and heat generation caused by on current (b) Calibrated I-V curve.

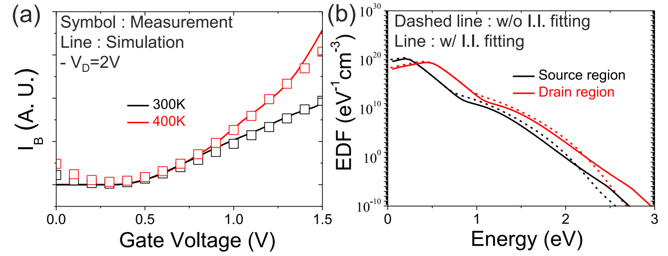

FIGURE 6. (a) Calibration result of body current ($I_B - V_G$) according to temperature (b) EDF modified by applying the parameters of I.I.

B. TCAD SIMULATION SETUP

To calibrate the HCD data, I-V calibration was conducted first. In the calibration process, accurate implementation of self-heating effect (SHE) is very important because self-heating has significant effect on the temperature dependence on HCD. SHE was considered by using the Thermodynamic model. Additionally, various thermal conductivities have been applied according to each material and thickness, and different doping concentrations and dopant materials have been considered in Si [19]. Figure 5(a) shows the FinFET structure designed by TCAD simulation and the heat generation obtained during the I-V calibration process. It can be seen that the maximum temperature occurs in the drain region where the field is high and heat is released to the drain/source and substrate. Figure 2(b) shows the results of the I-V calibration. eQuantumPotential and BALMob models were used to consider quantum effects and ballistic transport, respectively. In the case of the BALMod model, the ballistic component was added to the original mobility term. Also, various mobility models including phonon, Coulomb, carrier, and surface scattering were considered using the Phumob, CarrierCarrier, and Enormal(Lombardi) models and velocity saturation was considered using the HighFieldSaturation model. Tensile stress was applied to the channel to consider strain effect due to the source/drain.

In hot carrier conditions, a high electric field causes a large amount of impact ionization. Therefore, in order to improve the accuracy of the hot carrier simulation, the body current ($I_B - V_G$) was calibrated. The VanOverstraeten model, an impact ionization model, was used and the data and simulation results were found to fit well (Figure 6 (a)). Carrier

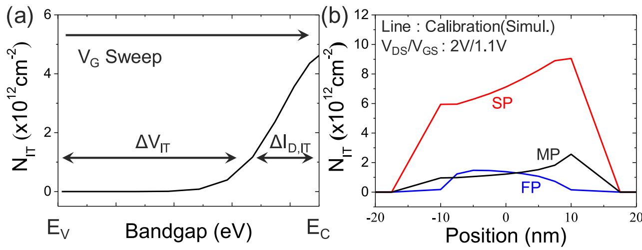

FIGURE 7. **(a) N_{IT} distribution within the bandgap (b) N_{IT} distribution in the channel.**

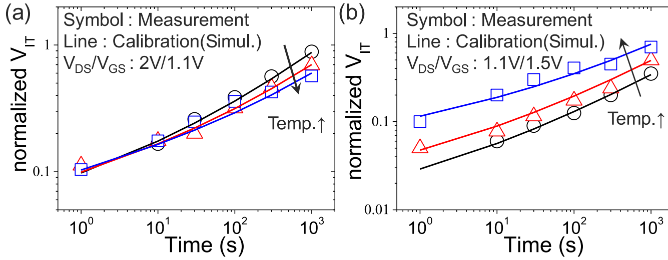

FIGURE 8. **(a) Calibration results between the ΔV_{IT} data and the simulation versus stress time at V_{DS}/V_{GS} : 2V/1.1V condition (b) V_{DS}/V_{GS} : 1.1V/1.5V.**

energy changes because the amount of I.I. changes during the calibration process. Figure 6 (b) shows the change of EDF by applying the parameters of I.I. extracted during the calibration process. The SP component is most affected because the distribution of high energy carriers is different.

C. CALIBRATION

Figure 7(a) shows the N_{IT} distribution within the bandgap which is determined through the calibration process. In the case of nMOSFETs, the Fermi level in the bandgap is swept from E_v to E_c when the gate voltage increases. Therefore, the N_{IT} distribution between E_v and middle level in the bandgap contributes to V_{IT}. The additional N_{IT} distribution near E_c contributes to on-current degradation. Figure 7(b) shows the N_{IT} distribution in the channel. As mentioned above, since SP and MP are carrier energy dependent components, SP and MP occur in the drain region where the lateral field is strong. On the other hand, the FP component shows a peak in the source region where the vertical field is high because the vertical field is an important factor.

Figure 8 shows the calibration results between the ΔV_{IT} data and the simulation versus stress time. Iteration was performed until a parameter set was obtained that satisfies all conditions, and the ΔV_{IT} was calibrated well according to temperature. Current degradation rate ($\Delta I_D/I_D$) is an important parameter in HCD. However, the current degradation rate and the interface trap density are not directly proportional because the reference current is different for each temperature. On the other hand, the ΔV_{TH} is directly proportional to the interface trap density because it is an absolute value rather than a ratio. Therefore, in this paper, we analyzed HCD temperature trend through ΔV_{TH}.

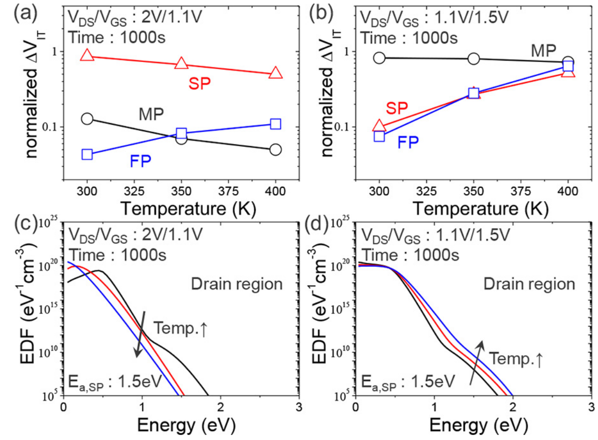

FIGURE 9. **(a), (b) Temperature dependence on each mechanism and (c), (d) Energy distribution function (EDF) in two voltage conditions.**

In the calibration process, carrier energy was calculated by considering Phonon, Coulomb, CarrierCarrier and I.I. scattering. In addition, the vibrational mode of Si-H bond was the bending mode and the bond dispersion and dipole moment due to activation energy (E_a) fluctuation were considered.

IV. RESULTS AND DISCUSSION

Figure 9 shows the temperature dependence on each mechanism that causes interface traps. The MP is related to the number of carriers and vibration frequency of the Si-H bond. When vibration occurs, Si-H bonds tend to lose energy rather than gain energy. Although there is no significant change of the number of carriers as the temperature increases, the vibration frequency of Si-H bond increases [20]. Therefore, the MP decreases as the temperature increases. FP is a phenomenon where Si-H bonds, which are weakened by the oxide field, break due to thermal energy. The FP accordingly increases as the temperature increases.

The SP is significantly affected by factors that change the carrier energy such as scattering, voltage, and temperature conditions because the E_a is high. When the drain voltage is high, many carriers with high energy are distributed throughout the channel. Therefore, the effect of increased carrier energy according to increasing temperature is not dominant in this case. Meanwhile, phonon scattering increases as the temperature increases which decreases the carrier energy, and decreases the SP (Fig. 9(c)). On the other hand, when the drain voltage is low, most carriers have low energy. Since phonon scattering occurs under carriers with high energy majorly, carriers with low energy have low influence on phonon scattering. Therefore, SP increases since the energy of carriers increases as temperature rises (Fig. 9(d)). As a result, the tendency of the SP can be considered as a significant factor that determines the temperature dependence on the total interface traps.

Figure 10(a) shows the comparison of the effect of each mechanism in two voltage conditions. It is especially worth

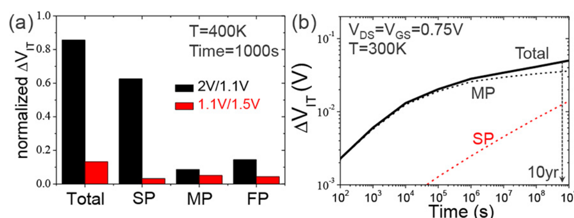

FIGURE 10. (a) Comparison of the effect of each mechanism in two voltage conditions (b) ΔV_{IT} components in the operating region.

noting the results of the FP component. Degradation due to the FP is generally high when in strong oxide field conditions. However, FinFETs have a high self-heating effect, which can lead to high degradation even at lower oxide fields. Therefore, in nominal operating condition, the composition of mechanisms can be changed because of the lower voltage and weaker self-heating effect compared to the accelerated stress conditions.

Figure 10(b) shows the predicted degradation under nominal operating condition through simulation. The time required for deterioration is different for each component, and MP occurs first because of lowest E_a. On the other hand, FP occurs under accelerated stress conditions, but not in the nominal operating condition. Therefore, it is possible to underestimate the actual lifetime when accelerating under the conditions of Figure 10(a). However, because the components of V_{IT} differ depending on the structure and operating voltage of the device, it is important that the acceleration conditions reflect the components in the nominal operating condition in order to accurately predict the lifetime. Therefore, researches that accurately analyze HCD using each mechanism are very important.

V. CONCLUSION

Temperature dependence of HCD was analyzed under two voltage conditions. In the case of oxide traps, deterioration increases as temperature increases under all conditions. However, in the case of interface traps, opposite temperature dependence was shown under two voltage conditions. In order to analyze this dependence, interface traps were separated into three components and the temperature dependence of each component was analyzed. MP and FP have a constant temperature trend depending on voltage conditions. However, SP is highly influenced by scattering and shows various temperature dependences. Due to the self-heating, FinFET has different temperatures at accelerated conditions and nominal operating condition. In the nominal operating region, FP disappears due to weak self-heating. However, the components vary depending on the structure of the device and the operating voltage. Therefore, it is necessary to consider these components when determining the acceleration condition.

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