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Low-Leakage Capacitive Coupling Structure for a-Si:H Gate Driver With Less Delay of Clock Signals Used in AMLCDs

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ABSTRACT This work proposes a hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) gate driver with a low-leakage capacitive coupling structure to reduce the delay of the clock signal. The proposed circuit suppresses the fluctuation in the gate node of the driving TFT induced by clock-feed-through effect, reducing the leakage current that flows from the clock signal line to the power source line with a low voltage level. This reduction in the leakage current can improve the degradation in the voltage of the clock signal and thus avoid the increase in the rising time of the scan pulse. Measurements for extracting the drain current versus gate-to-source voltage (I_D-V_{GS}) curves of a fabricated a-Si:H TFT are made to establish a simulation TFT model by fitting the obtained curves. For the same parameters of the TFTs and capacitances, the leakage current and the rising time of the output waveform of the proposed circuit are 45.45% and 21.36% lower, respectively, than those of previously developed gate driver.

INDEX TERMS a-Si:H TFTs, capacitive-coupling effect, clock-feed-through effect, gate driver, leakage current.

I. INTRODUCTION

Displays with a high resolution and a narrow bezel, which provide a superior image quality, have become mainstream in recent years. Three common backplanes of the display are hydrogenated amorphous silicon (a-Si:H), amorphous indium-gallium-zinc-oxide (a-IGZO), and low-temperature poly-silicon (LTPS) thin-film transistors (TFTs) [1]–[7]. With the features of the mature manufacturing process, low cost of manufacture, and a high uniformity over glass substrates, a-Si:H TFTs have been extensively used in display applications. Hence, to reduce the cost of displays with high resolution, the pixels and peripheral driver circuits that are based on a-Si:H technology must be developed. As the resolution of displays increases, the duration of a scan pulse, which is generated by integrated gate drivers, decreases [8]–[11]. Additionally, large numbers of gate-to-drain and gate-to-source capacitances (C_{gd} and C_{gs}) from switching TFTs of pixels increase the output loadings of the gate driver. As the operating frequency and the output loadings of the gate driver increase, the insufficient driving capability of the circuit may generate a scan pulse with serious delay. Therefore, a-Si:H TFT gate drivers with a high driving capability are required to generate short rising and falling times of the scan pulse for high-resolution displays. In the design of gate driver circuits, the channel width of TFTs is typically increased to enhance driving capability, accelerating the charging and discharging of the circuit. Since a large driving TFT is customarily used to charge and discharge the output node of the circuit, it accompanies large C_{gd} and C_{gs}. However, the large capacitance C_{gd} of the driving TFT will increase the loading of the clock signal line, causing delay in the clock signal. This problem will become

worse as the resolution of a display increases. Therefore, to prevent the widening of the channel of the driving TFT, several methods, including multi-level clock modulation, the use of a low-leakage pull-down structure, and capacitive coupling, have been developed to increase the driving capability of the gate driver and thereby improve the delay of the scan pulse. The voltage modulation [12], [13] accelerates the charging and discharging to the output node of the gate driver by using clock signals with multiple voltage levels. This method generates a driver IC of great complexity, increasing the cost of the display. Without modifying the existing driver IC, development of pull-down structures with low leakage current [14], [15] can completely turn off pull-down TFTs, avoiding an increase in the rising time of the scan pulse. The reduction in the leakage current of the pull-down structure, however, is inadequate for use in high-resolution or high-frame-rate displays when the operating frequency of the gate driver increases. In contrast, the capacitive coupling method [16], [17], which raises the driving current of the driving TFT by increasing its gate-to-source voltage (V_{GS}), can greatly improve the driving capability of the gate driver. Since this method uses the capacitive coupling effect to bootstrap the voltage at the gate node of the driving TFT, the parasitic capacitances must be considered in the circuit design. The bootstrapped voltage is divided by parasitic or other stored capacitances, limiting improvement in the driving capability of the driving TFT. Furthermore, the fluctuation at the gate node of the driving TFT that is induced by the clock-feed-through effect must also be suppressed to avoid the formation of a direct current path from the clock signal to the lowest power source of the circuit. This current delays the clock signals, preventing the shorting of rising time of the scan pulse.

This work presents a new gate driver circuit that applies the capacitive coupling method to shorten the rising and falling times of the scan pulse. The capacitive coupling effect is used to increase the gate voltage of the driving TFT to improve the driving capability of the circuit. Moreover, the clock-feed-through effect of parasitic capacitors is suppressed to prevent the non-output stages of the gate driver from producing leakage currents that cause the delays in the clock signals. Experimental results indicate that the proposed circuit can effectively yield a shorter rising time of the scan pulse compared with the previously developed work [17].

II. GATE DRIVER WITH CAPACITIVE COUPLING METHOD

A. LEAKAGE CURRENT OF PREVIOUSLY DEVELOPED GATE DRIVER

Fig. 1 displays a schematic, a system diagram, a timing diagram, and the leakage current path of the previously developed gate driver. Clock signals (CK1-CK4) are used to drive the circuit. Although the circuit can shorten the rising and falling times of the output waveform, it has a leakage current that flows from the clock signal to V_L through the driving TFT (T2) and the pull-down TFT (T6) during the stabilizing period, as shown in Fig. 1(d). Since C1 and C2 are

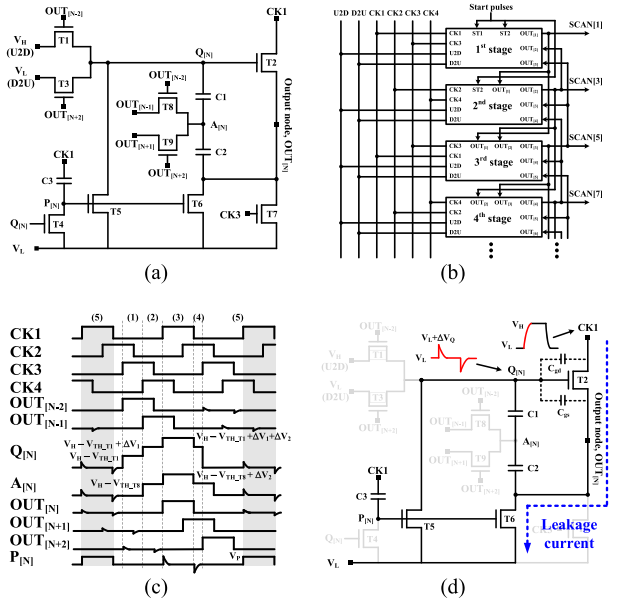

FIGURE 1. (a) Schematic, (b) system diagram, (c) timing diagram, and (d) leakage current path of previously developed gate driver [17].

in series after the circuit has generated a scan pulse, the equivalent capacitance on the gate node of the driving TFT becomes smaller. The change in the clock signal greatly affects the floating node Q owing to the capacitive coupling of C_{gd_T2}, as follows.

$$\Delta V_Q \cong \Delta V_{CK} \times \frac{C_{gd\_T2}}{C_{gd\_T2} + C_{gs\_T2} + \frac{C1 \times C2}{C1 + C2}} \quad (1)$$

Consequently, the driving TFTs in the non-output stages are turned on slightly. The leakage current produces a delay in the clock signals when the voltage level of clock signals changes from V_L to V_H. This phenomenon becomes a problem when the resolution of the display increases. The delay of the clock signals limits the improvement in the rising time of the scan pulse in the previously developed gate driver despite the increase in the driving capability of T2.

B. PROPOSED GATE DRIVER

To increase the driving capability and improve the leakage current of the driving TFT, a new gate driver, which exploits the capacitive coupling method, is proposed. Fig. 2 shows a schematic and a timing diagram of the proposed gate driver, whose operation is described as follows. In the first period, node $Q_{[N]}$ is charged to V_H-V_{TH_T1} through T1, so T2 is turned on to keep node $OUT_{[N]}$ at V_L. Meanwhile, node $A_{[N]}$ is reset to V_L through T8. In the second period, since node $Q_{[N-2]}$ is at V_H-V_{TH_T1} + ΔV_3 + ΔV_4, node $A_{[N]}$ is fully charged to V_H. Hence, node $Q_{[N]}$ is bootstrapped to V_H-V_{TH_T1} + ΔV_3 through the capacitive coupling of C2. In the third period, since T2 is operated in the linear region, V_H is completely transmitted to node $OUT_{[N]}$ when CK3 goes to V_H. Herein, the voltage of node $Q_{[N]}$ is bootstrapped to V_H-V_{TH_T1} + ΔV_3 + ΔV_4 by C2, considerably

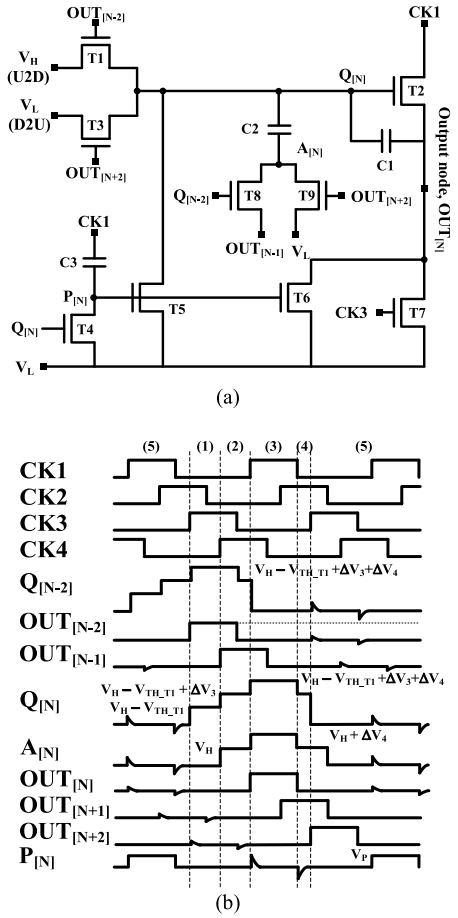

FIGURE 2. (a) Schematic and (b) timing diagram of proposed gate driver.

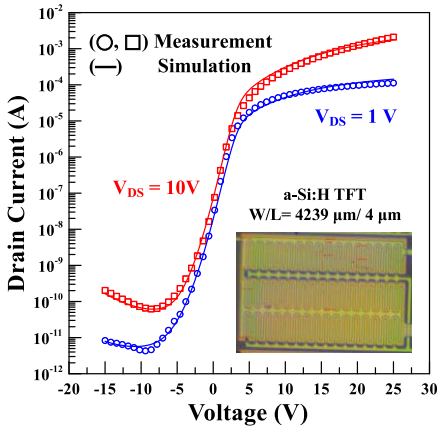

FIGURE 3. Transfer curves of an a-Si:H TFT using for simulation model.

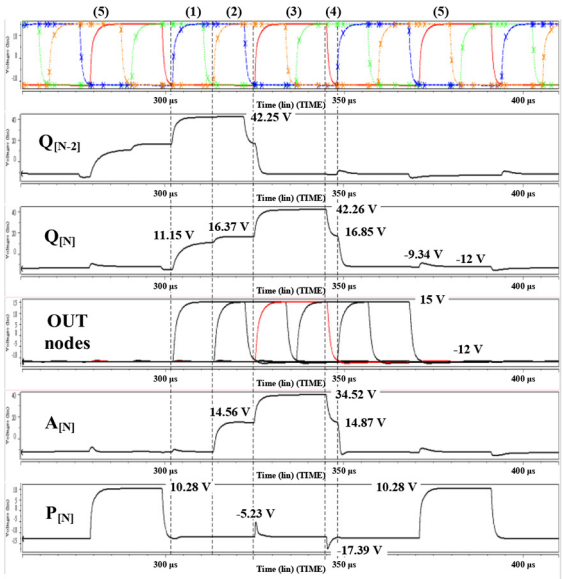

FIGURE 4. Simulated voltage waveforms of proposed gate driver in each period.

increasing the V_{GS} of T2. Therefore, T2 with higher driving capability exhibits faster charging of node $OUT_{[N]}$, yielding a shorter rising time of the output waveform. In the fourth period, when CK3 changes from V_H to V_L, node $Q_{[N]}$ is returned to V_H-V_{TH_T1} + ΔV_3, which still provides a high V_{GS} of T2. Node $OUT_{[N]}$ is thus discharged quickly to V_L through T2. In the fifth period, $OUT_{[N+2]}$ is at V_H, so T3 and T9 are turned on to discharge nodes $Q_{[N]}$ and $A_{[N]}$ to V_L. In the stabilizing period, when CK3 goes to V_H, node $P_{[N]}$ is coupled periodically to V_P by C3. V_P turns on T5 and T6 to stabilize nodes $Q_{[N]}$ and $OUT_{[N]}$, respectively, at V_L. T7 is also activated by CK1 to maintain node $OUT_{[N]}$ at V_L. Herein, the ideal coupled voltage at the floating node $Q_{[N]}$, which is affected by C_{gd}, is given by the following equation.

$$\Delta V_Q \cong \Delta V_{CK} \times \frac{C_{gd\_T2}}{C_{gd\_T2} + C_{gs\_T2} + C_1} \tag{2}$$

Since the equivalent capacitance at node Q exceeds that in the previously developed work, the fluctuation of V_Q can be suppressed and the leakage currents from T2 to T6 in non-output stages reduced. Therefore, based on the aforementioned operation of the proposed gate driver, the proposed circuit can yield short rising and falling times of the output waveform and avoid the delay of clock signals.

III. RESULTS AND DISCUSSION

The feasibility of the proposed gate driver is verified using an HSPICE simulator. To construct a simulation model (RPI, level 61), the electrical characteristics of an a-Si:H TFT with a 4239μm channel width and a 4μm channel length are extracted using a source meter. Fig. 3 plots the measured and simulated transfer curves of the TFT. The V_{TH} and field-effect mobility of the TFT are 3 V and 0.2 $cm^2/V{\cdot}s$, respectively. The RC loading of the scan line of the gate driver is 2.1 kΩ and 80 pF to meet the requirement of a small panel with a resolution of HD + (720 × 1440) and a frame rate of 120 Hz. The loading of the clock bus lines is 1.54 kΩ and 133.5 pF. Also, eight clocks are placed equally on both sides of the panel to support the pre-charging method [17]. The pulse width and duty ratio of the clock signals are thus set to 20 μs (5.75 μs ×4−3μs)

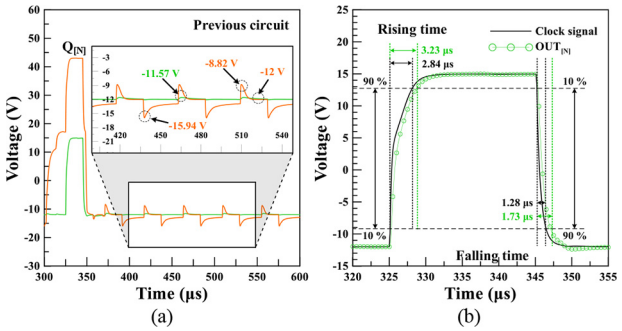

FIGURE 5. Simulated voltage waveforms of (a) node $Q_{[N]}$ and (b) node $OUT_{[N]}$ and clock signal of previously developed gate driver.

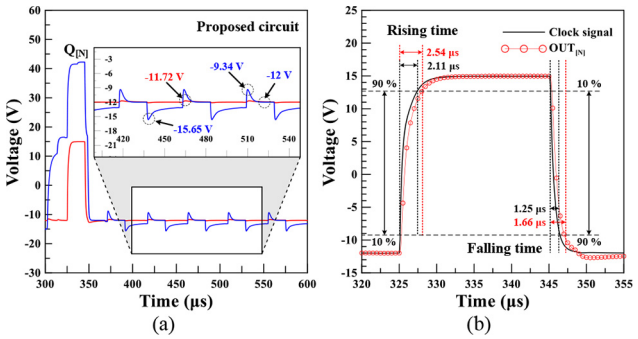

FIGURE 6. Simulated voltage waveforms of (a) node $Q_{[N]}$ and (b) node $OUT_{[N]}$ and clock signal of proposed gate driver.

and 43.5% (20 μs/ 46 μs ×100%), respectively. Herein, the pre-charging time is 14.25 μs, and the data input time is 5.75 μs. Under such specifications, Table 1 lists the sizes and parasitic capacitances of each TFT and the stored capacitors in the previously developed and proposed gate drivers. Fig. 4 plots the simulated voltage waveforms at each node in the proposed gate driver. Since node $Q_{[N-2]}$ is at 42.25 V, node $A_{[N]}$ is charged from −12 V to 15 V through T8. The floating node $Q_{[N]}$ is thus raised to 16.37 V, increasing the driving capability of T2. When CK changes from −12 V to 15 V, the voltage of node $Q_{[N]}$ is bootstrapped to 42.26 V, and 15 V provided by CK1 is fully delivered to node $OUT_{[N]}$ through T2. Thereafter, the voltage at node $Q_{[N]}$ remains at 16.87 V, enabling T2 to discharge node $OUT_{[N]}$ to −12 V. Herein, the voltage node $Q_{[N]}$ is bootstrapped twice to increase the driving current in T2, accelerating the charging and discharging of the $OUT_{[N]}$ node and the scan line. During the stabilizing period, node $P_{[N]}$ is coupled to 10.28 V by C3 to activate T5 and T6 to stabilize nodes $Q_{[N]}$ and $OUT_{[N]}$ at −12 V. Notably, the voltage at node $Q_{[N]}$ coupled by C_{gd_T2} is also discharged from −9.34 V to −12 V.

Figs. 5 and 6 plot the voltage waveforms at nodes $Q_{[N]}$ and $OUT_{[N]}$, and the clock signals of the previously developed and proposed gate drivers. In the previous circuit, node $Q_{[N]}$ is coupled to −8.82 V by C_{gd_T2} when CK1 goes to 15 V periodically, as shown in Fig. 5(a). The voltage of node

TABLE 1. Parameters of previously developed work and this work.

Previous work [17] & this work			
Parameter	Value	Parameter	Value
T1, T3 (μm/μm)	560/4	C1 (pF)	2
T2 (μm/μm)	4239/4	C2 (pF)	2
T4, T5 (μm/μm)	100/4	C3 (pF)	1.2
T6, T7 (μm/μm)	280/4	C_{gd_T2} (pF)	0.813
T8, T9 (μm/μm)	280/4	C_{gs_T2} (pF)	1.626
Clock signal & output loading			
Parameter	Value	Parameter	Value
CK1-CK4 (V)	-12 ~ 15	V_H (V)	15
Scan loading	2.1 kΩ, 80 pF	V_L (V)	-12

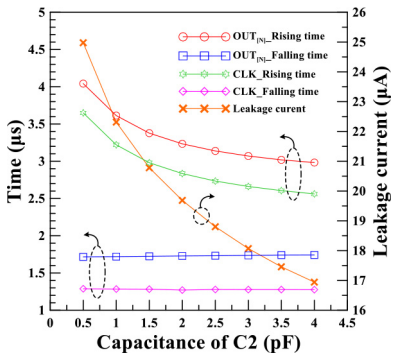

FIGURE 7. Leakage current and rising and falling times of output waveforms and clock signals of previously developed work varying with capacitance of C2.

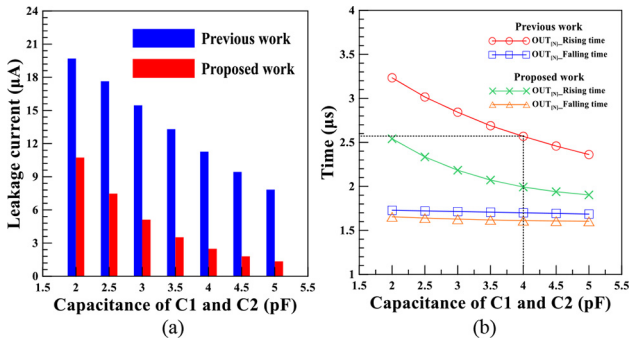

FIGURE 8. (a) Leakage current and (b) rising and falling times of output waveforms of previously developed and proposed works varying with capacitance of C1 and C2.

$Q_{[N]}$ immediately turns on T2, and a generated current of 19.69 μA flows from CK1 line (15 V) to $V_L$line (−12 V) through T2 and T6. The $OUT_{[N]}$ node is thus charged to −11.57 V. In this case, when the clock signals change from −12 V to 15 V, 179 leakage paths (1440 rows/8 clocks – 1 rows) are presented in each clock signal line. These leakage paths produce a serious delay in the clock signal, reducing the improvement in the rising time of the output waveform that is achieved by the previously developed gate driver. Fig. 5(b) shows that the rising times of CK1 and the output waveform are 2.84 μs and 3.23 μs, respectively. The delay of the clock signal will become worse as the resolution of the display increases. In the proposed gate driver, since the capacitance at the gate node of T2 is designed to

be larger, node $Q_{[N]}$ in Fig. 6(a) is lifted only to −9.34 V, greatly reducing the leakage current to 10.74 μA, which is reduced by 45.45% ((19.69 uA-10.74 uA)/19.69 uA × 100%). Notably, the voltage of node $OUT_{[N]}$ is thereby suppressed to −11.72 V. As shown in Fig. 6(b), the rising times of CK1 and the output waveform become 2.11 μs and 2.54 μs, which are less than those in the previously developed circuit because the leakage current is lower. The rising time of the output waveform is improved by 21.36% ((3.23 us-2.54 us)/3.23 us × 100%). Therefore, the capacitance at node $Q_{[N]}$ becomes a crucial factor in the application of the capacitive coupling method to the gate driver.

The performance of the previously developed gate driver is affected by the total capacitance of C1 and C2 in series. Since C1 in both circuits is used to bootstrap the gate voltage of T2 before the gate driver generates output pulse, the capacitance of C2 determines the leakage current. Fig. 7 plots the variation of the leakage current, rising times, and falling times of the clock signal and output waveforms of the previously developed circuit with varying capacitance. Herein, the capacitance of C1 is fixed at 2 pF. Since the leakage current of T2 declines from 24.98 μA to 16.94 μA as the capacitance of C2 increases from 0.5 pF to 4 pF, the rising time of the output waveform is shortened to 2.98 μs. Based on the results in Figs. 5 to 7, the leakage current of T2 dominates the rising time of the output waveform. Herein, to reduce the leakage current that is induced by the clock-feed-through effect, the capacitances of C1 and C2 are set equal, and the rising and falling times of the output waveform are investigated. Fig. 8(a) shows that, since the capacitance of the proposed circuit is larger than that of the previously developed circuit, the leakage current of the proposed circuit is much lower. When the capacitances of C1 and C2 are increased from 2 pF to 5 pF, respectively, the leakage currents of the previously developed and proposed circuits are reduced from 19.69 μA and 10.74 μA to 7.83 μA and 1.34 μA. As shown in Fig. 8(b), to achieve the same rising time of 2.54 μs that was generated by the proposed circuit, the capacitances of C1 and C2 of the previously developed circuit must be set to 4 pF and 4 pF, respectively, so the layout area is much greater. The proposed circuit can improve the rising and falling times of the output waveform and allow for a smaller circuit area than that of the previously developed circuit.

IV. CONCLUSION

An a-Si:H TFT gate driver that exploits a new capacitive coupling method with less delay of the clock signal is reported upon. Owing to the removal of storage capacitors in series, the proposed circuit can suppress the leakage current flowing from the clock signal to V_L through the pull-up and pull-down TFTs, avoiding the increase in the rising time of the clock signal. Simulated results indicate that the leakage current is 8.95 μA lower than that of the previously developed circuit. The rising time of the output waveform is thus improved by 21.36%. Moreover, the proposed circuit has a smaller layout area without higher capacitances of the storage capacitors, which would make the bezel of a display in which they are used smaller.

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