Design and Analysis of a 28GHz 9KV ESD-Protected Distributed Travelling-Wave TRx Switch in 22nm FDSOI

FEILONG ZHANG [1], **CHENG LI**[1], **MENGFU DI** [1], **ZIJIN PAN**[1], **CHAOJIANG LI**[2], **NED CAHOON**[2], **AND ALBERT WANG** [1] **(Fellow, IEEE)**

1 Department of Electrical and Computer Engineering, University of California at Riverside, Riverside, CA 92507, USA
2 GlobalFoundries, Essex Junction, VT 05452, USA

CORRESPONDING AUTHOR: A. WANG (e-mail: aw@ece.ucr.edu)

This paper is based on a paper entitled "A 28GHz SPDT TRx Switch with 9KV ESD Protection in 22nm SOI CMOS for 5G Mobiles," presented at the 2019 IEEE S3S Conference.

ABSTRACT This paper presents design and analysis of a 28GHz broadband single-pole double-throw (SPDT) distributed travelling-wave radio-frequency (RF) switch designed in a foundry 22nm fully-depleted silicon-on-insulator (FDSOI) CMOS technology. The 28GHz SPDT transmitter-receiver (TRx) switch covers the n257 and n258 bands of the fifth-generation (5G) mobile wireless systems. Measurements show compatible switch performance to similar millimeter-wave (mm-wave) RF switches of various topologies designed in compound semiconductor high-electron-mobility transistor (HEMT) and Si bulk CMOS technologies. The SPDT switches achieve the highest reported 9KV ESD protection in measurements. It reveals that the ESD-induced parasitic effects have substantial impacts on mm-wave broadband RF switches. Careful ESD-RFIC co-design is suggested for designing 5G RF switches in above-6GHz bands.

INDEX TERMS 5G, TRx, switch, SOI, ESD, travelling wave, SPDT.

I. INTRODUCTION

RF switches are indispensable components to the RF front-ends (RFFE) ICs for smartphone systems. Nowadays, high-end RFFE modules supporting 4G/LTE mobiles typically contain many RF switches, as depicted in Fig. 1, including TRx switches, band switches that are usually integrated into power amplifier modules including duplexers (PAMiD) or low-noise amplifier (LNA) modules, and antenna switches that include coupler to support envelope tracking (ET) for PA and antenna tuner to enlarge frequency covering range. To support carrier aggregation, output switch/Mux is needed to handle signals from primary receiving (PRx) path, diversity receiving (DRx) path and multiple-input-multiple-output (MIMO) path. Since emerging 5G mobile systems involve rich frequency bands and heavy carrier aggregation, more and various RF switches are needed in 5G systems. Meanwhile, RF switches are vital to antenna configurations in 5G to improve quality of service (QoS). For example, sounding reference signal (SRS) switch is utilized in RFFE to hop transmissions to any receiving downlink antenna port, which calibrates the MIMO channel and improve the downlink signal-to-noise ratio (SNR). In 5G time division duplexing (TDD) systems, the SRS switch also allows 5G next-generation node base stations (gNB) to evaluate cell channel state information, which is critical to MIMO performance at high frequency. To achieve higher data rates, 5G new radios (NR) are being developed for sub-6GHz and mm-wave bands, which mostly utilize TDD transceiver architectures in mm-wave bands. To achieve low time latency, 5G systems have restrictive RF switching time requirements. To improve the power efficiency and sensitivity of transceivers, RF switches require low insertion loss (IL) and high isolation (Iso). In short, RF switches are key components in 5G systems and above-6GHz RF switch design is extremely challenging.

Major research efforts have been devoted to RF switch designs in mm-wave bands globally. Millimeter-wave single-pole multi-throw switches were demonstrated in high
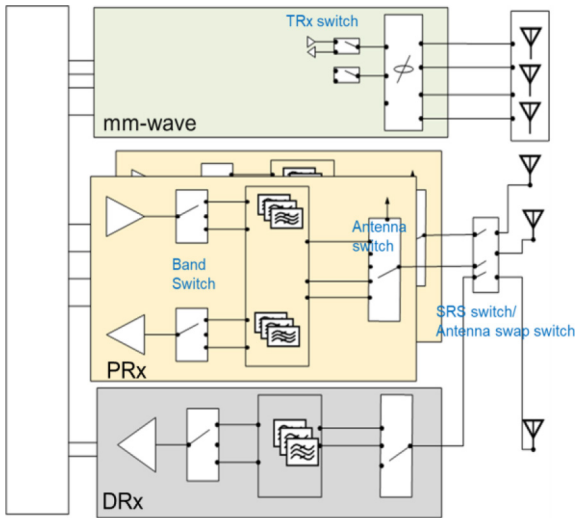
FIGURE 1. An illustration of a simplified 5G RF front-end architecture, which utilizes many and various RF switches in different blocks, such as SRS switches, antenna switches, band switches and TRx switches.
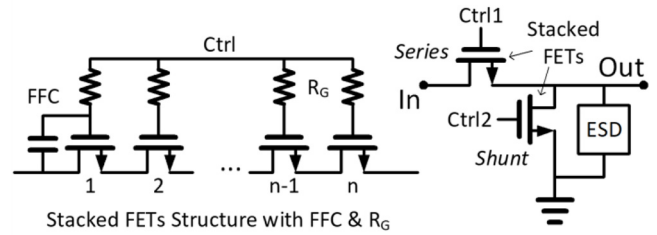

FIGURE 2. Topology of a 28GHz series-shunt SPDT with ESD protection designed in a 45nm SOI shows serious ESD-induced degradation of switch performance [3].
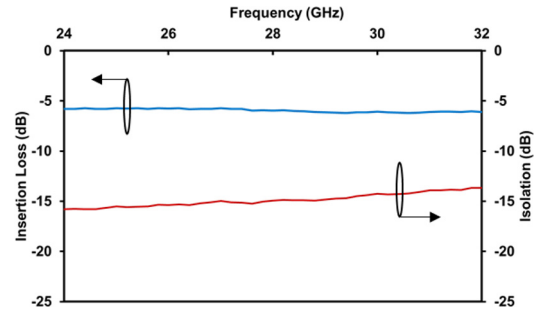

FIGURE 3. Measured IL and Iso for the ESD-protected 28GHz serious-shunt switch designed in a 45nm SOI CMOS shows poor insertion loss and isolation due to ESD-induced parasitic effects [3].

performance HEMTs for up to 100GHz [1] and bulk CMOS. However, III-IV technologies are naturally incompatible to Si integration, while bulk CMOS processes are inherently parasitic-heavy and noisy, both unsuitable for high-performance RF SoC integration with RF front-ends. SOI technologies, featuring ultralow parasitic capacitance and perfect isolation, become attractive for RF ICs for 5G NR systems. Particularly, fully-depleted SOI (FDSOI) technology is attractive to RF switch designs because it has no kink-effect and allows floating body to improve switch performance. FDSOI technologies have the potential for highly integrated 5G systems including baseband and mm-wave circuit domains. This paper discusses design detail of the SPDT switch in Sections II and III and the ESD design and characterization details in Sections IV and V.

II. ABOVE-6GHZ RF SWITCH TOPOLOGIES
To support TDD in mm-wave bands, single pole double throw (SPDT) switch is needed to switch signals between transmitting and receiving channels (i.e., TRx switch). In sub-6GHz systems, series-shunt switch topology has been popular, which delivers excellent switch performance including a flat frequency response. In a series-shunt switch, the transistor on-state resistance (R_{on}) determines insertion loss (IL), while the transistor off-state capacitance (C_{off}) dictates isolation (Iso). Both R_{on} and C_{off} are related to the transistor size, and the figure of merit (FOM), $R_{on}xC_{off}$, is process technology limited. For advanced SOI technologies, a FOM of lower than 100fs is achievable, which ensures good switch performance across a several GHz range [2]. Unfortunately, series-shunt switches suffer from severe performance degradation in the above-6GHz bands, such as in the 28GHz/38GHz bands, due to significant leakage through OFF branches as frequencies increase [3]. We previously reported design of a series-shunt 28GHz TRx

switch fabricated in a foundry 45nm SOI process, which features a feed-forward coupling capacitor topology to balance voltage distribution across transistors in the FET stacks and therefore improve switch linearity as depicted in Fig. 2. Fig. 3 presents the measured insertion loss and isolation for the series-shunt 28GHz switch, which shows poor switch performance, e.g., a high insertion loss of 5dB and isolation worse than 17dB, mainly due to the poor transistor behaviors at high frequency. Modification to the conventional series-shunt topology may be made to improve switch performance. For example, a stress memorization technique was reported to achieve better FOM to improve insertion loss and isolation of conventional series-shunt FET based switches by enhancing channel mobility of transistors [4]. Using on-chip inductor matching techniques to resonate out the parasitic capacitance of FETs were also reported, but it is limited by the availability of high-performance on-chip inductors in CMOS, such as the quality factor [5], [6]. Moreover, L-C matching network is intuitively narrow band. Alternatively, travelling wave switch topology becomes attractive for broadband mm-wave switches in GaAs HEMT and bulk CMOS [7]. Travelling wave switch consists of inductive transmission lines and transistors used to control switch impedance. For travelling wave SPDT switches, a quarter-wave line is often used to transfer the low impedance off branch to high impedance state. However, a quarter-wave line covers a narrow band only and takes large chip area, which make it unsuitable for 5G chips because a 5G mobile system requires a large number of high-performance RF switches, in the meantime also require small chip footprint. Additionally,
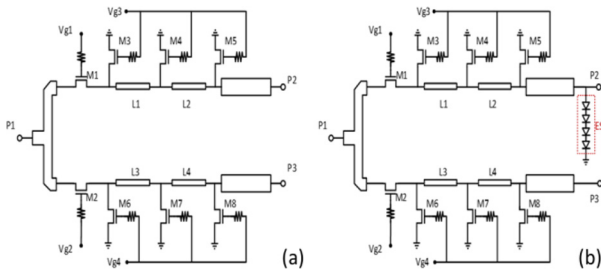
FIGURE 4. Schematic of the 28GHz traveling wave SPDT switch designed in this work: (a) SPDT without ESD protection, and (b) SPDT with 4-diode-string ESD protection.
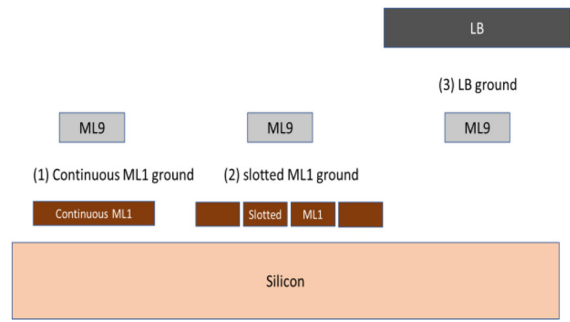

FIGURE 5. Illustration of microstrip line design splits, all using the same mid-layer ML9 as Signal line, but featuring different Ground lines: Case-1: continuous ML1 as Ground line (violating Foundry Design Rules); Case-2: slotted ML1 as Ground (following Foundry Design Rules); and Case-3: continuous top metal LB as Ground (allowed by Foundry Design Rules).

a series transistor can be used in a travelling wave switch to achieve high off branch impedance. It is generally considered that traveling wave topologies of various versions should be used to design high-performance RF switches for 5G systems operating in the above-6GHz bands, particularly in 28GHz/38GHz and beyond bands.

III. DISTRIBUTED TRAVELING-WAVE SPDT DESIGN

This paper, an extended version of our S3S paper [8], discusses in detail the design and analysis of a distributed travelling-wave 28GHz mm-wave SPDT switches fabricated in a foundry 22nm FDSOI CMOS for 5G mobile systems with robust on-chip ESD protection. Fig. 4 depicts the schematics of the SPDT travelling-wave switches. The 28GHz mm-wave SPDT switch features a three-stage travelling-wave topology consisting of distributed inductive transmission lines and controlling transistors. Considering the complex massive-MIMO architecture in mm-wave 5G systems, a switch size is major design concern. Therefore, we chose not to use the popular quarter-wave transmission line structure in this design because they would consume too much Si die area, and the long transmission line trace would also lead to higher insertion loss due to the non-ideal lossy transmission line nature. The series transistors (M1, M2) provide extra control of the switch status and improve the switch isolation. To ensure the ruggedness, thick oxide long channel nMOSFETs are used for the series and shunt controlling transistors (M1-M8), benefited from its higher gate breakdown voltage (BV_{DS}). Floating body connection is utilized to achieve better $R_{on}xC_{off}$ FOM in this 22nm FDSOI process. The MOSFET sizes are optimized together with the transmission lines. Considering the area limitation, transmission line segments are designed to be short for smaller inductance, and concurrently, the shunt transistors are designed with smaller size following $Z_0 = L/C$. M3-M8 are carefully sized to be L = 100nm and W = 20.3μm. The on-state resistance is designed to be 17Ω and off-state capacitance is set to 6.3fF. The drawback for using small size is the relatively larger device mismatch effect over the process, power and temperature (PVT) range. For M1 and M2, transistor size is chosen to be W=115μm and a minimum L=100nm, which achieves a good trade-off balance between switch insertion loss and isolation. Under a 1.8V operation voltage,

the on-state resistance is 3.6Ω and the off-state capacitance is 21.5fF for M1 and M2. A 10KΩ resistor is added to the gate to reduce the leakage. The distributed transmission line segments feature a characteristic impedance of 70Ω.

Careful design optimization for the transmission lines is vitally critical to the performance of the distributed traveling-wave switches, which was guided by comprehensive EM field simulation in this work. In this design, we choose to use microstrip lines because it consumes less area than co-planar waveguides and is easier to realize. Conventionally, microstrip lines in CMOS use the higher metal layer (e.g., ML9) as the signal line and the bottom metal (i.e., ML1 in this foundry 22nm SOI as depicted in Fig. 5, which is closer to the active devices in Si) as the ground plane. To form a Ground three times wider than a Signal line as required, the ML1 ground plane must be slotted as per the foundry Design Rules (DR) for metal filling density consideration in advanced CMOS, which, however, increases loss significantly due to the impedance discontinuity and ground resistance. Moreover, the repeated slots in ML1 lines will introduce substantial ripples in transmission line's character impedance, which can lead to serious distortion to signals in high frequency. Since the top layer metal (LB) has lower sheet resistance and the width can be designed wide without using the slots as required by the Design Rules as in ML1 case, we proposed a novel microstrip line design technique that uses the top LB metal, instead of the traditional bottom ML1 metal, to form the Ground line, while using the middle layer metal (ML9) as the signal line, as illustrated in Fig. 5. The disadvantage of this microstrip line structure may be that less electromagnetic field is expected inside the microstrip lines due to the high dielectric permittivity of materials under the signal line. A careful comparison study of the microstrip line layout impacts on the 50Ω transmission lines in this foundry 22nm SOI CMOS process was conducted by EM field simulation using HFSS. The EM filed simulation involved three microstrip line layout splits: Case-1 and Case-2 use the middle ML9 metal as the Signal lines and the wide bottom ML1 metal as the Ground lines, with the ML1 being slotted for Case-2 (per the
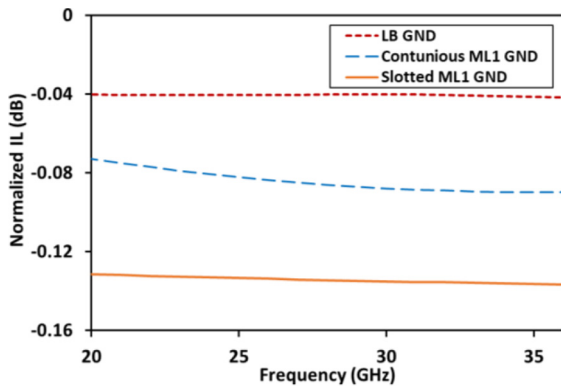
FIGURE 6. HFSS simulation for the three microstrip line cases shows lowest IL when using our new non-slotted top-layer LB as Ground. (normalized to the same electrical length; characteristic impedance of all three case are 50ohm).
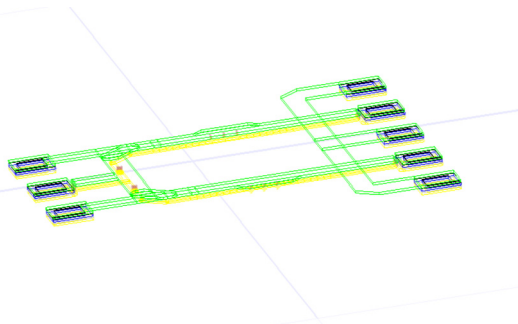

FIGURE 7. Illustration for the HFSS EM simulation deck for the microstrip lines used in travelling-wave switches created in the SOI CMOS BEOL stack.

foundry Design Rules), but non-slotted (continuous ML1) for Case-1 as a reference; Case-3 utilizes the middle ML9 as the Signal line while the topmost metal LB as Ground line. Fig. 6 presents the EM simulation comparison for the three cases, which clearly shows that Case-2 (slotted ML1 recommended by the Foundry) induces the worst loss, while our new LB-ML9 design in Case-3 achieves the lowest IL for the same electrical length. Therefore, Case-3 microstrip line layout pattern was used in this distributed travelling-wave switch design. In the design, parasitic resistance and capacitance of active controlling transistors are extracted for both on-state and off-state. Fig. 7 depicts the EM field simulation model for the back-end-of-the-line (BEOL) of the travelling-wave switch, including the testing pads and the transmission line, which are simulated using EM tools. In the EM simulation deck, the ports are set at each channel toward the active device (MOSFET). The whole switch circuit performance is optimized in Cadence with S-parameters extracted by HFSS.

IV. ESD PROTECITON DESIGN

ESD protection design is extremely challenging for high-frequency and broadband RF ICs [9]–[12], particularly for 5G mobile chips that utilize the above-6GHz bands,
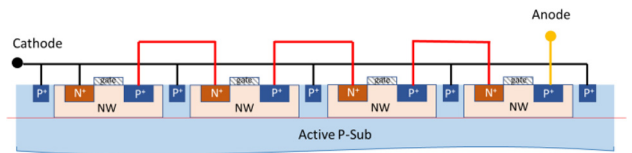

FIGURE 8. A cross-section illustration for the 4-gated-diode diode-string ESD protection structure designed in this work.
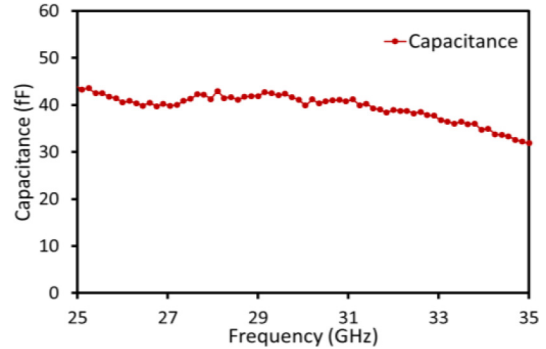

FIGURE 9. Measured parasitic C_{ESD} of the 4-diode diode-string ESD protection structures using a de-embedded method.

which are very sensitive to any ESD-induced parasitic effects including parasitic capacitance, leakage current and noises [9]. For smartphones to survive in real world applications, robust ESD protection for RF ICs becomes critical. In this work, we designed 9KV human body model (HBM) ESD protection for the 28GHz travelling-wave switches. Robust charged device model (CDM) ESD protection was also a key design consideration in this work. In this design, we chose to use a four-gated-diode diode-string ESD protection structure for the mm-wave switches. Fig. 8 depicts a cross-section for the 4-diode-string ESD protection structure where, uniquely, the oxide isolator layer in the SOI substrate was removed within the ESD layout area to improve the ESD heat dissipation in order to achieve higher ESD protection level. To optimize ESD protection while minimizing the inherent ESD-induced parasitic effects, comprehensive TCAD (technology computer-aided-design) ESD simulation was conducted using a mixed-mode ESD simulation technique [10]. To avoid the switch power dropout caused by ESD leakage, the ESD protection requires relatively high ESD triggering voltage (V_{t1}), which was designed as $V_{t1} \sim 2V$, to ensure 19dBm output power for this 28GHz mm-wave switch. Per TCAD ESD simulation, each diode in the ESD diode-string structure was designed to have a width of 300μm. Careful evaluation of the ESD-induced parasitic capacitance (C_{ESD}) was conducted to minimize its impact on switch performance at 28GHz. Fig. 9 shows the measured C_{ESD} results for the ESD diode-string structure across a wide 5G bandwidth.

V. MEASUREMENT AND ANALYSIS

The distributed travelling-wave 28GHz switches were fabricated in a foundry 22nm FDSOI technology. Fig. 10 shows
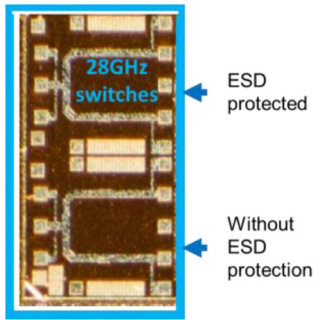
FIGURE 10. A die photo for the 28GHz SPDT switches with and without ESD protection fabricated in a foundry 22nm SOI CMOS.
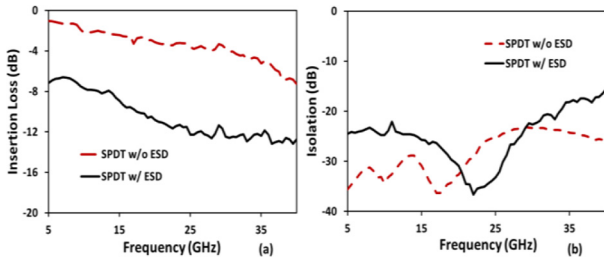

FIGURE 11. Measured switch performance of the 28GHz SPDT switches with and without 9KV ESD protection: (a) Insertion Loss, and (b) Isolation.
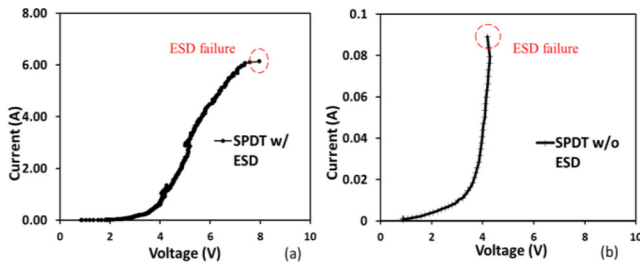

FIGURE 12. Measured ESD protection performance for the 28GHz SPDT switches at port 2 by standard TLP ESD testing for (a) SPDT with 9KV HBM ESD protection, and (b) SPDT without ESD protection.

TABLE 1. mm-wave switch performance comparison.

| Ref.	ESD	Process	Freq. (GHz)	Topologies	IL (dB)	Iso (dB)
[4]	No	130nm SOI	DC-50	Series-shunt with mobility enhancement	<2.1	>27
[5]	No	65nm CMOS	25-39.5	Series-shunt with matching inductor	<1.9	>25
[6]	No	180nm SOI	DC-40	Series-shunt with matching inductor	<5	>17
[7]	No	90nm CMOS	DC-60	Travelling wave	<3	>48
[13]	No	180nm CMOS	DC-50	Travelling wave	<6	>26
[14]	No	130nm CMOS	DC-28	Series-shunt with enhanced body floating	<2.5	>15
This work	**No**	**22nm FD-SOI**	**DC-30**	**Travelling wave without ESD protection**	**<3.9**	**>23**
This work	**9KV**	**22nm FD-SOI**	**DC-30**	**Travelling wave with ESD protection**	**<12.6**	**>22**
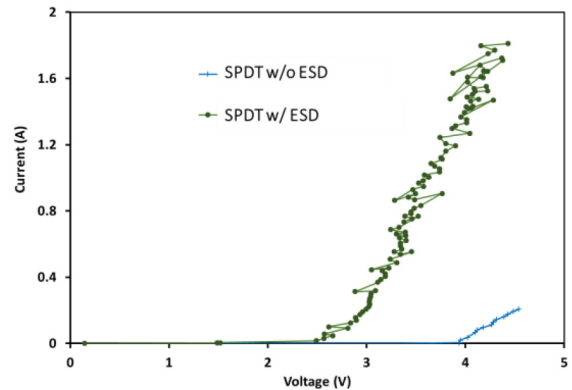
FIGURE 13. Measured ESD protection performance for the SPDT switches at port 2 by standard VFTLP ESD testing for CDM ESD protection for the 28GHz SPDT switches with (green line) and (blue line) ESD protection.

a die photo for the 28GHz SPDT switch that has a chip size of 0.66×0.64 mm² (including GSG test pads). Bare die S-parameter measurement was conducted using a Cascade RF probe station and an Agilent-E8363B across the 5GHz to 40GHz spectrum. Fig. 11 shows the measured S-parameters for the 28GHz SPDT switches. There are two switch design splits: SPDT without ESD protection and SPDT with ESD protection. From 5GHz to 20GHz, the SPDT switch without ESD protection achieves insertion loss range of 1.0dB to 3.1dB and isolation better than 30dB. Across the n257 and n258 bands (24.25-29.5GHz) for 5G applications, the insertion loss is better than 3.9dB and the isolation is better than 23dB. The performance of the distributed traveling-wave 28GHz switches without ESD protection is generally comparable to the reported state-of-the-art mm-wave switches of various different topologies (Table 1) [4]–[7], [13], [14]. Comprehensive ESD characterization was performed using

transmission line pulsing (TLP) testing (ESD pulse rising time of 10ns and duration of 100ns, Barth Model 4002 TLP Tester) for HBM ESD protection and very-fast TLP (VFTLP) testing (ESD pulse rising time of 1ns and duration of 10ns, Barth Model 4012 VFTLP Tester) for ultrafast CDM ESD protection performance for the 28GHz switches. Fig. 12 presents the TLP ESD testing results for the 28GHz SPDT switches (port 2), which clearly shows that the ESD-protected SPDT achieves on-chip HBM ESD protection of at least 9KV as designed; as a comparison, the SPDT without ESD protection failed at a very low ESD stressing level of lower than 150V (some self ESD protection exists). Fig. 13 gives the VFTLP ESD testing results (port 2). It was observed that the diode-string ESD protection structure can protect the SPDT switch against ultrafast CDM ESD stressing up to 1.8A; while in comparison, the SPDT without ESD protection failed at a low CDM ESD stressing level of 0.2A. Analysis of ESD parasitic impacts on SPDT

performance was conducted. While it is worth noting that, to our best knowledge, this may be the first reported travelling-wave mm-wave SPDT designed in FDSOI with a center frequency of 28GHz for 5G systems featuring 9KV HBM ESD protection; Fig. 11 clearly shows that the on-chip ESD protection structure, though optimized by ESD simulation, still substantially affects the SPDT specs, i.e., causing a large degradation of insertion loss by ∼6dB at low frequency and ∼8.7dB at 28GHz. This inherent ESD-induced degradation in switch performance was mainly because the lack of SOI process data (Foundry confidential) that is required to ensure ESD simulation accuracy in this design. This work clearly shows that the inherent ESD-induced parasitic effect is inevitable and will affect switch performance in mm-wave bands. It is strongly suggested that careful ESD-RFIC co-design must be conducted for mm-wave switch designs, regardless whether ESD simulation is performed for the individual ESD protection structures [12].

VI. CONCLUSION

This paper reports details of design and analysis of the first 9KV ESD-protected 28GHz distributed traveling wave based SPDT switch designed and fabricated in a foundry 22nm FD-SOI technology for 5G n257 and n258 bands. EM simulation was conducted to optimize the physical layout design of the microstrip lines. The measured insertion loss and isolation are comparable to the state-of-the-art mm-wave switches designed in HMET and bulk CMOS with various topologies. ESD testing shows the highest reported on-chip ESD protection for mm-wave switches up to 9KV in HBM ESD mode and 1.8A in CDM ESD mode. Analysis also shows that mm-wave switches can be seriously affected by ESD protection. It is clear that careful ESD-RFIC co-design is needed for mm-wave switches to achieve high switch performance and ESD robustness simultaneously. This work also shows that distributed travelling wave based mm-wave switches in FDSOI is a viable solution for 5G systems in above-6GHz bands, opening a door for future RF SoC designs.

ACKNOWLEDGMENT

REFERENCES

[1] J. Kim, W. Ko, S-H. Kim, J. Jeong, and Y. Kwon, "A high-performance 40–85 GHz MMIC SPDT switch using FET-integrated transmission line structure," *IEEE Microw. Compon. Lett.*, vol. 13, no. 12, pp. 505–507, Dec. 2003.

[2] A. Balasubramaniyan and A. Bellaouar, "RF/mmWave front-end module switch in 22nm FDSOI process," in *Proc. IEEE SOI 3D Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, 2018.

[3] C. Wang *et al.*, "A study of impacts of ESD protection on 28/38GHz RF switches in 45nm SOI CMOS for 5G mobile applications," in *Proc. IEEE Radio Wireless Symp. (RSW)*, 2018, pp. 157–160.

[4] B. Yu *et al.*, "Ultra-wideband low-loss switch design in high-resistivity trap-rich SOI with enhanced channel mobility," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 10, pp. 3937–3949, Oct. 2017.

[5] W. Lee and S. Hong, "Low-loss and small-size 28 GHz CMOS SPDT switches using switched inductor," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, 2018, pp. 148–151.

[6] A. S. Cardoso, P. Saha, P. S. Chakraborty, D. M. Fleischhauer, and J. D. Cressler, "Low-loss, wideband SPDT switches and switched-line phase shifter in 180-nm RF CMOS on SOI technology," in *Proc. IEEE Radio Wireless Symp. (RWS)*, 2014, pp. 199–201.

[7] H.-Y. Chang and C.-Y. Chan, "A low loss high isolation DC-60 GHz SPDT traveling-wave switch with a body bias technique in 90 nm CMOS process," *IEEE Microw. Compon. Lett.*, vol. 20, no. 2, pp. 82–84, Feb. 2010.

[8] F. Zhang *et al.*, "A 28GHz SPDT TRx switch with 9KV ESD protection in 22nm SOI CMOS for 5G mobiles," in *Proc. IEEE SOI 3D Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, 2019.

[9] A. Z. H. Wang *et al.*, "A review on RF ESD protection design," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1304–1311, Jul. 2005.

[10] H. Feng *et al.*, "A mixed-mode ESD protection circuit simulation-design methodology," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 995–1006, Jun. 2003.

[11] F. Lu *et al.*, "A systematic study of ESD protection co-design with high-speed and high-frequency ICs in 28nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 10, pp. 1746–1757, Oct. 2016.

[12] X. S. Wang *et al.*, "Concurrent design analysis of high-linearity SP10T switch with 8.5kV ESD protection," *IEEE J. Solid-State Circuits*, vol. 49, no. 9, pp. 1927–1941, Sep. 2014.

[13] M.-C. Yeh, Z.-M. Tsai, and H. Wang, "A miniature dc-to-50 GHz CMOS SPDT distributed switch," in *Proc. Eur. Gallium Arsenide Semicond. Appl. Symp. (GAAS)*, 2005, pp. 665–668.

[14] Q. Li, Y. P. Zhang, K. S. Yeo, and W. M. Lim, "16.6- and 28-GHz fully integrated CMOS RF switches with improved body floating," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 2, pp. 339–345, Feb. 2008.

FEILONG ZHANG received the B.S. degree from the University of Science and Technology of China in 2015, and the Ph.D. degree in electrical and computer engineering from the University of California at Riverside, Riverside, CA, USA, in 2018. He is currently an RF Design Engineer with Qualcomm. His research interests include RF front-end circuit designs for 5G applications and ESD protection design and simulation in advanced technologies.

CHENG LI received the B.E. degree in electrical engineering from Xidian University, China, in 2012, and the M.S. degree in electrical engineering from the University of Southern California, USA, in 2015. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, University of California at Riverside, Riverside, CA, USA. His research interests include ESD protection designs, thermal, and power management ICs.

MENGFU DI, photograph and biography not available at the time of publication.

ZIJIN PAN received the B.S. degree from the University of Science and Technology of China in 2018. She is currently pursuing the Ph.D. degree in electrical and computer engineering with the University of California at Riverside, Riverside, CA, USA. Her current research interests include visible light communication SoC design and ESD protection design for ICs.

CHAOJIANG LI, photograph and biography not available at the time of publication.

NED CAHOON, photograph and biography not available at the time of publication.

ALBERT WANG (Fellow, IEEE) is a Professor of electrical and computer engineering with the University of California at Riverside, Riverside, CA, USA. He has authored one book and over 270 peer-reviewed papers. He holds 16 U.S. patents. He was the President of IEEE Electron Devices Society. He is a Fellow of National Academy of Inventors.