Received 5 September 2019; revised 12 October 2019; accepted 9 February 2020. Date of publication 17 February 2020; date of current version 26 February 2020.
The review of this paper was arranged by Editor K. Shenai.

Digital Object Identifier 10.1109/JEDS.2020.2974186

Trench Shielded Planar Gate IGBT (TSPG-IGBT) With Self-Biased pMOS Realizing Both Low On-State Voltage and Low Saturation Current

RONGXIN CHEN, BO YI (Member, IEEE), AND XING BI CHEN (Fellow, IEEE)

State Key Laboratory of Electronic Thin Films and Integrated Devices of China, University of Electronic Science and Technology of China, Chengdu 610054, China

CORRESPONDING AUTHOR: B. YI (e-mail: yb@uestc.edu.cn)

This work was supported in part by the National Natural Science Foundation of China under Grant 61804021, and in part by the Fundamental Research Funds for the Central Universities under Grant ZYGX2019J020.

ABSTRACT A novel trench shielded planar gate IGBT (TSPG-IGBT) with self-biased pMOS is proposed in this paper. It features a P-layer beneath the trench of the TSPG-IGBT to form a self-biased pMOS, which provides an additional path for the hole current and clamps the potential of the nMOS's intrinsic drain for lower saturation current. In the off-state, with the increasing potential of the N-cs (N-doped carrier store layer), the self-biased pMOS turns on and the potential of the P-layer will be clamped by the hole channel. Then, the reverse voltage is sustained by the P-layer/N-drift junction and the potential of the N-cs is shielded by the clamped P-layer region. Therefore, the N-cs can be heavily doped to reduce the on-state voltage (V_{on}) without decreasing the breakdown voltage. Compared with the conventional TSPG-IGBT, the V_{on} of the proposed TSPG-IGBT is reduced by 0.3 V at the current density of 200 A/cm^2 with the same turn-off loss. Besides, the saturation current density of the proposed one is decreased by 24%.

INDEX TERMS Insulated gate bipolar transistor (IGBT), self-biased pMOS, on-state voltage, saturation current, turn-off loss.

I. INTRODUCTION

The insulated gate bipolar transistor (IGBT) is widely used in power electronics. The compromise among on-state voltage (V_{on}), turning-off loss (E_{off}) and short circuit safe operating area (SCSOA) is the key issue need to be considered in the design of IGBTs. The IEGT (Injection Enhanced Gate Transistor) [1]–[3] and the CSTBT (Carrier Store Trench Bipolar Transistor) [4]–[5] were introduced to reduce the on-state voltage V_{on}. In the CSTBT, with the increase of the doping concentration of the N-cs (N-doped carrier store layer), the V_{on} of the IGBT is reduced and a better trade-off between V_{on} and E_{off} can be obtained. However, with the increasing dose of the N-cs, the breakdown voltage of the IGBT decreases dramatically [4]. In [6]–[13], the charge compensation can be used to increase the doping concentration of the N-cs without sacrificing the breakdown voltage. In [14], the trench shielded planar gate IGBT (TSPG-IGBT) balances the charge by using a deep trench. However, the dose of the N-cs (D_{ncs}) needs to be completely depleted when sustaining high voltage. The doping concentration of the N-cs (N_{ncs}) is still limited. In [15], [16], clamping the potential of nMOS's intrinsic drain with self-biased pMOS allows a further increasing N_{ncs} and decreases the saturation current density, as the D_{ncs} doesn't need to be completely depleted when sustaining high voltage.

In this paper, a novel trench shielded planar gate IGBT (TSPG-IGBT) with self-biased pMOS is proposed and investigated by TCAD tools. Due to the combination of the "self-clamping" effect and the trench charge compensation, the N_{ncs} can be further improved without compromising the blocking capability and the saturation current density is also reduced which enlarges the SCSOA.

II. DEVICE STRUCTURE AND MECHANISM

As shown in Fig. 1(b), the proposed structure has the same source trench and planar gate as the conventional TSPG-IGBT which is shown in Fig. 1(a). To enhance the electron injection at the cathode side, a heavily doped N-cs is

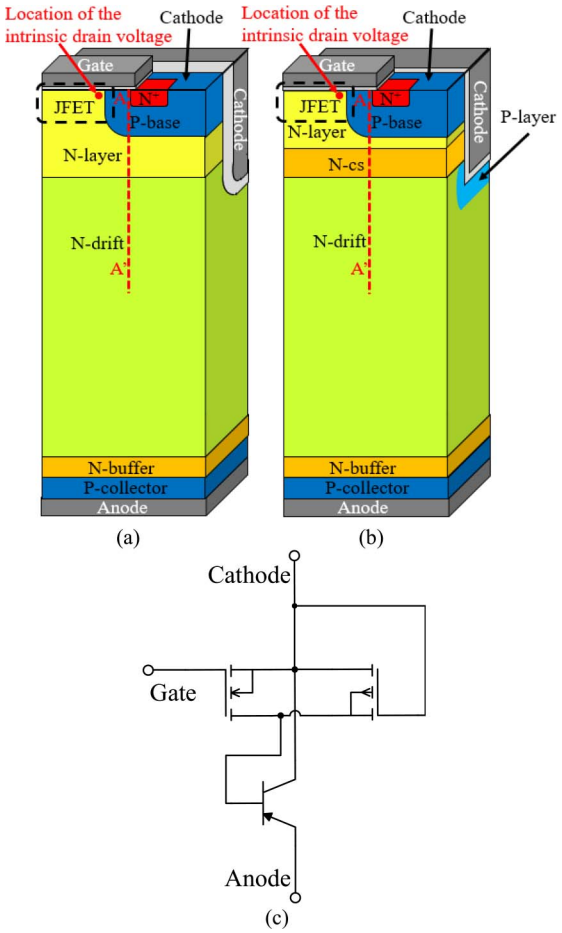

FIGURE 1. **(a) Conventional structure: Trench Shielded Planar Gate IGBT (TSPG-IGBT). (b) Proposed structure: Trench Shielded Planar Gate IGBT with self-biased pMOS. (c) Simplified equivalent circuit for the proposed structure.**

formed beneath the N-layer in the proposed TSPG-IGBT. To shield the potential of the N-cs, an additional P-layer under the source trench is introduced. The P-layer, N-cs/N-layer and the P-base as well as the source trench form a pMOS.

During the off-state, with the increasing potential of the anode, the potential of the N-cs increases. When the potential of the N-cs is more than the absolute value of the threshold voltage of the pMOS (V_{thP}), the pMOS will be automatically turned on. The P-layer will be connected to the cathode through the hole channel and the potential of the P-layer will be clamped at a low value. The further increased anode potential will be sustained mainly by the P-layer/N-drift junction. Consequently, the potential of the N-cs and the N-layer is shielded at a low value. Therefore, the N-cs can be heavily doped to obtain a lower V_{on} before the breakdown occurs at the reverse biased P-base/N-layer junction.

During the on-state, the heavily doped N-cs enhances the electron injection at the cathode and reduces the conduction loss. As the potential of the anode rises, pMOS is turned on and the potential of P-layer is clamped. As long as the region of the N-drift sandwiched by the P-layer is fully depleted, the potential of the N-layer and the N-cs are clamped at

TABLE 1. **Device specifications.**

Parameters	Value
Threshold voltage of the nMOS, V_{thN} (V)	5.6
N-drift doping, N_{ND} (cm^{-3})	1×10^{14}
N-drift thickness, T_{ND} (μm)	45
P-base thickness, T_{PB} (μm)	2.5
N-layer thickness, T_{NL} (μm)	5
P-layer peak doping, N_{PL} (cm^{-3})	3×10^{17}
P-layer thickness, T_{PL} (μm)	3
P-layer gap width, W_{PL} (μm)	0.5

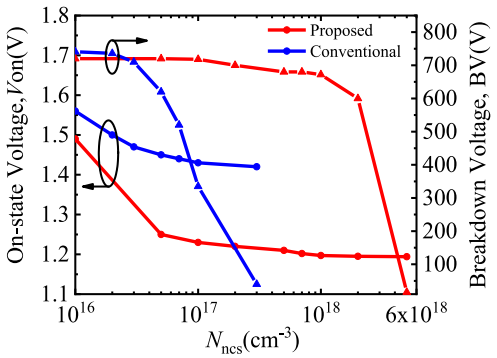

FIGURE 2. **Effect of the breakdown voltage and V_{on} depending on N_{ncs}.**

a low value by the hole channel. Because the N-layer and N-cs serve as the intrinsic drain of the nMOS, a lower saturation current density can be obtained in the proposed structure compared with that of the conventional one. As the potential of the nMOS's intrinsic drain (V_{ND}) is determined by the clamped potential, the length of the channel can be reduced to improve the conduction performance without increasing the saturation current density. Consequently, the on-state voltage is reduced by reducing the channel length and increasing the doping concentration of N-cs, and the saturation current density is adjusted by designing different threshold voltage of the pMOS (V_{thP}). In other words, the on-state voltage and the saturation current density of the proposed structure can be varied separately.

III. SIMULATION RESULTS AND DISCUSSIONS

A. STATIC CHARACTERISTICS

Fig. 2 shows the effect of N_{ncs} on the breakdown voltage and the on-state voltage at $J_A = 200$ A/cm^2. In the conventional structure, with N_{ncs} increasing from 1×10^{16}cm^{-3} to 3×10^{17} cm^{-3}, the on-state voltage decreases from 1.56 V to 1.42 V, but its breakdown voltage reduces dramatically from 742 V to 40 V. In the proposed structure, the breakdown voltage begins to reduce when N_{ncs} increases to 1×10^{18} cm^{-3}. This is because the pMOS clamps the potential of the nMOS's intrinsic drain in the off-state, the reverse voltage is mainly sustained by the P-layer/N-drift junction, shown in Fig. 3.

Fig. 3 compares the potential distribution and depletion lines of the conventional structure and the proposed structure at BV = 700 V. In the proposed structure, the reverse voltage

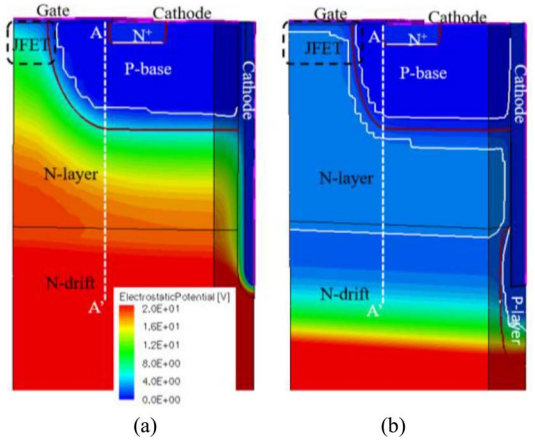

FIGURE 3. Potential distribution and depletion lines of (a) the conventional structure and (b) the proposed structure in reverse state ($V_{Gate} = 0$ V). White lines are depletion lines. Red lines are the metallurgical junction interfaces.

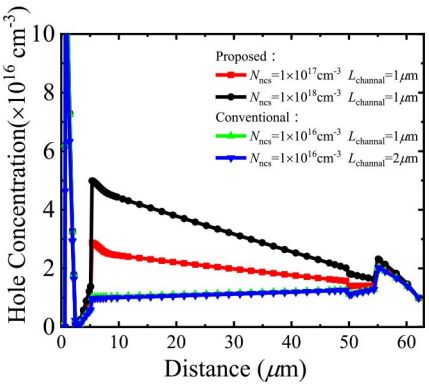

FIGURE 4. Hole concentration distributions along line AA' at $J_A = 200$ A/cm^2.

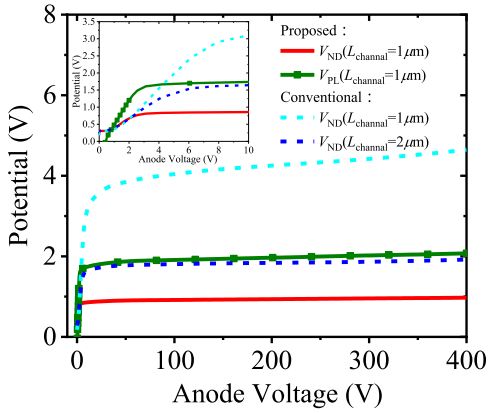

FIGURE 5. Dependences of the potential of nMOS's intrinsic drain (V_{ND}) and the potential of the P-layer (V_{PL}) upon the anode voltage.

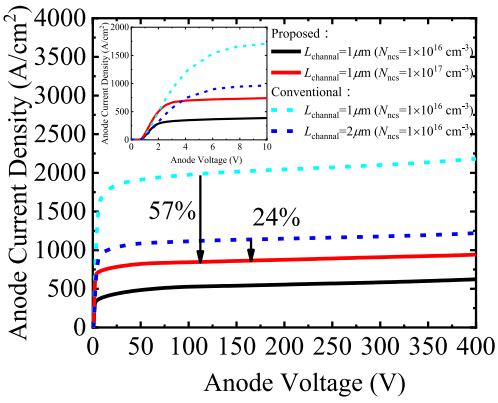

FIGURE 6. Effect of channel length on saturation current density and conduction voltage drop.

is sustained by the P-layer/N-drift junction rather than the P-base/N-layer junction. The N-layer does not need to be fully depleted to sustain the high voltage. Therefore, the N-cs can be heavier doped to reduce the conduction voltage without sacrificing breakdown voltage.

Fig. 4 shows the distributions of the hole concentration along line AA' at anode current density $J_A = 200$ A/cm^2. The higher value of the N_{ncs} contributes to a higher hole carrier density near the cathode side, which improves the on-state conductivity significantly.

For the conventional TSPG-IGBT, shortening of the channel length means that the JFET region is wider, which results in a higher potential at the intrinsic drain of the nMOS in the on-state, as shown in Fig. 5. V_{ND} is about 4.5 V for the conventional one with channel length $L_{channel} = 1\mu$m. While, for the proposed one, the V_{PL} is clamped at about 1.7 V after the anode voltage raises over 3V. Because the V_{ND} is shielded by the clamped P-layer voltage (V_{PL}), the V_{ND} is only about 1 V, even when the channel length is 1 μm. Higher V_{ND} and shorter channel result in larger electron current density for the conventional one. Therefore, for the conventional TSPG-IGBT, the saturation current density is much larger than that of the proposed one, as shown in Fig. 6.

Fig. 6 shows the influence of $L_{channel}$ and N_{ncs} on the current density of the conventional and the proposed TSPG-IGBT. For the conventional one, with the decrease of $L_{channel}$, the V_{on} decreases. However, the saturation current density increased dramatically which jeopardizes the SCSOA. For the proposed device with $L_{channel} = 1\mu$m and $N_{ncs} = 1\times10^{16}$ cm^{-3}, the V_{on} is large and the saturation current density is too small due to the premature turned on of the pMOS, which is not enough for surge current. With $N_{ncs} = 1\times10^{17}$ cm^{-3}, the V_{thP} goes up and the P-layer is clamped at a higher value which increases the barrier for holes flowing from the N-drift [17]. The barrier causes a large number of holes to be blocked at the cathode which reduces V_{on} of the device [18]. The anode saturation current density is also improved but still restricted at a low value by the clamped P-layer for larger SCSOA.

As shown in Fig. 7, the clamped-potential of the P-layer increases from 1.2 V to 7.1 V with the increasing N_{ncs} (from 1×10^{16}cm^{-3}to 2×10^{18}cm^{-3}), due to the higher threshold voltage of the pMOS [19]. Then, the clamped-potential of nMOS's intrinsic drain and the anode saturation

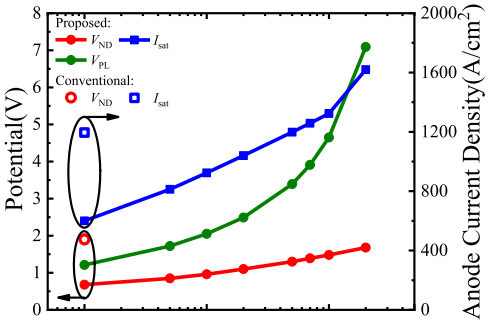

FIGURE 7. Effect of the clamped-potential of nMOS's intrinsic drain (V_{ND}), the clamped-potential of the P-layer (V_{PL}) and the saturation current density (I_{sat}) depending on N_{ncs}.

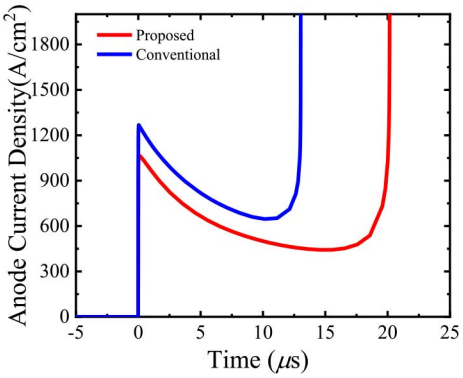

FIGURE 8. Comparison of SCSOA of the proposed structure with the conventional structure (V_{bus} = 400 V).

current density also increase, as shown in Fig. 7, which will jeopardize the breakdown voltage (as shown in Fig. 2) and the Short Circuit Safe Operation Area (SCSOA). When $N_{ncs} = 5 \times 10^{17}$cm^{-3}, the saturation current density of the proposed one equals to that of the conventional one, which indicates they have an approximate SCSOA.

Fig. 8 compares the SCSOA of the proposed structure with the conventional structure. Owing to the smaller saturation current density when $N_{ncs} = 1 \times 10^{17}$ cm^{-3}, the SCSOA of the proposed structure is about 1.75 times larger than that of the conventional structure.

B. TRANSIENT CHARACTERISTICS

Fig. 9 compares the trade-off relationship between V_{on} and E_{off} by varying the doping concentration of P-collector. At $E_{off} \approx 3.5$ mJ/cm^2, the on-state voltage of the proposed one with $N_{ncs} = 1 \times 10^{17}$ cm^{-3} is reduced by 0.3 V, compared with that of the conventional structure.

Fig. 10 shows the turn-off waveforms of the proposed and the conventional structure. Even though the doping concentration of the P-collector (N_{pcol}) for the proposed one is reduced from 2×10^{16} cm^{-3}to 1×10^{15}cm^{-3}, both structures have the same on-state voltage (about 1.5 V). The E_{off} of the proposed and conventional devices are 0.88 mJ/cm^2 and 3.58 mJ/cm^2, respectively. The E_{off} of the proposed one is reduced by about 75.4% even though the turn-off delay time

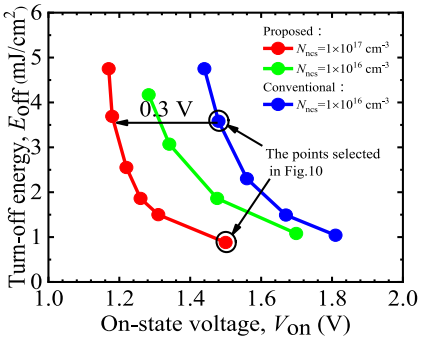

FIGURE 9. Trade-off relationship between the E_{off} and V_{on} at turn-off current density of 200 A/cm^2 and V_{bus} = 400 V.

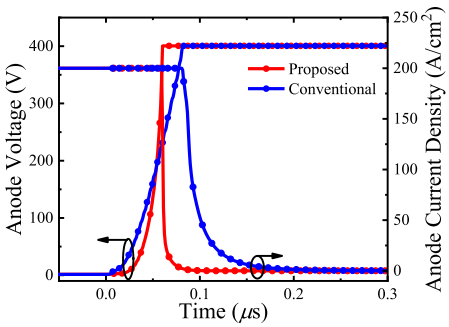

FIGURE 10. Turn-off waveform at J_A= 200 A/cm^2 and V_{bus} = 400 V ($N_{pcol} = 2 \times 10^{16}$ cm^{-3} for the conventional one and $N_{pcol} = 1 \times 10^{15}$ cm^{-3} for the proposed one).

of the proposed one is a little larger than that of the conventional one. This is because the high carrier concentration at the cathode side can be swept out quickly by the high electric field at the voltage rising stage of the turning-off [20]. After that, the proposed one has a smaller tail current at the current falling stage of the turning-off due to the lighter doped P-collector.

IV. CONCLUSION

A novel TSPG-IGBT with self-biased pMOS is proposed and investigated by numerical simulations. TCAD simulation results indicate that the concentration of the N-cs can be improved to 1×10^{18} cm^{-3} without jeopardizing the breakdown voltage, because the potential of the N-cs is clamped by the self-biased pMOS. As a result, a 24% reduction in the saturation current density and a 0.3 V reduction in the on-state voltage are achieved without sacrificing the turn-off loss. Additionally, the SCSOA of the proposed one is 1.75 times larger due to the smaller saturation current density.

REFERENCES

[1] M. Kitagawa, I. Omura, S. Hasegawa, T. Inoue, and A. Nakagawa, "A 4500 V injection enhanced insulated gate bipolar transistor (IEGT) operating in a mode similar to a thyristor," in *Proc. IEEE Int. Elect. Devices Meeting*. Washington, DC, USA, 1993, pp. 679–682, doi: 10.1109/IEDM.1993.347221.

[2] T. Inoue, H. Ninomiya, K. Sugiyama, K. Matsusihta, T. Ogura, and H. Ohashi, "New collector design concept for 4.5 kV injection enhanced gate transistor (IEGT)," in *Proc. IEEE 14th Int. Symp. Power Semicond. Devices ICs (ISPSD)*. Sante Fe, NM, USA, 2002, pp. 49–52, doi: 10.1109/ISPSD.2002.1016168.

[3] K. Oyama *et al.*, "Novel 600-V trench high-conductivity IGBT (Trench HiGT) with short-circuit capability," in *Proc. IEEE 13th Int. Symp. Power Semicond. Devices ICs (ISPSD)*. Osaka, Japan, 2001, pp. 417–420, doi: 10.1109/ISPSD.2001.934642.

[4] H. Takahashi, H. Haruguchi, H. Hagino, and T. Yamada, "Carrier stored trench-gate bipolar transistor (CSTBT)-a novel power device for high voltage application," in *Proc. IEEE 8th Int. Symp. Power Semicond. Devices ICs (ISPSD)*. Maui, HI, USA, 1996, pp. 349–352, doi: 10.1109/ISPSD.1996.509513.

[5] T. Takahashi, Y. Tomomatsu, and K. Sato, "CSTBT (III) as the next generation IGBT," in *Proc. IEEE 20th Int. Symp. Power Semicond. Devices ICs (ISPSD)*. Orlando, FL, USA, 2008, pp. 72–75, doi: 10.1109/ISPSD.2008.4538900.

[6] M. Antoniou, F. Udrea, F. Bauer, and I. Nistor, "The soft Punchthrough+ superjunction insulated gate bipolar transistor: A high speed structure with enhanced electron injection," *IEEE Trans. Electron Devices*, vol. 58, no. 3, pp. 769–775, Mar. 2011, doi: 10.1109/TED.2010.2101076.

[7] M. Antoniou *et al.*, "Novel approach toward plasma enhancement in trench-insulated gate bipolar transistors," *IEEE Electron Device Lett.*, vol. 36, no. 8, pp. 823–825, Aug. 2015, doi: 10.1109/LED.2015.2433894.

[8] O. Spulber *et al.*, "A novel trench clustered insulated gate bipolar transistor (TCIGBT)," *IEEE Electron Device Lett.*, vol. 21, no. 12, pp. 613–615, Dec. 2000, doi: 10.1109/55.887483.

[9] M. Sweet *et al.*, "Clustered insulated gate bipolar transistor: A new power semiconductor device," *IEE Proc. Circuits Devices Syst.*, vol. 148, no. 2, pp. 75–78, Apr. 2001, doi: 10.1049/ip-cds:20010168.

[10] N. Luther-King, M. Sweet, and E. M. S. Narayanan, "Clustered insulated gate bipolar transistor in the super junction concept: The SJ-TCIGBT," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3072–3080, Jun. 2012, doi: 10.1109/TPEL.2011.2162965.

[11] M. T. Rahman *et al.*, "A novel carrier accumulating structure for 1200V IGBTs without negative capacitance and decreasing breakdown-voltage," in *Proc. IEEE 30th Int. Symp. Power Semicond. Devices ICs (ISPSD)*. Chicago, IL, USA, 2018, pp. 491–494, doi: 10.1109/ISPSD.2018.8393710.

[12] M. Huang, B. Gao, Z. Yang, L. Lai, and M. Gong, "A carrier-storage-enhanced superjunction IGBT with ultralow loss and on-state voltage," *IEEE Electron Device Lett.*, vol. 39, no. 2, pp. 264–267, Feb. 2018, doi: 10.1109/LED.2017.2788458.

[13] K.-H. Oh *et al.*, "Experimental investigation of 650V superjunction IGBTs," in *Proc. IEEE 28th Int. Symp. Power Semicond. Devices ICs (ISPSD)*. Prague, Czechia, 2016, pp. 299–302, doi: 10.1109/ISPSD.2016.7520837.

[14] J. Hu, M. Bobde, H. Yilmaz, and A. Bhalla, "Trench shielded planar gate IGBT (TSPG-IGBT) for low loss and robust short-circuit capalibity," in *Proc. IEEE 25th Int. Symp. Power Semicond. Devices ICs (ISPSD)*. Kanazawa, Japan, 2013, pp. 25–28, doi: 10.1109/ISPSD.2013.6694390.

[15] N. Luther-King, M. Sweet, and E. M. S. Narayanan, "Performance of a trench pMOS gated, planar, 1.2 kV Clustered insulated gate bipolar transistor in NPT technology," in *Proc. IEEE 21th Int. Symp. Power Semicond. Devices ICs (ISPSD)*. Barcelona, Spain, 2009, pp. 164–167, doi: 10.1109/ISPSD.2009.5158027.

[16] P. Li, X. Lyu, J. Cheng, and X. Chen, "A low on-state voltage and saturation current TIGBT with self-biased pMOS," *IEEE Electron Device Lett.*, vol. 37, no. 11, pp. 1470–1472, Nov. 2016, doi: 10.1109/LED.2016.2614514.

[17] F. Yang *et al.*, "A novel IGBT structure with floating N-doped buried layer in P-base to suppress latch-up," *IEEE Electron Device Lett.*, vol. 37, no. 9, pp. 1174–1177, Sep. 2016, doi: 10.1109/LED.2016.2593904.

[18] M. Mori *et al.*, "A planar-gate high-conductivity IGBT (HiGT) with hole-barrier layer," *IEEE Trans. Electron Devices*, vol. 54, no. 6, pp. 1515–1520, Jun. 2007, doi: 10.1109/TED.2007.895874.

[19] X. Chen, "Low voltage power supply," U.S. Patent US8 294 215 Oct. 2012.

[20] K. Sheng, F. Udrea, and G. A. J. Amaratunga, "Optimum carrier distribution of the IGBT," *Solid-State Electron.*, vol. 44, no. 9, pp. 1573–1583, 2000, doi: 10.1016/S0038-1101(00)00103-9.