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Schottky Barrier Height Engineering in β -Ga₂O₃ Using SiO₂ Interlayer Dielectric

ARKKA BHATTACHARYYA¹, PRANEETH RANGA¹, MUAD SALEH², SAURAV ROY¹,
MICHAEL A. SCARPULLA^{1,3}, KELVIN G. LYNN^{2,4,5}, AND SRIRAM KRISHNAMOORTHY¹

¹ Department of Electrical and Computer Engineering, University of Utah, Salt Lake City, UT 84112, USA

² Materials Science and Engineering Program, Center for Materials Research, Washington State University, Pullman, WA 99164, USA

³ Department of Materials Science and Engineering, University of Utah, Salt Lake City, Utah 84112, USA

⁴ School of Mechanical and Materials Engineering, Washington State University, Pullman, WA 99164, USA

⁵ Department of Physics, Washington State University, Pullman, WA 99164, USA

CORRESPONDING AUTHOR: A. BHATTACHARYYA (e-mail: a.bhattacharyya@utah.edu)

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ABSTRACT This paper reports on the modulation of Schottky barrier heights (SBH) on three different orientations of β -Ga₂O₃ by insertion of an ultra-thin SiO₂ dielectric interlayer at the metal-semiconductor junction, which can potentially lower the Fermi-level pinning (FLP) effect due to metal-induced gap states (MIGS). Pt and Ni metal-semiconductor (MS) and metal-interlayer-semiconductor (MIS) Schottky barrier diodes were fabricated on bulk n-type doped β -Ga₂O₃ single crystal substrates along the (010), (−201) and (100) orientations and were characterized by room temperature current-voltage (I-V) and capacitance-voltage (C-V) measurements. Pt MIS diodes exhibited 0.53 eV and 0.37 eV increment in SBH along the (010) and (−201) orientations respectively as compared to their respective MS counterparts. The highest SBH of 1.81 eV was achieved on the (010)-oriented MIS SBD using Pt metal. The MIS SBDs on (100)-oriented substrates exhibited a dramatic increment ($>1.5\times$) in SBH as well as reduction in reverse leakage current. The use of thin dielectric interlayers can be an efficient experimental method to modulate SBH of metal/Ga₂O₃ junctions.

INDEX TERMS Gallium oxide, Schottky contact, metal-insulator-semiconductor, Fermi-level pinning, power device.

I. INTRODUCTION

Beta-Ga₂O₃ is a transparent conducting oxide which has emerged as a promising candidate for next generation power electronic devices largely due to its wide band gap ($E_g \sim 4.6 - 4.9$ eV) [1], [2]. With a large projected breakdown field of 6-8 MV/cm, the predicted Baliga Figure of Merit (BFOM) is more than three times greater than the conventional wide band gap semiconductors such as SiC and GaN [3]. The availability of native single crystal substrates made from cost-effective melt-grown techniques and the ability to grow high quality epitaxial films with controllable doping using advanced epitaxial techniques makes it further attractive for high power vertical devices [4]–[9]. However, due to the difficulty with p-type doping and the flat valence band dispersion resulting in very large effective mass for holes, the use of β -Ga₂O₃ is currently restricted to

unipolar power devices such as metal-semiconductor FETs, MOSFETs and rectifying diodes [2], [10], [11]. Schottky contacts with enhanced barrier heights and low reverse leakage currents is crucial for high-power device applications. Therefore, the optimization of metal-semiconductor (MS) Schottky contacts (SCs) on β -Ga₂O₃ is of key importance for reliable functioning of these unipolar devices. It is of particular interest to investigate whether it is possible to obtain large Schottky barrier heights ($\sim E_g/2$) that can potentially then be used to design Enhancement-mode MESFETs.

In the last few years, formation of SCs on β -Ga₂O₃ and their electrical properties were studied and investigated, most of which involved SCs with various high workfunction metals, surface treatments and different metal deposition techniques on different orientations of β -Ga₂O₃ substrates [13]–[30]. The anisotropic material properties

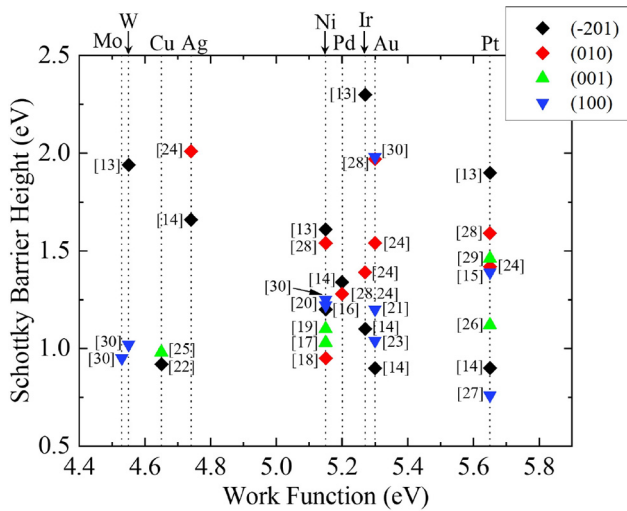


FIGURE 1. Overview of Schottky barrier heights extracted using I-V, C-V and internal photoemission (IPE) measurements on four different orientations of β -Ga₂O₃ using different metals as a function of metal workfunction. The metal workfunction values were considered from reference [12].

of β -Ga₂O₃ due to its highly asymmetric monoclinic crystal structure has also attracted immense research interest [10], [11]. A brief overview of the measured Schottky barrier heights (SBH) of SCs with high work function metals on various orientations of β -Ga₂O₃ is shown in Figure 1. The (010) orientation exhibits lower oxygen-dangling bond density and higher surface band-bending compared to (-201) orientation [31], [32] and is expected to exhibit larger SBH, but Yao *et al.* [13] showed that higher barrier heights can be achieved on (-201) orientation with surface treatments. Farzana *et al.* [28] reported a range of SBH (1.28-1.97eV) using different metals suggesting that the classical Fermi level pinning effect (FLP) may not be the dominant factor for SC formation on (010) β -Ga₂O₃ SBDs, but there are other reports on (010) β -Ga₂O₃ with lower reported barrier heights [18], [24]. Study on (100) and (001) β -Ga₂O₃ is rather sparse and till date very low barrier heights have been reported for (100) β -Ga₂O₃ [15], [17], [19], [20], [23], [25], [26], [30]. Furthermore, it is also observed from Figure 1 that the SBH on β -Ga₂O₃ does not show an universal trend with the metal workfunction indicating that surface/interface states due to defects and crystal orientation, crystal quality and their passivation with different types of surface treatment or metal deposition techniques can play a very important role in determining the effective SBH.

According to the Schottky-Mott rule, the SBH achieved at a SC is the difference between the metal work function and the semiconductor electron affinity. However, the Schottky-Mott rule is rarely observed. The effective barrier height that is established at a metal-semiconductor interface is actually governed by a combination of various factors such as metal workfunction difference, interface states and the effect of image force lowering [23]. The interface states

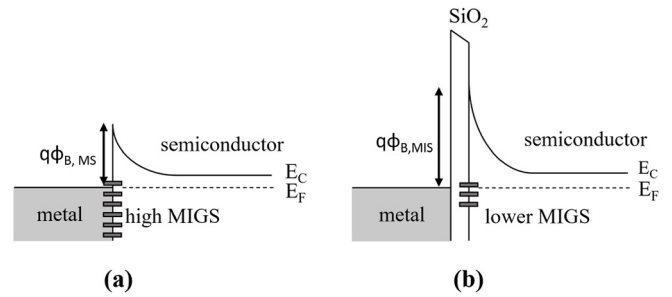


FIGURE 2. Schematic of energy band diagram of (a) MS and (b) MIS Schottky junctions showing the lowering of MGS with the insertion of SiO₂ interfacial layer and a possible enhancement of Schottky barrier height.

at a metal-semiconductor junction are mostly mid-gap states that originate from the metal wave functions decaying into the semiconductor band gap and are called metal-induced gap states (MIGS) [33]. The other contribution to the interface states come from the reconstruction of the dangling bonds, defects and localized impurities at the metal-semiconductor interface [34]. Depending on the density of these interface states, the Fermi level gets pinned near one of the band edges and thus play a very important role in determining the effective barrier height that can be measured. The weak dependence of SBH on the metal workfunction has also been observed and studied in other semiconductor materials like Ge, Si, and InGaAs and is attributed to FLP caused by metal-induced gap states or defects at the metal-semiconductor interface [34]–[38]. Many groups in the past have reported that the introduction of a thin interfacial dielectric layer, both in-situ and ex-situ, can act as a blocking layer to prevent the spilling of metal electron waves and thus can potentially lower the FLP effect due to MIGS [35]–[38] (Fig. 2(b)). This provides a simple and elegant solution to engineer the effective barrier height by reducing the contribution from MIGS. In this work, we investigate the modulation of Schottky barrier height on different orientations of β -Ga₂O₃ single crystal substrates with the insertion of ultra-thin SiO₂ dielectric layer at the metal-semiconductor interface.

II. DEVICE FABRICATION AND CHARACTERIZATION

The 5 mm × 5 mm × 0.6 mm edge-defined film-fed grown (EFG) Sn-doped (010) and (-201) β -Ga₂O₃ substrates were acquired from Novel Crystal Tech (Japan). The Zr-doped (100) β -Ga₂O₃ single crystal bulk substrates were grown by vertical gradient freeze (VGF) method and the details are available in reference [39]. The (100)-oriented samples were prepared by sawing first and then cleaving along the cleavage plane (100) into samples of 3.5 × 4.5 × 0.6 mm³ dimensions and the substrate orientation was confirmed by XRD measurements and reported elsewhere [39]. On (010) oriented substrates, the electron concentration and mobility from Hall measurements were measured to be 1.1 × 10¹⁸ cm⁻³ and 89 cm²/Vs, respectively. For the (-201) oriented substrates, the electron concentration and mobility values measured

were $1.7 \times 10^{18} \text{ cm}^{-3}$ and $32 \text{ cm}^2/\text{Vs}$, respectively. From Hall effect measurements, the room temperature net electron concentration and mobility were measured to be $1.2 \times 10^{18} \text{ cm}^{-3}$ and $78 \text{ cm}^2/\text{Vs}$, respectively in the (100)-oriented samples. It should be noted that the electron concentration is similar for the samples along all the three orientations considered here for this study. The electron concentrations and doping profile were also further confirmed using capacitance-voltage measurements as discussed later in the paper.

Six substrates, two of each orientation, were first cleaned using conventional solvents (acetone, IPA and DI water) followed by dip in Piranha solution (98% H₂SO₄: 32% H₂O₂ 4:1) for 5 mins. Three substrates, one of each orientation, were processed as MS diodes and the rest three substrates, one of each orientation, were processed as metal-interlayer (SiO₂)-semiconductor (MIS) diodes. Series resistance effect was dominant in the capacitance voltage measurements on the (010) and (-201) SBDs necessitating formation of quasi-lateral diodes with concentric Ohmic-Schottky design with 5-30 μm spacing between the Ohmic and Schottky pads. For the (010) oriented substrate, first an extra step of heavily-doped Ga₂O₃ (100 nm thick, $N_D(\text{Si}) \sim 1 \times 10^{20} \text{ cm}^{-3}$) was selectively grown in the ohmic contact regions by Agnitron Agilis MOCVD system using 500 nm thick SiO₂ (PECVD) masks to realize good ohmic contacts. Then Ti/Au (50 nm/50 nm) was sputtered in the Ohmic contact regions defined by photolithography and lift-off process followed by rapid thermal annealing at 450°C in nitrogen for 1.5 minutes. On the (-201) oriented substrates, first Ti/Au (50 nm/50 nm) Ohmic contacts were sputter deposited and patterned using photolithography and lift-off process and no further processing was needed to realize good ohmic contacts. Following this, SiO₂ dielectric was deposited by ALD (discussed in the next paragraph) on the (010) and (-201) MIS samples and the oxide in the contact region was etched using a quick dip (10 seconds) in diluted HF solution after patterning by standard optical lithography. Next, 150 μm and 200 μm diameter circular Pt/Au (50 nm/50 nm) and Ni/Au (50 nm/50 nm) Schottky contacts were sputtered and e-beam evaporated respectively on the MS and MIS samples (both (010) and (-201)) after re-aligning to the ohmic contacts using standard photolithography. For the (100) oriented samples, SiO₂ dielectric was first deposited by ALD on the front side of MIS sample and then Ti/Au (50nm/50nm) ohmic contacts were sputtered on the backside of the sample. Then 150 μm and 200 μm diameter Pt/Au (50nm/50nm) and Ni/Au (50nm/50nm) Schottky contacts were sputter deposited and e-beam evaporated respectively on both MS and MIS samples. The MIS diodes on all three substrates were not subjected to any high temperature process after the ALD dielectric deposition. The processed MIS diode schematics are shown in Figure 3. The current-voltage (I-V) characteristics and capacitance-voltage (C-V) measurements (1 MHz) were performed in air at room temperature ($\sim 298\text{K}$) using a Keithley 4200A-SCS parameter analyzer.

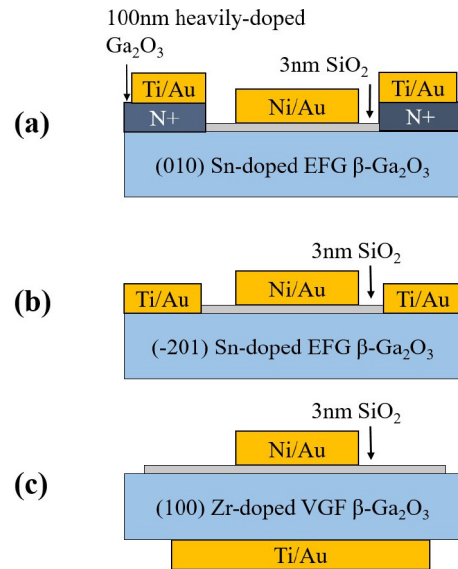


FIGURE 3. Schematic of MIS diode structures on (a) (010), (b) (-201), and (100) oriented β -Ga₂O₃ substrates with 3 nm SiO₂ interlayer using Ni Schottky metal (Pt MIS diodes had identical structures with Pt as anode instead of Ni). The respective MS diodes are similar in structure just without the SiO₂ dielectric interlayer.

Before loading the MIS samples into the ALD chamber, they were first solvent cleaned (acetone, IPA and DI water) followed by dip in Piranha solution (98% H₂SO₄: 32% H₂O₂ 4:1) for 5 mins. Before the start of the ALD deposition cycle, the substrates were treated with remote oxygen plasma (300W and 20 sccm O₂ flow) for 5 minutes. A 3nm thin SiO₂ layer was deposited on the three substrates for MIS processing at 200°C using a Cambridge Fiji F200 ALD tool using tris(dimethylamino)silane (3DMAS) precursor and O₂ plasma source. The oxide thickness was confirmed by performing optical ellipsometry on a monitor Si wafer using a Woollam V-VASE spectroscopic ellipsometer tool. The measured thickness of SiO₂ layer was 3.5 nm on the Si wafer and the SiO₂ formed on the Si wafer due to the remote plasma treatment was measured to be 4-5 Å. SiO₂ thickness on Ga₂O₃ is hence estimated to be 3 nm, and this is used as the interlayer thickness for further analysis.

III. RESULTS AND DISCUSSIONS

The current density-voltage (J-V) characteristics of all the representative Schottky diodes at RT are shown in Figure 4. Both the metal-semiconductor (MS) and metal-interlayer-semiconductor (MIS) Schottky diodes exhibited highly rectifying behavior with > 8 orders of magnitude of rectification at $\pm 2\text{V}$ along the (010) and (-201) orientations (Fig. 4 (a), (b)). The MS diodes on (100) substrates (Fig. 4(c)) were found to be less rectifying. The MIS SBDs showed an increased forward voltage compared to the MS diodes, along all the orientations as expected, indicating that the SBH of MIS diodes might be higher than their respective bare metal MS counterparts, in addition to the blocking of

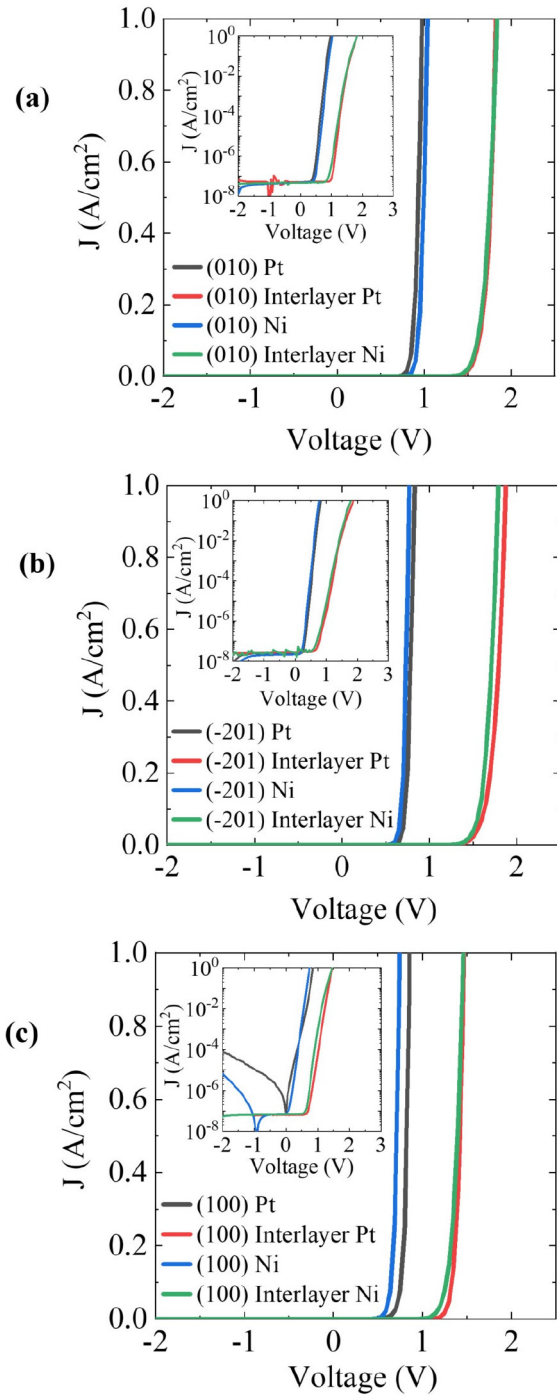


FIGURE 4. Linear J-V characteristics (200 μm diameter pad size) of the Pt and Ni MS and MIS SBDs on (a) (010), (b) (-201) and (c) (100)-oriented β -Ga₂O₃ showing the increase in forward voltages with the insertion of ultra-thin SiO₂ and the insets showing their corresponding log J-V characteristics.

current due to the band offset at the SiO₂/Ga₂O₃ interface with the insertion of an insulator [40].

For moderately-doped semiconductors, generally, thermionic emission (TE) is the dominant transport mechanism in ideal MS diodes [41]. The J-V characteristics of the MS SBDs and MIS SBDs were analyzed using the TE

model which can be expressed as

$$J = A^{**}T^2 e^{-\frac{q\Phi_B^{\text{eff}}}{kT}} \left(e^{\frac{qV}{nkT}} - 1 \right) \quad (1)$$

where,

$$J_0 = A^{**}T^2 e^{-\frac{q\Phi_B^{\text{eff}}}{kT}} \quad (2)$$

where A^{**} is the effective Richardson constant, with a calculated theoretical value of 41.1 A cm⁻²K⁻² (for electron effective mass of $m_e^* = 0.34m_0$) [10], q is the elementary charge, k is the Boltzmann constant, V is applied bias voltage, n is the ideality factor, Φ_B^{eff} is the effective barrier height, J_0 is the reverse saturation current density, and T is the absolute temperature. The effective barrier height is then calculated as,

$$q\Phi_B^{\text{eff}} = kT \ln \left(\frac{A^{**}T^2}{J_0} \right) \quad (3)$$

and the ideality factor, n , is defined as,

$$n = \frac{q}{2.3kT \left(\frac{d \log(J)}{dV} \right)} \quad (4)$$

The barrier heights and ideality factors extracted from the J-V characteristics are summarized in Table 1. The barrier heights for the MS SBDs were in the range 0.72 eV to 1.27 eV with lowest value for Ni on (100) substrate and the highest for Pt on (010) substrate. The extracted SBH values are comparable to most reports in the literature (Figure 1). The MS Pt and Ni diodes on the (100) oriented substrate exhibited lower barrier heights with higher values of n than the other two orientations which indicates higher degree of contribution from non-thermionic transport mechanisms. This effect has been observed in other reports on floating zone (FZ), Czochralski (CZ) and EFG grown (100) β -Ga₂O₃ bulk crystals [21], [23], [42]. For the MIS SBDs, the extracted SBH were in a range of 1.21 eV to 1.56 eV with Ni on (-201) being the lowest and Pt on (010) being the highest. Although, this may indicate an improvement in barrier heights with the insertion of an SiO₂ interlayer, but still these values are an underestimation as we will see in subsequent discussions. TE model can underestimate the barrier heights for non-ideal diodes ($n > 1$) due to barrier height inhomogeneities at the MS junction [41], [43].

The MIS SBDs on all the orientations exhibited comparatively higher n values which is expected and also has been observed in previously published reports in other semiconductor systems [44], [45]. The presence of an intentional or unintentional interfacial layer could result in tunneling of electrons through the insulator and enhanced surface band bending at the dielectric-semiconductor interface. Solving the metal-oxide semiconductor electrostatics taking into account the voltage drop across the thin oxide and also the interface trap charge, the ideality factor for non-ideal MIS Schottky diodes on n-type semiconductor can be modeled as a function

TABLE 1. Summary of extracted SBH from J-V characteristics for all MS and MIS SBDs using TE model.

Substrate	Metal	$q\Phi_{B,MS}^{IV}$ (eV)	n_{MS}	$q\Phi_{B,MIS}^{IV}$ (eV)	n_{MIS}	$\Delta q\Phi_B^{IV}$ (eV)
(010)	Pt	1.18 ± 0.06	1.15 ± 0.08	1.56 ± 0.08	1.36 ± 0.1	0.38 ± 0.14
	Ni	1.27 ± 0.04	1.16 ± 0.05	1.38 ± 0.06	1.61 ± 0.1	0.11 ± 0.1
(-201)	Pt	1.08 ± 0.08	1.13 ± 0.2	1.30 ± 0.05	1.37 ± 0.1	0.22 ± 0.13
	Ni	1.04 ± 0.04	1.15 ± 0.08	1.21 ± 0.07	1.91 ± 0.2	0.17 ± 0.1
(100)	Pt	0.84 ± 0.03	1.56 ± 0.07	1.22 ± 0.04	1.66 ± 0.08	0.38 ± 0.07
	Ni	0.72 ± 0.02	1.51 ± 0.04	1.24 ± 0.03	1.41 ± 0.05	0.52 ± 0.05

$q\Phi_{B,MS}^{IV}$, $q\Phi_{B,MIS}^{IV}$ = Schottky barrier heights (eV) and n_{MS} , n_{MIS} = ideality factors of MS and MIS diodes respectively from J-V characteristics. $\Delta q\Phi_B^{IV} = q\Phi_{B,MIS}^{IV} - q\Phi_{B,MS}^{IV}$ (eV).

of interface density of trap states, D_{it} and also the interfacial layer thickness as done by Card and Rhoderick [44],

$$n = 1 + \frac{\delta}{\epsilon_{ox}} \left(\frac{\epsilon_s}{W} + qD_{it} \right) \quad (5)$$

where, n is the ideality factor extracted from the TE model, δ is the interlayer oxide thickness, ϵ_{ox} is the permittivity of the oxide, ϵ_s is the semiconductor permittivity, W is the depletion depth inside the semiconductor, q is the elementary charge and D_{it} is the interface state density. This model, although, not very accurate when the interface state densities are very high, it can be very effective for estimation of mean D_{it} value, especially for ultra-thin oxides when conventional C-V measurement techniques, such as high-low method, quasi-static measurements become unviable because of very high dissipation losses even at very low forward bias while the device is moved from depletion to accumulation. The dual sweep I-V characteristics (-3V to 3V to -3V) of the MIS SBDs show very low hysteresis for the (100), (010) and (-201)-oriented substrates indicating minimal charge trapping at the semiconductor-dielectric interface. However, the (-201) MIS SBDs exhibited comparably a little higher hysteresis than other two orientations which can be attributed to the presence of higher D_{it} as previously reported [46]. Nevertheless, all the MIS diodes exhibited low hysteresis ($\Delta V < 0.15V$) indicating good quality interfaces for the MIS SBDs. Hence, we use the measured value of n to estimate D_{it} in the MIS diodes.

SBH values extracted from J-V characteristics in general, can underestimate the barrier height because of the barrier height inhomogeneity and current conduction through localized low SBH regions. We performed C-V measurements on both the MS and MIS diodes along the (010), (100) and (-201) orientations. First, we assume that the voltage drop across thin dielectric SiO₂ interfacial layer to be negligible. For a Schottky-diode under bias, the C-V relationship can

be expressed as [41],

$$C = \frac{A\epsilon_s}{W} = A \sqrt{\frac{q\epsilon_s N_D}{2(V_{bi} - V - \frac{kT}{q})}} \quad (6)$$

and

$$\frac{A^2}{C^2} = \frac{2(V_{bi} - V - \frac{kT}{q})}{q\epsilon_s N_D} \quad (7)$$

where, ϵ_s is the semiconductor permittivity (for β -Ga₂O₃, $\epsilon_s = 10\epsilon_o$ [10], where ϵ_o = permittivity of free space), V_{bi} is the built-in potential, N_D is the doping concentration in the semiconductor, A is the area of the anode and W is the semiconductor depletion width. V_{bi} and N_D can be extracted from the V-axis intercept and the slope of $(A/C)^2$ -V plots respectively. Figure 5 shows the room temperature C-V (inset) and $(A/C)^2$ -V plots of all the SBDs measured at 1MHz. Any variations in the $(A/C)^2$ -V slopes can be attributed to slight fluctuation in the doping for various Ga₂O₃ substrates used in this work. However, the doping profiles were flat (Figure 5(d)) for all the three orientations and the net electron concentrations were similar ($\sim 1 \times 10^{18} \text{ cm}^{-3}$) and matched with the Hall measurements. The barrier height is then extracted using the expression,

$$q\Phi_B = qV_{bi} + qV_n + kT \quad (8)$$

$$qV_n = E_C - E_F = kT \ln \left(\frac{N_C}{N_D} \right) \quad (9)$$

where, E_C is the conduction band minima, E_F is the Fermi level and N_C is the effective density of states in the conduction band which is calculated to be $4.97 \times 10^{18} \text{ cm}^{-3}$ for an electron effective mass of $0.34m_o$ for β -Ga₂O₃ [10].

Although, the equation (7) in the C-V method can be a very accurate technique for Schottky barrier height extraction for metal-semiconductor SBDs, it is not appropriate for MIS SBDs [44], [45]. This is because it overestimates the V_{bi}

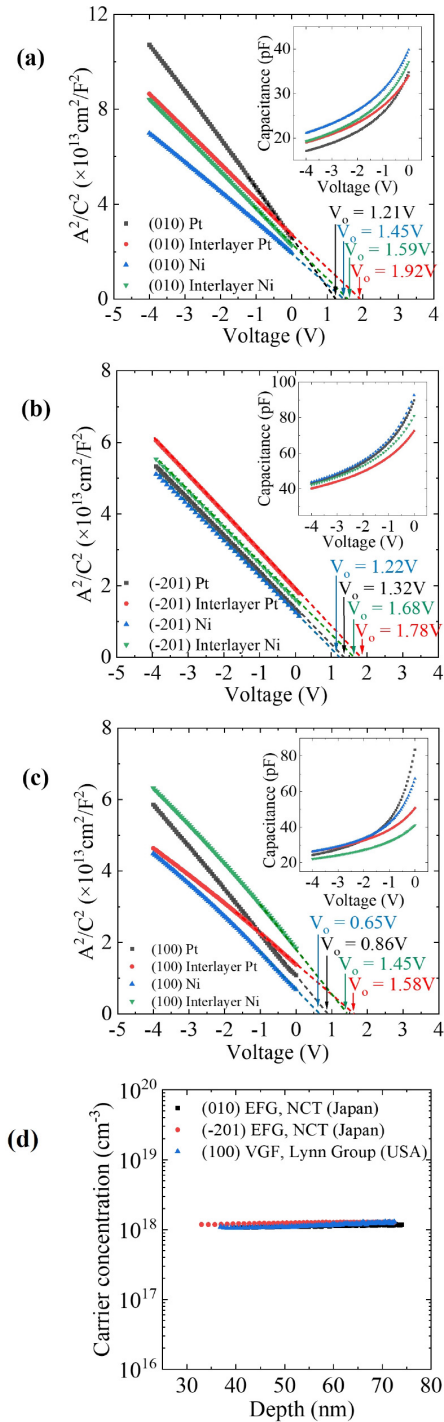


FIGURE 5. $(A/C)^2$ - V characteristics of the Pt and Ni MS and MIS SBDs on (a) (010), (b) (-201) and (c) (100) - oriented β -Ga₂O₃ showing the increment in intercept voltages with the insertion of ultra-thin SiO₂ and the insets showing their corresponding C-V characteristics. (d) Net carrier concentration vs depth profile obtained from C-V measurements of representative devices along three orientations of β -Ga₂O₃ substrates used in this work. ((010) EFG : $1.02 \pm 0.3 \times 10^{18} \text{ cm}^{-3}$, (-201) EFG : $1.6 \pm 0.1 \times 10^{18} \text{ cm}^{-3}$, (100) VGF : $1.4 \pm 0.2 \times 10^{18} \text{ cm}^{-3}$).

values for MIS structures even with very thin SiO₂ layers because the dielectric constant of SiO₂ is very low ($\epsilon_{ox} = 3.9\epsilon_0$) and so the voltage drop across the oxide cannot be

considered negligible as assumed earlier. The effect of the presence of an interfacial layer on the V_{bi} extraction from $(A/C)^2$ - V plots was well studied in the past which shows that the oxide layer voltage drop and interface trap charges if not accounted for can lead to higher extracted values for V_{bi} [44], [45]. Assuming the occupancy of the interface trap charges is completely governed by the semiconductor Fermi level and as the variation of interface trap state density is not too dramatic (of the same order) within the semiconductor band gap, the capacitance-voltage relationship for a reversed biased n-type MIS SBD as modeled by Cowley [45] can be expressed as,

$$\frac{A^2}{C^2} = \frac{2(1 + \alpha)}{q\epsilon_s N_D} \left[(1 + \alpha) \left(V_{bi} - \frac{kT}{q} \right) + \sqrt{V_1 \left(V_{bi} - \frac{kT}{q} \right)} + V + \frac{V_1}{4(1 + \alpha)} \right] \quad (10)$$

and, $\alpha = qD_{it} \frac{\delta}{\epsilon_{ox}}$ and $V_1 = 2q\epsilon_s N_D \frac{\delta^2}{\epsilon_{ox}^2}$ where, δ is the interfacial oxide layer thickness ($\sim 3\text{nm}$ SiO₂) and D_{it} is a mean interface trap state density estimated using equation (5). The V-axis intercept voltage, V_o from the linear $(A/C)^2$ - V plots is given by,

$$V_o = (1 + \alpha)V_{bi} + \sqrt{V_1 V_{bi}} + \frac{V_1}{4(1 + \alpha)} \quad (11)$$

The small correction of kT that arise due to mobile carriers near the depletion region edge [45] was added to the barrier height calculation like in equation (8). It can be considered that V_{bi} extracted from V-axis intercept of the $(A/C)^2$ - V plot using equation (11) to be the true V_{bi} for all the MIS devices. Table 2 summarizes the MIS diode barrier heights extracted using both the general C-V method ($q\Phi_{B,MIS}^{CV}$) and C-V method with correction proposed by Cowley ($q\Phi_{B,MIS}^{CV,\delta}$). It can be seen that the general C-V method applied to MIS diodes overestimated the V_{bi} and hence the SBH values for all the devices on three orientations by ~ 0.1 - 0.2 V. Therefore, for MIS SBDs, only the SBH values extracted using equation (11) were considered for further analysis.

The MS SBDs were analyzed using the general C-V method and the measured SBH ($q\Phi_{B,MS}^{CV}$) values were in the range of 0.71 eV - 1.5 eV, a bit higher than those from I-V measurements, as expected. For the MS SBDs, the highest measured barrier height (1.5 eV) was on the (010)-oriented substrate using Ni as the Schottky metal. On the (-201) and (100)-oriented substrates, the MS Pt SBDs showed higher measured barrier heights than the Ni SBDs. The (100)-oriented MS SBDs exhibited the lowest barrier heights compared to all other orientations (Pt: 0.92 eV, Ni: 0.71 eV). (100)-oriented β -Ga₂O₃ has consistently exhibited lower barrier heights in literature than the other two orientations (Figure 1).

For the MIS SBDs, all the Pt MIS SBDs exhibited higher barrier heights than Ni for their respective orientations. The highest barrier achieved is 1.81eV for the Pt MIS SBDs

TABLE 2. Summary of extracted SBH from C-V characteristics for all MS and MIS SBDs.

Substrate	Metal	$q\Phi_{B,MS}^{CV}$ (eV)	$q\Phi_{B,MIS}^{CV}$ (eV)	$q\Phi_{B,MIS}^{CV,\delta}$ (eV)	$\Delta q\Phi_B^{CV}$ (eV)
(010)	Pt	1.28 ± 0.04	1.97 ± 0.05	1.81 ± 0.05	0.53 ± 0.09
	Ni	1.50 ± 0.03	1.64 ± 0.02	1.54 ± 0.02	0.04 ± 0.05
(-201)	Pt	1.38 ± 0.08	1.84 ± 0.03	1.75 ± 0.03	0.37 ± 0.11
	Ni	1.26 ± 0.05	1.74 ± 0.06	1.28 ± 0.06	0.02 ± 0.11
(100)	Pt	0.92 ± 0.02	1.63 ± 0.03	1.44 ± 0.03	0.52 ± 0.04
	Ni	0.71 ± 0.02	1.51 ± 0.02	1.32 ± 0.02	0.61 ± 0.05

$q\Phi_{B,MS}^{CV}$, $q\Phi_{B,MIS}^{CV}$ = Schottky barrier heights (eV) of MS and MIS diodes respectively from C-V characteristics using general C-V method. $q\Phi_{B,MIS}^{CV,\delta}$ = Schottky barrier heights of MIS diodes from C-V method by Cowley. $\Delta q\Phi_B^{CV} = q\Phi_{B,MIS}^{CV,\delta} - q\Phi_{B,MS}^{CV}$ (eV).

on (010) substrate. Although Pt MIS SBDs on (010) and (-201)-oriented substrates exhibited considerable increment in SBH (0.53 eV and 0.37 eV respectively), but the Ni SBDs exhibited a bit lower increment in SBH (0.04 eV and 0.02 eV respectively). One possible reason could be that either the FLP effect due to MIGS were already low on Ni SBDs or the metal electron wave functions could still be penetrating into the semiconductor bandgap through the thin SiO₂ interfacial layer. MIGS penetration through a high bandgap dielectric layer is highly unlikely [37], indicating that FLP effect was indeed lower to begin with in the case of Ni diodes. The Pt and Ni MIS SBDs exhibited large improvement in the SBHs on the (100) oriented substrates with an increment of 0.52eV and 0.61eV respectively (Pt: 1.44 eV, Ni: 1.32 eV). This is because of the decoupling of the Fermi level in the semiconductor and the metal due to the insertion of an inter-layer dielectric. Surface-pretreatment or metal deposition in oxygen-rich conditions to reduce oxygen vacancies at the surface has been previously reported to result in some of the highest barrier heights on β -Ga₂O₃ [13], [24]. Apart from FLP due to MIGS penetration, oxygen vacancy defect sites at the surface of β -Ga₂O₃ has also been predicted to pin the Fermi-level at specific energy levels (1.3 eV, 1.6 eV and 2.2 eV) below the conduction band edge [14]. Gao *et al.* experimentally demonstrated that remote oxygen-plasma treatment of β -Ga₂O₃ surface can lead to diffusion of activated oxygen atoms into the lattice from the surface and thus, reduce oxygen-vacancy related defects [47]. Therefore, we hypothesize that inserting a high bandgap interfacial dielectric layer (SiO₂) blocks MIGS penetration and remote oxygen plasma pretreatment prior to dielectric deposition could passivate oxygen vacancies at the interface which can result in enhanced Schottky barrier heights in β -Ga₂O₃.

IV. CONCLUSION

In this work, we demonstrate the enhancement of Schottky barrier heights on three orientations of β -Ga₂O₃ substrates

by insertion of ultra-thin SiO₂ interfacial layer at the MS junction. Pt and Ni MS and MIS SBDs were fabricated on three different orientations ((010), (-201) and (100)) of β -Ga₂O₃ to investigate and compare orientation dependence on barrier height modulation and these devices were characterized by room temperature I-V and C-V measurements. Pt MIS SBDs showed on average an increment of 0.37 - 0.53 eV compared to their MS counterparts. (100)-oriented β -Ga₂O₃, in general, has lower barrier heights than the other two orientations. (100)-oriented MIS SBDs showed dramatic enhancement of barrier heights (1.5× - 1.8×) and reduction of reverse leakage current on this orientation due to significant enhancement of SBH with the interlayer dielectric. A promising application of this technique can be the realization of Enhancement-mode MESFETs with low gate leakage.

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