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NCFET-Based 6-T SRAM: Yield Estimation Based on Variation-Aware Sensitivity

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ABSTRACT The key feature of NCFET (negative capacitance field effect transistor) is its sub-threshold slope (SS) < 60 mV/decade at 300 K. In this work, the n-type NCFET (i.e., pull-down (PD) and pass-gate (PG) transistor in six-transistor (6T) SRAM bit-cell) has SS of 53.92 mV/decade, and the p-type NCFET (i.e., pull-up (PU) transistor in the 6T SRAM bit-cell) has SS of 58.96 mV/decade. In the NCFET-based SRAM cell (vs. conventional SRAM cell with conventional planar bulk MOSFETs), its read (hold)-stability and write-ability are evaluated by the metric of read static noise margin (SNM) and write-ability current (I_w), respectively. Then, under process-induced random variation, sensitivities of SNM and I_w are extracted. Finally, the yield of NCFET-based SRAM array (vs. conventional SRAM array) is quantitatively estimated using the cell-sigma.

INDEX TERMS Yield estimation, sensitivity, cell sigma, SRAM, NCFET.

I. INTRODUCTION

The cache memory (static random access memory, or SRAM) in digital computer has been playing a key role of processing/fetching data in-between central processing unit (CPU) and main memory (DRAM). Although several SRAM configurations such as 4-T, 8-T SRAM cell have been proposed and studied, the six-transistor (6-T) SRAM has been the de-facto front-runner in terms of memory performance for limited bit-cell area. Fig. 1 shows the circuit scheme of 6-T SRAM bit-cell. Because of two cross-coupled inverters in the cell, the storage node (i.e., CH and CL nodes) is symmetric to each other. As long as the cell power supply voltage (V_{DD}) is maintained, the data stored in the cell cannot be lost. Herein, lowering/minimizing V_{DD} would be one of the keys to save the power consumption in SRAM array.

Negative capacitance field effect transistor (NCFET) is one of the promising devices for lower power applications. The use of a material with ferroelectric characteristic results in negative capacitance effect, resulting in internal voltage amplification that can overcome the Boltzmann limit (i.e., the best SS is 60 mV/decade at 300 K). In fact, by simply inserting CMOS-compatible ferroelectric material (e.g., HZO, HAlO) in the gate stack, sub-60 mV/decade SS can be implemented in NCFET at 300 K due to the boosted-up surface potential by negative capacitance effect [1], [2], [3].

To reduce the power consumption in SRAM array, many attempts for NCFET-based SRAM bit-cell have been done. Previous studies [4], [5] have claimed that the read/write performance of NCFET-based SRAM (vs. conventional SRAM) can be improved. However, there is no discussion on the yield estimation of NCFET-based SRAM. In this work, by introducing the cell sigma concept [6], the yield of NCFET-based SRAM (vs. conventional SRAM) is quantitatively estimated (Note that the read and write metric used for read and write yield were selected as RSNM and I_w, respectively). The yield estimation method is based on variation-aware sensitivity. The sensitivities of SNM and I_w to width, length, and threshold voltage can be compared and analyzed. Also, with the quantitative analysis of SRAM yield, the minimum operating voltage (V_{DD}) for a given yield requirement can be projected.

II. NCFET-BASED SRAM

A. NEGATIVE CAPACITANCE FET IN 6-T SRAM BIT-CELL

NCFET (a.k.a., ferroelectric-gated FET; FeFET) with MFIS (Metal-ferroelectric-insulator-semiconductor) gate

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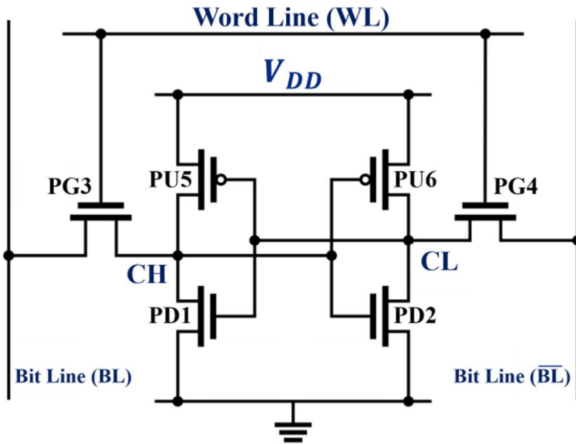

FIGURE 1. The circuit schematic of 6-T SRAM bit-cell. PU and PD transistors make up cross-coupled inverters. The write operation is performed between PG and PU, and the read operation is performed between PG and PD.

stack structure are known to be designed for higher drive current (I_{on}) and steep sub-threshold slope [7]. In this study, the hysteresis-free NCFETs with MFIS gate stack are simulated using 3D Sentaurus technology computer-aided design (TCAD) and MATLAB tools. The ferroelectric material used for the simulation is 2 nm-thick Al:HfO_2, i.e., an HfO_2 based ferroelectric material that is known to be compatible to CMOS process [8]. The insulator (i.e., 'I' of MFIS) located under the ferroelectric layer is 0.9 nm-thick HfO_2. The electrical characteristics of the NCFET device is simulated by using the Landau-Khalatnikov (LK) model, in accordance with the method given in [9], [10]. From the LK equation of [1], [10], the voltage drop across the ferroelectric layer (V_{fe}) can be written as

$$V_{fe} = V_G - \psi_s \approx \alpha_0 Q + \beta_0 Q^3, \quad (1)$$

where indicating V_G as gate voltage, ψ_s as surface potential, and Q as charge on the capacitor per unit area. Coefficients of a_0 and b_0 are defined as $a_0 = 2\alpha T_{fe}$ and $b_0 = 4\beta T_{fe}$, respectively (note that T_{fe} indicates the thickness of ferroelectric layer) [11]. The parameters of ferroelectric material (i.e., Al:HfO_2) are as follows: remnant polarization (P_r) of 5 $\mu C/cm^2$, coercive field (E_c) of 1.15 MV/cm, $\alpha = -3\times10^9$ m/F, and $\beta = 6 \times 10^{11}$ m^5/C^2F [12]. Because internal voltage (V_{int}) can be calculated as the voltage difference between V_G and V_{fe}, the I_{ds} value of NCFET can be numerically simulated from the baseline MOSFET [11].

Since SS generally degrades (i.e., the value of SS increases) with increasing temperature, it can be forecasted that SS will increase at temperatures above 300 K [13], [14]. In [15] (which fabricated the MFIS structured hysteresis-free NCFET using Al:HfO_2), the body factor (m) was extracted from measured SS of NCFET: m = 0.96. Note that m = 1 when a device is governed by the Boltzmann limit. Based on this body factor, SS of the simulated NCFET is 69 mV/decade for n-type device and 76 mV/decade for p-type device at 400 K. Therefore, as the temperature increases, the performance of SRAM should be degraded. The plot of SS-vs.-temperature for n-type/p-type device is drawn in Fig. 3(d).

TABLE 1. Device performance parameters for V_{DD} = 1.0 V.

	NCFET		Baseline	
	N-type	P-type	N-type	P-type
I_{on} [mA/μm]	1.61	0.94	1.40	0.81
I_{off} [nA/μm]	8.40×10^{-3}	7.67×10^{-3}	0.28	0.26
on/off ratio	1.91×10^8	1.22×10^8	5.00×10^6	3.18×10^6
V_{Tsat} / V_{Tlin} [V]	0.31 / 0.34	0.33 / 0.37	0.31 / 0.34	0.33 / 0.37
SS [mV/decade]	53.92	58.96	73.24	79.58

With the simulated hysteresis-free NCFETs, NCFET-based 6-T SRAM bit-cell is designed; the n-type NCFET used for PD and PG transistor has the channel width of 0.1 μm and 0.05 μm, respectively. And, the p-type NCFET used for PU transistor has the channel width of 0.04 μm. Note that all the six transistors in a SRAM bit-cell have the identical channel length of 0.02 μm. The electrical characteristics of those NCFETs in 6-T SRAM cell are shown and summarized in Fig. 2, Fig. 3, and Table 1. Compared against the baseline MOSFET, the NCFET has SS < 60 mV/decade at 300K as well as higher on-state drive current (I_{on}) and lower off-state leakage current (I_{off}) [see Fig. 2(a)]. SS_{avg} was calculated as the voltage required to increase the drain current by 10 times. The voltage range for SS_{avg} is from $I_{DS} = I_{off}$ at V_{GS} = 0 V to I_{DS} = 5 μA/μm at $V_{GS} = V_T$ (threshold voltage). From output characteristics shown in Fig. 2(b) and (c), drain-source on-state resistance (R_{ds}) is derived and shown in Fig. 3(a) and (b). It can be seen that the NCFET shows smaller R_{ds} than baseline MOSFET. The smaller R_{ds} is, the less the power loss of the device is [16]. Figure 3(c) shows transconductance (g_m) derived from I_{DS}-V_{GS} of Fig. 2(a). The larger g_m value of NCFET is associated with its steep-slope characteristics.

B. EVALUATION OF READ-STABILITY & WRITE-ABILITY

Read stability is evaluated by read static noise margin (SNM). The SNM is defined as the minimum voltage that can flip-flop the originally-stored node voltage in SRAM cell. This can be derived from the voltage transfer characteristic (VTC) of inverter during read operation [17], [18]. The voltage of internal node CH (V_{CH}) satisfies the Eq. (2) below

$$\begin{aligned} &I_{D1}(V_{GS} = V_{CL}, V_{DS} = V_{CH}) \\ &\quad = I_{D3}(V_{GS} = V_{WL} - V_{CH}, V_{DS} = V_{BL} - V_{CH}) \\ &\qquad + I_{D5}(V_{GS} = V_{CL} - V_{DD}, V_{DS} = V_{CH} - V_{DD}), \quad (2) \end{aligned}$$

and complementary node CL (V_{CL}) is symmetrical to V_{CH}.

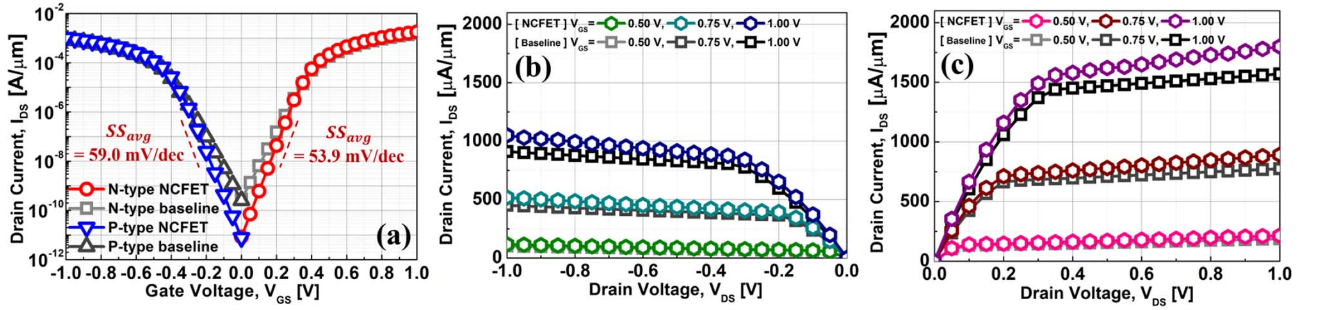

FIGURE 2. (a) I_{DS}-V_{GS} of NCFET and baseline MOSFET. NCFET (vs. baseline MOSFET) has steeper SS (n-type: 53.9 mV/decade, p-type: 59.0mV/decade), higher I_{ON}, and lower I_{OFF}. Note that V_{DS} = 1.0 V. I_{DS}-V_{DS} of NCFET and baseline MOSFET (b) for p-type and (c) for n-type. Because threshold voltages of the devices are designed to be matched, the DIBL of NCFET and baseline MOSFET is identical (i.e., DIBL = 33 mV/V).

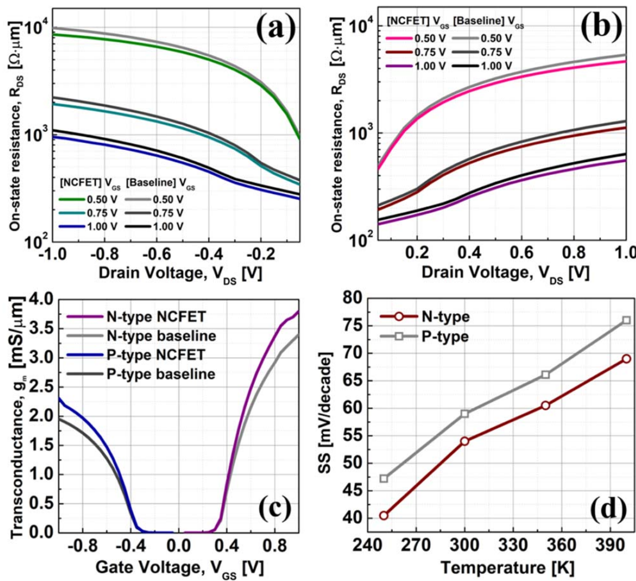

FIGURE 3. Drain-to-source on-state resistance (R_{DS}) of (a) p-type and (b) n-type is estimated at V_{GS} = 0.50 V, 0.75 V, and 1.00 V. (c) The estimated transconductance (g_m) at V_{DS} = 1.0 V. (d) Temperature vs. subthreshold slope (SS).

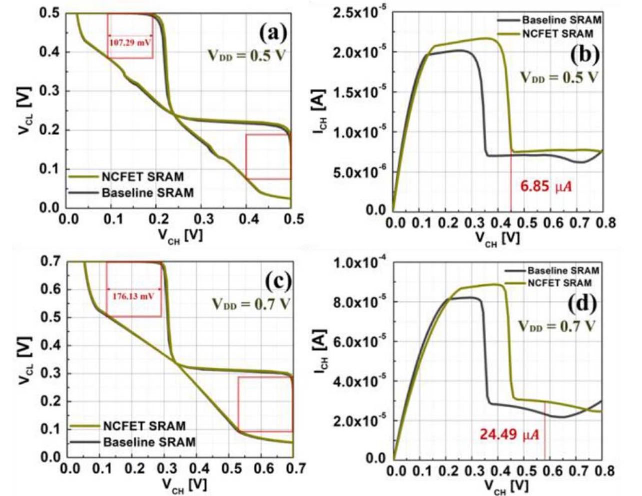

FIGURE 4. (a) Read-stability and (b) write-ability of SRAM at V_{DD} = 0.5 V, (c) read-stability and (d) write-ability of SRAM at V_{DD} = 0.7 V. In "butterfly curve", SNM is defined as the side length of the largest square which is fit in the curve. The SNM of NCFET-based SRAM is 107.29 mV at V_{DD} = 0.5 V and 176.13 mV at V_{DD} = 0.7 V. In "N-curve" (which represents write ability), the length of red-colored line in the graph indicates the write-ability current (I_W). Note that I_W of NCFET-based SRAM is 6.85 μA at V_{DD} = 0.5 V and 24.49 μA at V_{DD} = 0.7 V.

Write ability is estimated by write-ability current (I_w). The measurement of I_w can be done by using the Kirchhoff's Current Law (KCL) at the storage node in cell. This is applied to draw I_{CH} (I_{CL}) *vs.* V_{CH} (V_{CL}) plot during the operation of writing '0' and '1' [19]. The net current of the node CH (I_{CH}) can be calculated by

$$\begin{aligned} I_{CH} &= I_{D3}(V_{GS} = V_{WL}, V_{DS} = V_{CH}) \\ &\quad - I_{D5}(V_{GS} = V_{CL} - V_{DD}, V_{DS} = V_{CH} - V_{DD}) \\ &\quad + I_{D1}(V_{GS} = V_{CL}, V_{DS} = V_{CH}) \end{aligned} \tag{3}$$

From the "N-shaped" plot for I_{CH} vs. V_{CH} (i.e., N-curve), I_w is derived.

The estimated SNM and I_w are summarized in Fig. 4 and Fig. 5. The NCFET-based SRAM shows higher SNM when V_{DD} is lower than 0.7 V. This means that, due to the internal voltage amplification in NCFET, the data stored in NCFET-based SRAM cell can be maintained even at the low V_{DD}. However, when V_{DD} is 0.7 V or higher, the NCFET-based SRAM shows slightly worse performance than the baseline SRAM, in terms of read-stability. This indicates that there exists a trade-off between write-ability and read-stability. When SNM is lower, a smaller voltage applied to the bit-line can flip the data stored internally. This can be understood that the higher V_{DD} is, the higher I_w is [see Fig. 5(b)]. Since I_w increases over the entire range of V_{DD}, it can be confirmed that the write-ability of NCFET-based SRAM is significantly improved, compared against that of baseline SRAM.

III. VARIATION-AWARE SENSITIVITY ANALYSIS

Due to various deviations in the process of manufacturing IC chips, device parameters of six transistors that make up a 6-T SRAM bit-cell is not completely fabricated as originally designed. Such process-induced variations include LER

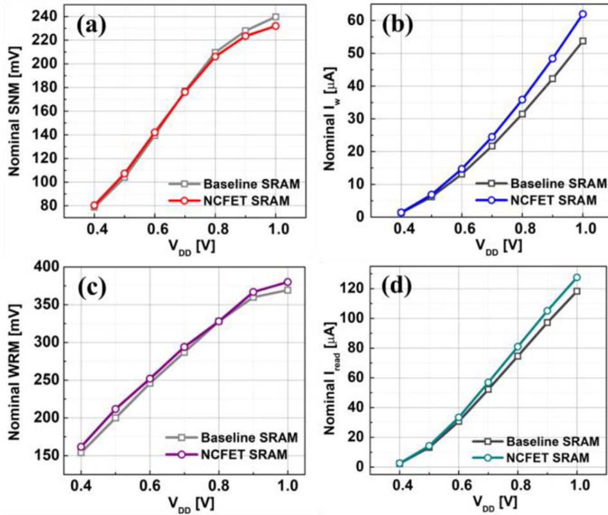

FIGURE 5. (a) Nominal static noise margin and (b) write-ability current for NCFET-based SRAM and MOSFET-based SRAM (baseline SRAM). The NCFET-based SRAM (*vs.* baseline SRAM) has a higher read stability at $V_{DD} = 0.6$ V and below. In terms of write ability, the NCFET-based SRAM tends to be better than the baseline SRAM at all the V_{DD} values. (c) Write noise margin (WRM) vs. V_{DD} for NCFET-based SRAM and baseline SRAM, (d) read-ability current (I_{read}) vs. V_{DD} for NCFET-based SRAM and baseline SRAM.

(Line edge roughness), RDF (Random dopant fluctuation), and WFV (Work function variation). Random variations vary the device parameters, mostly channel width, channel length, and threshold voltage [20].

In this work, the sensitivity of SNM and I_w to each of six transistors (i.e., PD1, PD2, PG3, PG4, PU5, and PU6) are measured by three variation parameters (i.e., channel width, channel length, and V_{Tlin}). V_{Tlin} is the threshold voltage at $I_{DS} = 5$ μA/μm and $V_{DS} = 0.1$ V (threshold voltage was measured by constant current method [21]). Higher sensitivity means that the performance of the SRAM bit-cell changes significantly due to process-induced variation. The greater the sensitivity is, the less the tolerance for the variable is, which in turn degrades the SRAM yield.

The sensitivity of the channel width, length, and V_{Tlin} of NCFET-based SRAM and baseline SRAM are shown in Figs. 6, 7, and 8, respectively. The high drive voltage (i.e., $V_{DD} = 0.7$ V) and low drive voltage (i.e., $V_{DD} = 0.5$ V) are compared. In Fig. 6(c), the sensitivity of SNM to channel width shows that the SNM variation of PG3 in the NCFET-based SRAM is +11 mV when the variation is −0.025 μm. Compared to +37 mV in Fig. 6(a), it has very low deviation from the original SNM value. The variation in I_w is −16 μA [see Fig. 6(b)] and −4 μA [see Fig. 6(d)], which resulted in the fact that, as V_{DD} decreases, the sensitivity in channel width decreases. Figure 7 indicates that the sensitivity of SNM to channel length at $V_{DD} = 0.7$ V is similar as that at $V_{DD} = 0.5$ V. However, the sensitivity of I_w to channel length decreases significantly. In Fig. 7(c), the sensitivity of PG2 in NCFET-based SRAM is noticeably lower than that in baseline SRAM [see Fig. 7(g)]. Figure 8 shows that the sensitivity of SNM and I_w to V_{Tlin} has a resembling tendency regardless of V_{DD} scaling.

Taken together, when $V_{DD} = 0.5$ V, the width variation has little effect on the change of SNM and I_w values, and the length variation greatly affects the variation of SNM. In particular, the deviation in threshold voltage has a similar impact on SNM and I_w, irrespective of V_{DD}. Therefore, more focus on threshold voltage variation is required when designing an SRAM bit-cell that operates at low drive voltage. In addition, the variance in channel width and length is closely related to the threshold voltage of CMOS devices [22], so that the design with the consideration of all the variables is necessary to achieve high yield.

IV. YIELD ESTIMATION OF NCFET-BASED SRAM

Yield estimation of 6-T SRAM array was performed, by taking advantages of using the sensitivities of SNM and I_w. Cell sigma (σ) is defined as the value of minimum variation that causes the failure of SRAM cell operation [6]. For example, the cell sigma of 6σ is corresponding to the 3 fail bits out of 1 Mbit SRAM array. Using the cell sigma concept, we can do the quantitative diagnosis for manufacturing yield management. When SNM and I_w are called the metric, "f", and the parameter variation is "x_i", the metric "f" follows the Gaussian distribution by the central limit theorem [23].

$$\text{Cell sigma} = \frac{f(0)}{\sqrt{\sum_i \left(\frac{\partial f}{\partial x_i}\right)^2 \sigma_{x_i}^2}} \tag{4}$$

In this work, there are three variables (x_i): channel width (W), channel length (L), and V_{Tlin}. To measure the sensitivity and cell sigma, the variation vector is used; the variation vector of W and L were 0.002 μm, and that of V_{Tlin} is 0.01 V.

The yield of SRAM bit-cell is measured/evaluated in the unit of cell sigma (see Fig. 9). Baseline SRAM is designed with a target of six sigma yield at $V_{DD} = 0.6$V, which comes from the power supply voltage projected in the IRDS logic core device technology roadmap. In the NCFET-based SRAM, a huge increase in both read-stability cell sigma (σ_{SNM}) and write-ability cell sigma (σ_{Iw}) at $V_{DD} = 0.4$ V and 0.5 V was observed. In addition, when $V_{DD} = 0.6$ V or higher was confirmed to have the cell sigma > 6.

The yield enhancement in read/write cell sigma at the power supply voltage close to the sub-threshold region (i.e., $V_{DD} = 0.4$ V and 0.5 V) in NCFET-based SRAM results from the fact that the NCFET-based SRAM cell is driven with devices with subthreshold slope < 60 mV/decade at 300 K. It can be concluded that the NCFET-based SRAM (*vs.* baseline SRAM), which is specifically designed for V_{DD} of 0.5 V, can satisfy the requirement in IRDS roadmaps of 2034 and later.

The results of yield estimation for a single variable (i.e., W, L, and V_{Tlin}) are shown in Fig. 10. When the width

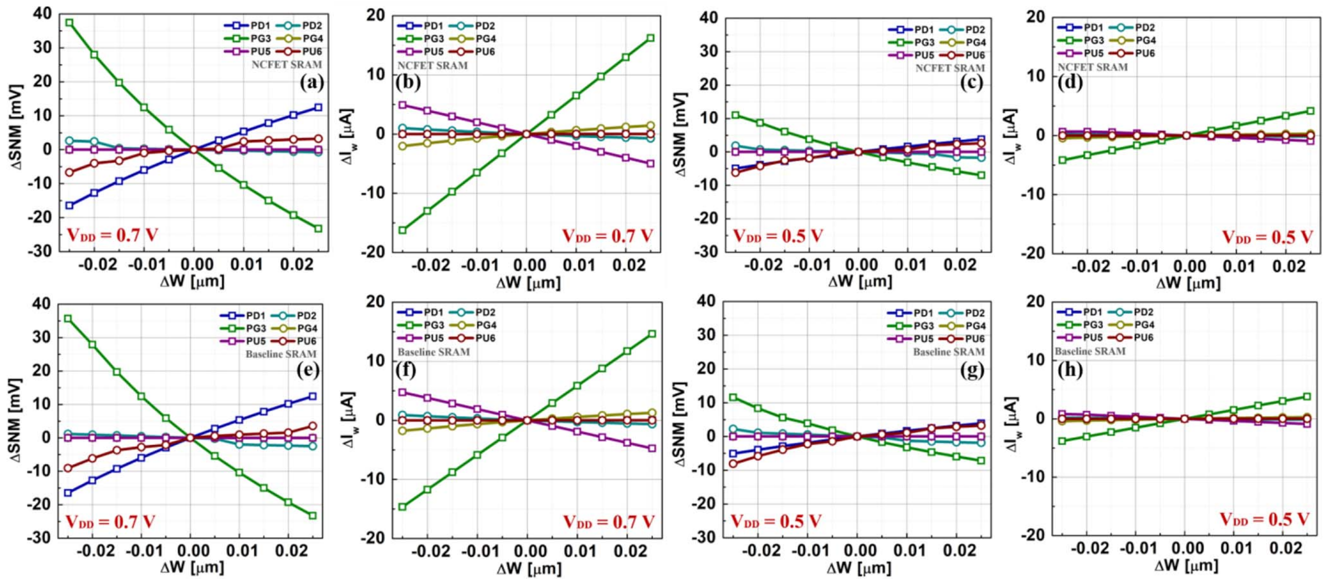

FIGURE 6. Sensitivities of SNM and I_W to channel width for CH node. (a)~(d) are for NCFET-based SRAM, and (e)~(h) are for baseline SRAM. The channel width variation is from −0.025 μm to +0.025 μm (i.e., 10 points were estimated at intervals of 0.005 μm). Note that PD, PG and PU transistor has the channel width of 0.1 μm, 0.05 μm, and 0.04 μm respectively. The steeper the slope of the graph is, the larger the sensitivity is. Therefore, the most sensitive device with respect to the channel width variation is PG3 at all cases.

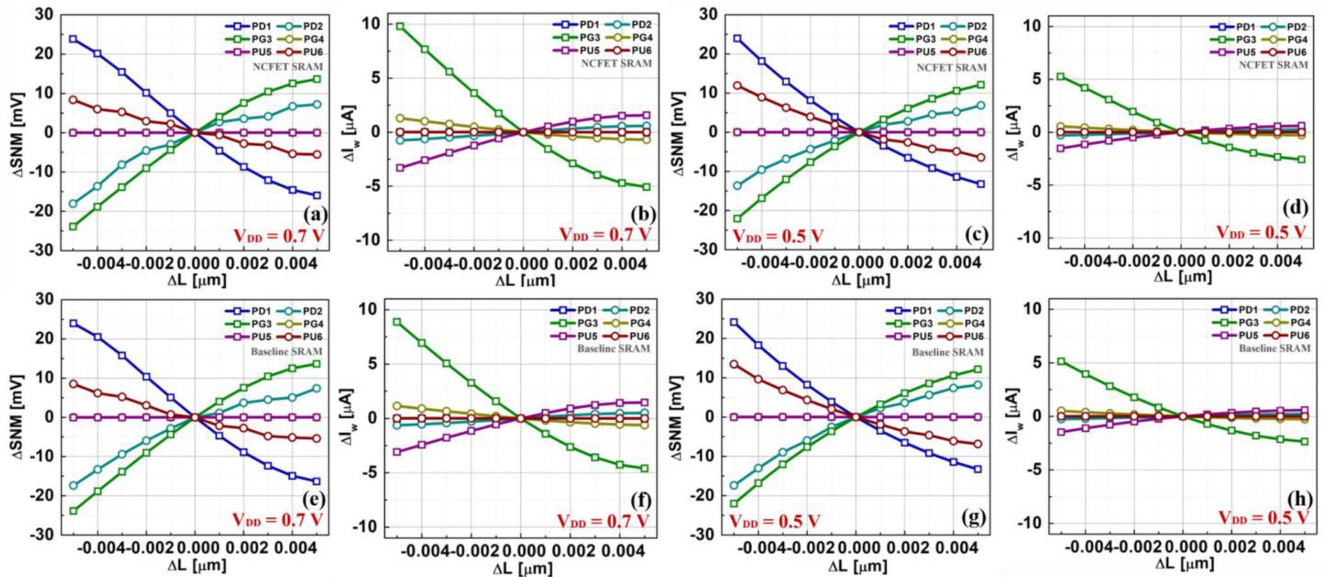

FIGURE 7. Sensitivities of SNM and I_W to channel length for CH node. (a)~(d) are for NCFET-based SRAM, and (e)~(h) are for baseline SRAM. The channel length variation is from −0.005 μm to +0.005 μm (i.e., 10 points were estimated at intervals of 0.001 μm). Note that PD, PG and PU transistor has the same channel length of 0.02 μm. PD1 and PG3 transistors have the largest SNM sensitivity, and PG3 has the highest I_W sensitivity.

variation was only applied [see Figs. 10(a) and (b)] and the V_{Tlin} variation was only applied [see Figs. 10(e) and (f)], both NCFET-based SRAM and baseline SRAM satisfies the 6-sigma of read/write operation at $V_{DD} = 0.4$ V or higher. On the other hand, when the length variation was only applied [see Figs. 10(c) and (d)], cell sigma values of read-stability and write-ability were measured analogous to those when all three variables were applied. In terms of the case which the variation vector of W and L were 0.002 μm and that of V_{Tlin} is 0.01 V, channel length variation has the greatest effect in yield estimation, in terms of cell sigma. The transistors used in the SRAM bit-cell in this work has the short channel length of 20 nm, which is considered to be the most critical factor. Therefore, NCFET, which only needs a process of adding a ferroelectric material over its gate oxide in the same baseline transistor device structure, can be a good choice for yield improvement at low power supply voltage, when 20nm-long short channel devices are used in SRAM bit-cell.

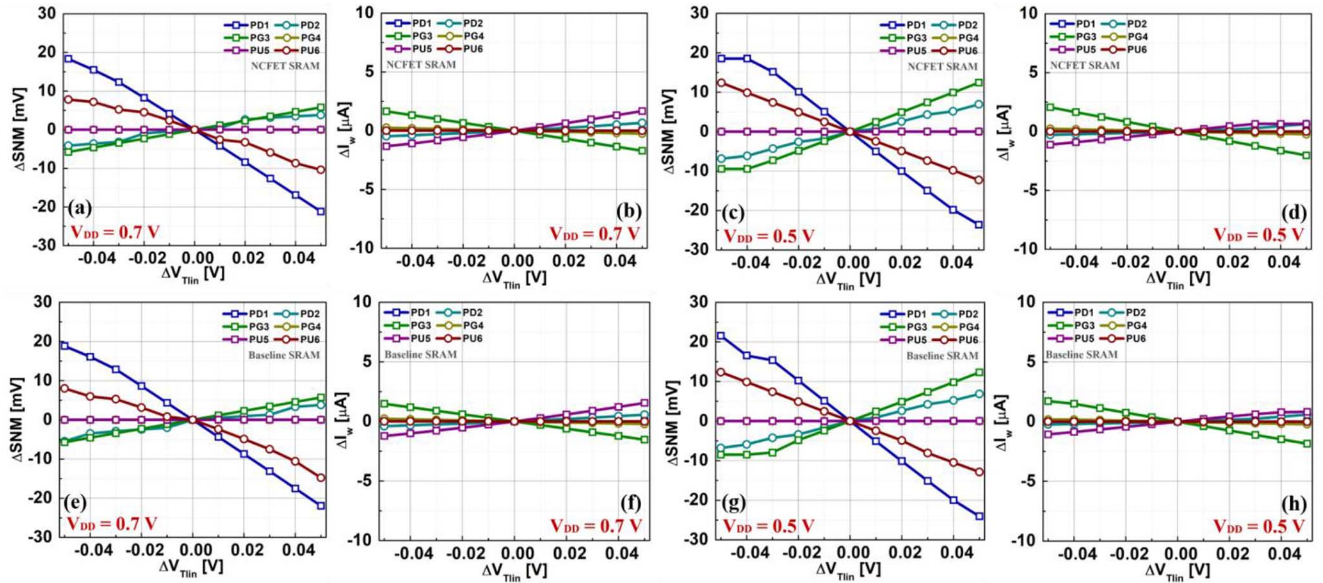

FIGURE 8. Sensitivities of SNM and I_W to V_{Tlin} for CH node. (a)~(d) are for NCFET-based SRAM, and (e)~(h) are for baseline SRAM. V_{Tlin} variation is from −0.05 V to +0.05 V (i.e., 10 points were estimated at intervals of 0.01 V). Note that NMOS (i.e., PD and PG) and PMOS (i.e., PU) transistor has the V_{Tlin} of 0.34 V and 0.37 V, respectively. PD1 has the largest SNM sensitivity, and PG3 has the largest I_W sensitivity.

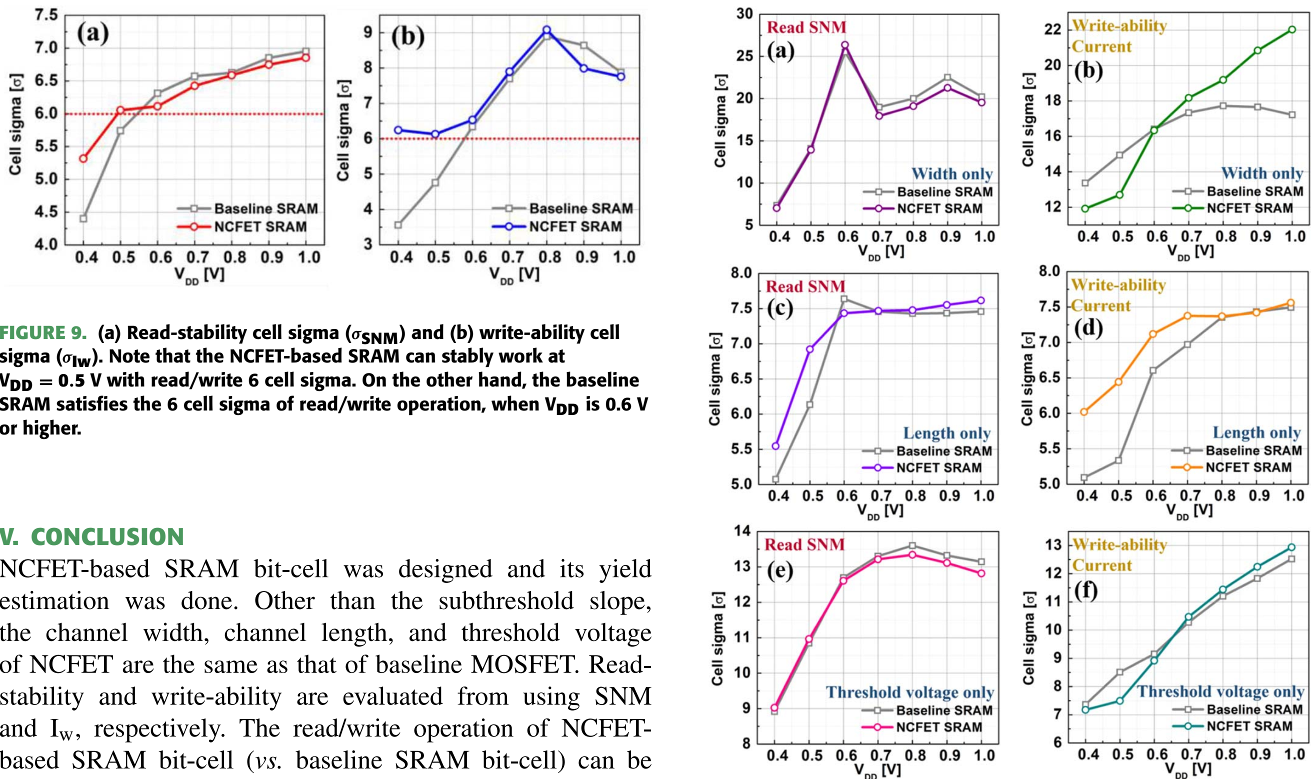

FIGURE 9. (a) Read-stability cell sigma (σ_{SNM}) and (b) write-ability cell sigma (σ_{Iw}). Note that the NCFET-based SRAM can stably work at $V_{DD} = 0.5$ V with read/write 6 cell sigma. On the other hand, the baseline SRAM satisfies the 6 cell sigma of read/write operation, when V_{DD} is 0.6 V or higher.

FIGURE 10. Read-stability cell sigma (left) and write-ability cell sigma (right). (a), (b) is only for a channel width, (c), (d) for a channel length, and (e), (f) for a threshold voltage. Note that the NCFET-based SRAM can stably work at $V_{DD} = 0.5$ V with read/write 6 cell sigma for a length variable, in (c) and (d).

V. CONCLUSION

NCFET-based SRAM bit-cell was designed and its yield estimation was done. Other than the subthreshold slope, the channel width, channel length, and threshold voltage of NCFET are the same as that of baseline MOSFET. Read-stability and write-ability are evaluated from using SNM and I_w, respectively. The read/write operation of NCFET-based SRAM bit-cell (*vs.* baseline SRAM bit-cell) can be better at V_{DD} of near the subthreshold regime. The yield estimation is based on the cell sigma concept, and the variables for estimating the cell sigma are W, L, and V_{Tlin}. The tendency of cell sigma is related with nominal SNM and I_w. When 20nm-long short channel devices are used in SRAM bit-cell, the channel length variation has been found to have the greatest effect on SRAM yield. The significant increase was observed in both σ_{SNM} and σ_{Iw} at $V_{DD} = 0.4$ V and 0.5 V in NCFET-based SRAM. Especially, representing six sigma at $V_{DD} = 0.5$V means that the IRDS roadmaps for the year of 2034 and later can be realized with NCFET-based SRAM bit-cell. As the promising device for lower power

applications, NCFET can utilized as SRAM devices thanks to its super steep-switching characteristic. The NCFET-based SRAM bit-cell can be a good choice in terms of maintaining high yield at near-threshold voltage of V_{DD}.

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