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A New 8T Hybrid Nonvolatile SRAM With Ferroelectric FET

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ABSTRACT This paper proposes a new 8T nonvolatile SRAM (nvSRAM) cell employing ULP FinFETs and ferroelectric FinFETs to enable energy-efficient and low-latency store/recall operations. Different from other types of nvSRAM requiring additional circuitry or nonvolatile memories connected to a standard 6T SRAM cell to achieve nonvolatility, the proposed hybrid nvSRAM cell reduces the area penalty by embedding the nonvolatile ferroelectric FinFETs in a 6T SRAM cell without sacrificing the cell stability, read/write performance and power consumption.

INDEX TERMS Ferroelectric field-effect transistor FET, negative-capacitance FET (NCFET), FinFET, nonvolatile SRAM (nvSRAM), nonvolatile memory.

I. INTRODUCTION

In order to realize the ultra-low power computing near memory system, a compact and fast embedded nonvolatile memory is expected to be important [1], [2]. Several nonvolatile SRAM (nvSRAM) solutions with additional circuitry or nonvolatile memories (e.g., RRAM, MTJ, etc.) connected to a 6T SRAM cell have been proposed [3]–[10]. Nevertheless, the added cost of integrating the nonvolatile memory with advanced logic technology and the large off-on energy ($E_{S\&R}$) due to store and recall operations are unsatisfactory [5].

To overcome these limitations, a 6T2C nvSRAM cell with two ferroelectric capacitors connected to a conventional 6T SRAM cell has been proposed recently [10]. However, the additional two ferroelectric capacitors enabling the nonvolatility lead to a large area penalty compared with using transistors.

Thanks to the recent discovery of ferroelectricity in doped hafnium-oxide [11], the ferroelectric FET with CMOS compatibility and scalability has garnered substantial interest.

In this work, we propose a new 8T hybrid nvSRAM cell (as shown in Fig. 1) employing FinFETs and ferroelectric FinFETs to achieve energy-efficient data storage with reduced area overheads. The read/write static noise margins and performance of 8T hybrid nvSRAM are also addressed.

This paper is organized as follows. In Section II, we describe the device design and simulation methodology. In Section III, the voltage conditions and operating principles for the 8T hybrid nvSRAM during the store/recall period are illustrated. The read/write operation, cell stability, performance and power consumption are examined in Section IV. Finally, the conclusion is drawn in Section V.

II. DEVICE DESIGN AND SIMULATION METHODOLOGY

Different from the hysteresis-free negative-capacitance FETs (NCFETs) that are promising for performing low-power Boolean logic operations in processing units, the ferroelectric FinFETs (see Fig. 2(a)) in the hybrid nvSRAM cell is designed to have two nonvolatile stable states in the hysteresis loop around $V_{gs} = 0$V in Figs. 2(b) and 2(c). One state can switch to the other by applying a sufficiently positive or negative V_{gs} pulse that exceeds the coercive voltage (~0.2V in this work) [13]. Even though the device is powered-off, the two polarization states in ferroelectric FET can still be maintained [14], [15]. This hysteresis characteristic can be achieved by capacitance engineering where the

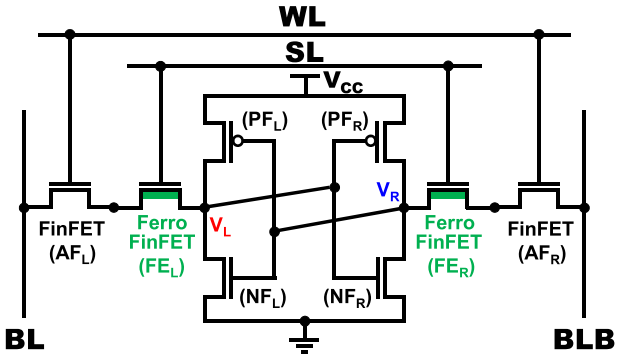

FIGURE 1. Schematic of proposed 8T hybrid nonvolatile SRAM cell. WL, BL/BLB, and SL are the word line, bit line, and storage line, respectively.

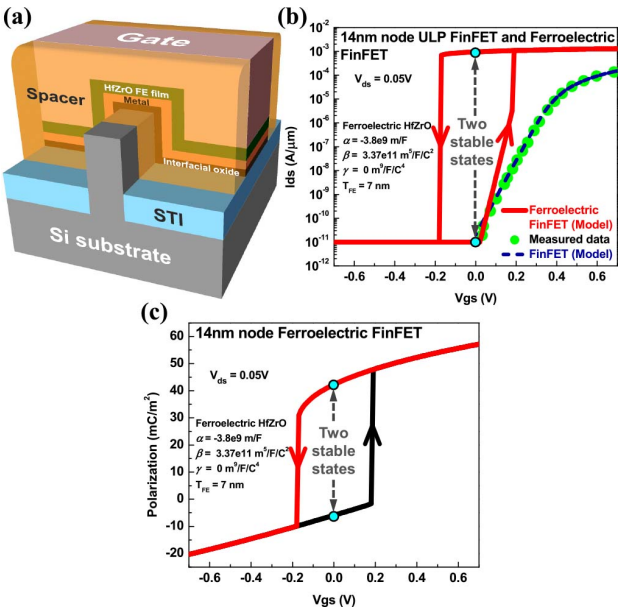

FIGURE 2. (a) Schematic of a ferroelectric FinFET structure. (b) I_{ds}-V_{gs} characteristics of the ferroelectric FinFET and the 14nm-node Ultra-Low-Power (ULP) FinFET [12]. Note that the hysteretic I_{ds}-V_{gs} and (c) polarization P-V_{gs} characteristics with two stable nonvolatile states in ferroelectric FinFET straddle V_{gs} = 0V by design.

value of ferroelectric capacitance $|C_{FE}|$ is made smaller than that of internal FinFET (metal) gate capacitance C_{mos} [16].

In this work, the ferroelectric FinFET is modeled by coupling the surface-potential-based BSIM-CMG model [17] with the time-dependent Landau-Khalatnikov equation [18] which has been adopted by [14], [19], [20]. (The floating metal gate between the interfacial oxide and the FE film in Fig. 2(a) is needed to implement this modeling approach. It may not be a necessary part of the ferroelectric FinFET design.) The short-channel gate charge model of the underlying FinFET, Q_{mos}, (i.e., the polarization charge seen by the ferroelectric) is derived based on an analytical short-channel surface potential equation of FinFETs [21], [22]. The model is self-consistently solved in the SPICE circuit simulator. We first calibrate the model of the underlying baseline FinFET with the reported data of a 14nm-node Ultra-Low-Power (ULP) FinFET

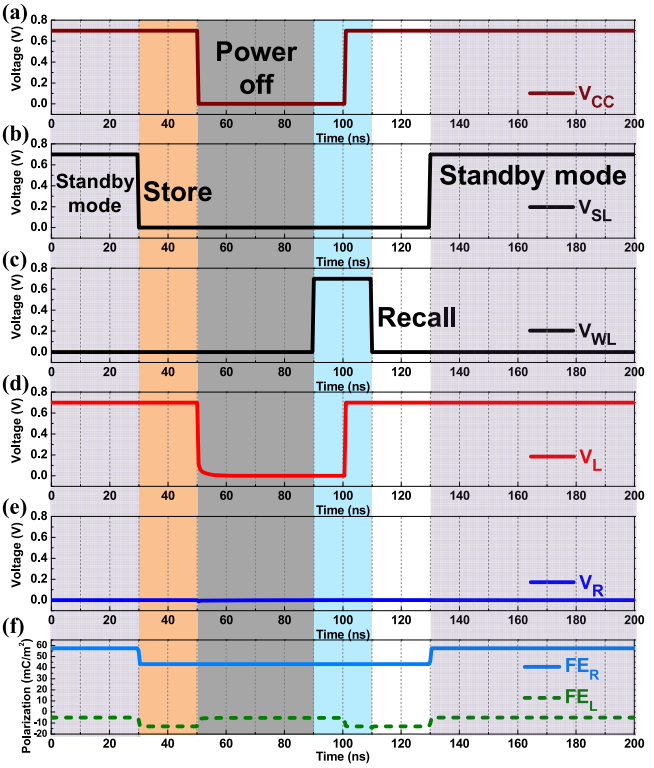

FIGURE 3. The transient waveforms of the proposed 8T hybrid nvSRAM during data storage and recall operations.

technology [12] shown in Fig. 2(b). The parasitic capacitance is estimated (∼0.14fF/μm) with 3D TCAD simulation [23] for the calibrated FinFET. The ferroelectric parameters of HfZrO used in this work are: $\alpha = -3.8 \times 10^9$ m/F, $\beta = 3.37 \times 10^{11}$ m^5/F/C^2 and $\gamma = 0$ m^9/F/C^4. These values were obtained based on the remnant polarization (P_r) and coercive field (E_c) data of HfZrO in [24]. The value of damping constant $\rho = 0.25$ Ωm has been adopted as in [14]. In our circuit evaluation, the front-end-of-line (FEOL) and back-end-of-line (BEOL) capacitive load is estimated based on the 14nm technology node [25].

III. OPERATION PRINCIPLE OF PROPOSED 8T HYBRID NVSRAM

Before the power failure, the data in cell storage nodes V_L and V_R should be stored in the ferroelectric FinFETs (FE_L and FE_R in Fig. 1). To demonstrate the nonvolatile characteristic in the proposed hybrid nvSRAM, the transient waveforms and their corresponding operation points in P-V_{gs} at each operation stage are shown in Fig. 3 and Fig. 4, respectively. The state of the nvSRAM is assumed to be "1" at V_L and "0" at V_R.

Normally, the SL is set to V_{DD} as shown at t = 0 in Fig. 3(b). The polarization in FE_L is at the low polarization state (i.e., at the subthreshold regime in Fig. 2(b)) while the polarization in FE_R is at the high polarization state (i.e., at the strong inversion regime in Fig. 2(b)) as shown in Fig. 4(a). The polarization states in FE_L and FE_R are determined by the state stored in V_L and V_R, respectively. The V_{gs} of FE_L

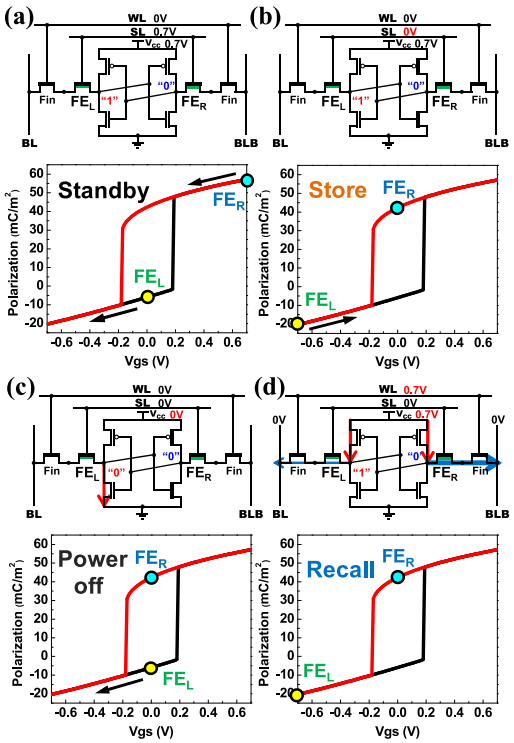

FIGURE 4. Schematics of hybrid nvSRAM voltage bias conditions and the corresponding operation points in *P-V*$_{gs}$ at each operation stage. The directions of arrows represent the movements of polarization states from the current stage to the next stage.

is zero due to the logical "1" at V_L, while the V_{gs} of FE$_R$ is V_{DD} due to the logical "0" at V_R. Before power-off, to ensure the polarization in FE$_L$ keeping at a low polarization state (i.e., prevent from the logical "1" at V_L discharging to logical "0" before the SL power-off), the SL is pulled down to *GND*. Note that, at this step, the polarization state in FE$_R$ remains stable as shown in Fig. 3(f). After the data storage operation, the power supply (V_{CC}) can be turned-off. Even after V_L is discharged to *GND*, the polarization states in FE$_L$ and FE$_R$ are still maintained (see Fig. 3(f)).

In Fig. 3(c), during the recall period, WL is pulled up to V_{DD} before the nvSRAM wakes up and provides a low resistance path from V_R to ground, and contrarily, a high resistance path from V_L to ground. After that, V_{CC} is pulled up to V_{DD} and charges both cell storage nodes V_L and V_R by the P-type FinFETs (see Fig. 4(d)). Because of different strength to pull down V_L and V_R by the bit line capacitances (see Fig. 4(d)), the node voltages are restored to the previous states before power-off. After V_L and V_R settle down, the SL is pulled up to V_{DD}, and the nvSRAM is ready to resume operation as a regular SRAM. Note that, the polarization states in FE$_L$ and FE$_R$ are not changed during the recall operation.

IV. READ/WRITE SNMS AND PERFORMANCE EVALUATION

Although there are several other nvSRAM architectures [3]–[10], they introduce nonvolatile memories

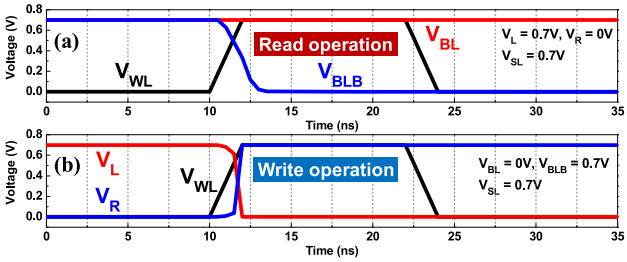

FIGURE 5. Transient waveforms of proposed 8T hybrid nvSRAM cell during (a) read and (b) write operations.

outside the 6T SRAM cell without changing the read/write operations, cell stability and performance of basic 6T SRAM cell. However, with ferroelectric FinFETs directly embedded in the proposed hybrid nvSRAM cell, its read/write operations, cell stability and performance should be further investigated.

Fig. 5 shows the transient waveforms of read and write operations. During the read operation (see Fig. 5(a)), the BL and BLB are precharged to V_{DD}. The SL is raised to V_{DD} to provide low resistance paths from cell storage nodes to the access pass-gate transistors (AF$_L$ and AF$_R$ in Fig. 1), so the read operation is still initiated by enabling the WL. Other voltage conditions are also similar to a conventional 6T SRAM during the read period. The BL and BLB capacitance of 16.8 fF is estimated for 64 cells per bit line [26] and adopted in all our simulations. Fig. 5(b) demonstrates the capability of bit writing in the hybrid nvSRAM cell. During the write operation, the SL is raised to V_{DD}. Once the WL is enabled, the bit lines can successfully flip the state of the cell. Then, the write process is completed.

Fig. 6 shows the comparison of read and write static noise margins (RSNM and WSNM) between the proposed 8T hybrid nvSRAM and conventional 6T SRAM. It can be seen that, in addition to the RSNM and WSNM, the read/write disturb voltages ($V_{read,0}$ and $V_{write,0}$) of the proposed 8T hybrid nvSRAM cell are comparable with that of the conventional 6T SRAM cell. Although there exists an embedded ferroelectric FinFET connecting the cell storage node and access pass-gate transistor in the hybrid nvSRAM cell, the voltage divider effect is negligible due to the relatively high ON-state current of ferroelectric FinFET (compared with the FinFET) shown in Fig. 2(b). Therefore, the read and write stabilities are still determined by the strength ratios of the pull-down transistor to the access pass-gate transistor and access pass-gate transistor to the pull-down transistor using FinFETs, respectively, which is similar to the design of a conventional 6T SRAM. This characteristic substantially reduces the complexity of the hybrid nvSRAM design.

Fig. 7 shows the comparison of cell performance between the proposed 8T hybrid nvSRAM and conventional 6T SRAM cells. Because the ferroelectric FinFET with a relatively higher ON-state current lessens the voltage divider effect between the cell storage node and the access pass-gate transistor, the read current is only determined by the access pass-gate transistor and pull-down

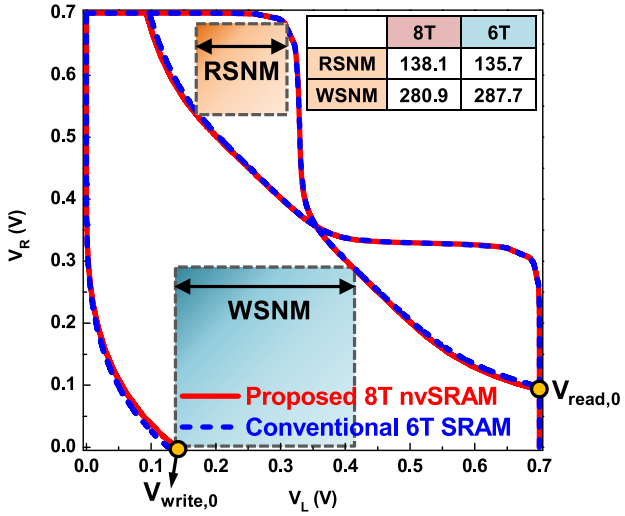

FIGURE 6. The RSNM and WSNM of proposed 8T hybrid nvSRAM cell are comparable to that of conventional 6T SRAM cell.

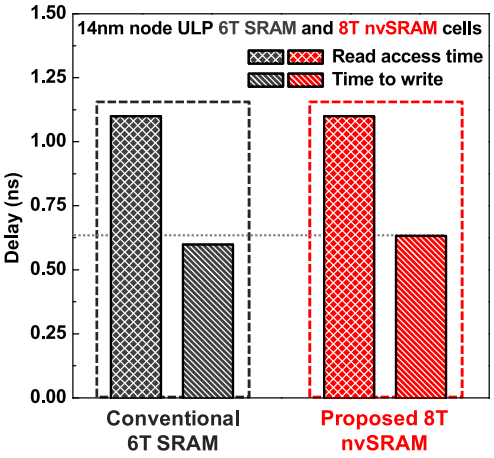

FIGURE 7. Comparable read/write performance of proposed 8T hybrid nvSRAM and conventional 6T SRAM cells. A slight increase in time-to-write of proposed 8T hybrid nvSRAM cell results from the enhanced gate capacitance in ferroelectric FinFET.

transistor using FinFETs. Thus, the read access time of the 8T hybrid nvSRAM is nearly identical to that of the conventional 6T SRAM. Based on the same reason, the time-to-write of 8T hybrid nvSRAM is comparable with the conventional 6T SRAM. A slight increase in time-to-write of a 8T hybrid nvSRAM cell results from the enhanced gate capacitance in the ferroelectric FinFET, especially for the ferroelectric FinFET with a thicker ferroelectric thickness (T_{FE}) [27], [28]. Nevertheless, the impact of enhanced gate capacitance of a ferroelectric FinFET on the read access time can be negligible due to the existence of the bit line capacitance which dominates the overall capacitance for the nvSRAM during the read operation. This can also explain the comparable energy consumption during the read and write operations between the proposed 8T hybrid nvSRAM and conventional 6T SRAM cells shown in Fig. 8.

The power off-on energy ($E_{S\&R}$) and break-even-time (BET) are critical energy-performance

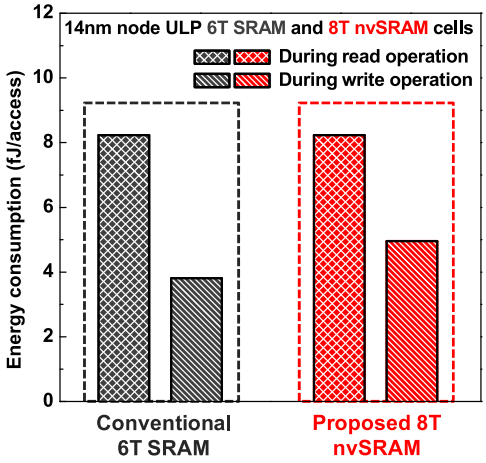

FIGURE 8. Comparable energy consumption during the read and write operations of proposed 8T hybrid nvSRAM and conventional 6T SRAM cells.

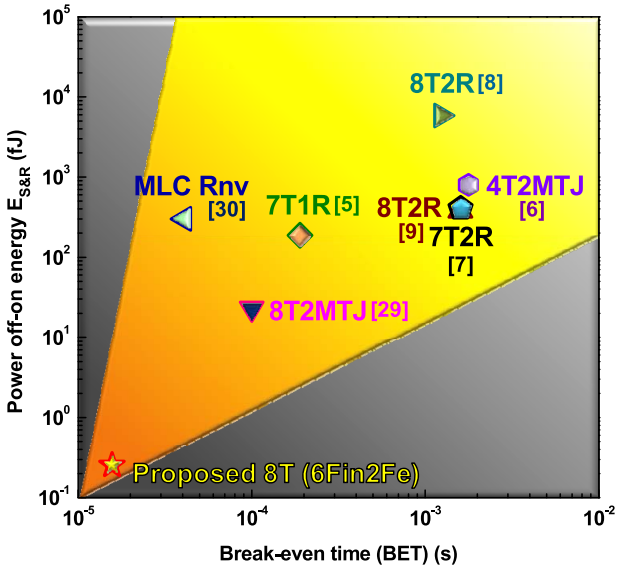

FIGURE 9. Comparison of power off-on energy ($E_{S\&R}$) and break-even time (BET) for various nvSRAMs. The $E_{S\&R}$ of the proposed 8T nvSRAM with ferroelectric FETs is simulated and extracted with 1μs power supply ramp-up time.

indices of nonvolatile logic circuits for power gating applications [3]. Fig. 9 shows the $E_{S\&R}$ and BET data for RRAM and MTJ based nvSRAMs [5]–[9], [29], [30]. In general, the nvSRAM based on MTJ devices (particularly the advanced SHE/SOT driven MTJs [31], [32]) can achieve superior energy efficiency than the RRAM based counterparts. It can be revealed from Fig. 9 that, compared with the simulated MTJ (8T2MTJ [29]) based nvSRAM, the proposed 8T nvSRAM with ferroelectric FETs can achieve better energy-efficiency and energy savings during the power gating which is favorable for the frequent data access. Note that the ferroelectric FinFET thoroughly gets shot of the large static current in RRAM and MTJ based nvSRAMs during store and recall operations.

V. CONCLUSION

To realize the ultra-low power computing system, we propose a new 8T hybrid nvSRAM cell employing FinFETs and ferroelectric FinFETs. The proposed hybrid nvSRAM cell demonstrates the nonvolatility with superior energy-efficiency during store and recall operations. Therefore, compared with the existing 6T2C nvSRAM with additional ferroelectric capacitors to achieve nonvolatility, the proposed 8T hybrid nvSRAM reduces the area penalty without sacrificing the cell stability, read/write performance and energy consumption.

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