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Trap Analysis Based on Low-Frequency Noise for SiC Power MOSFETs Under Repetitive Short-Circuit Stress

J. L. WANG[1,2], Y. Q. CHEN[1] (Member, IEEE), J. T. FENG[2], X. B. XU[2], Y. F. EN[1] (Member, IEEE), B. HOU[1], R. GAO[1], Y. CHEN[1] (Member, IEEE), Y. HUANG[1] (Member, IEEE), AND K. W. GENG[2] (Member, IEEE)

1 Science and Technology on Reliability Physics and Application of Electronic Component Laboratory, No.5 Electronics Research Institute of the Ministry of Industry and Information Technology Guangzhou, Guangzhou 510610, China

2 School of Electronic and Information Engineering, South China University of Technology, Guangzhou 510000, China

CORRESPONDING AUTHORS: Y. Q. CHEN, Y. F. EN, AND K. W. GENG (e-mail: yiqiang-chen@hotmail.com; enyf@ceprei.com; gengkw@scut.edu.cn)

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ABSTRACT In this paper, the degradation behavior of the electrical characteristics was investigated, and trap analysis based on low-frequency noise (LFN) was carried out for the commercial 1.2-kV/30-A silicon carbide (SiC) power MOSFETs under repetitive short-circuit (SC) stress. The experiment results show that the on-state resistance (R_{dson}) and threshold voltage (V_{th}) increase significantly. Meanwhile, the drain-source current (I_{ds}) decreases obviously with the increase of the SC cycles. Furthermore, the gate-source leakage current (I_{gss}) of the SiC power MOSFETs increase greatly and the blocking characteristics deteriorated after 1000 SC cycles. The positive shift was observed on the gate-capacitance versus gate-voltage (C_g-V_g) curve, which shows that the damage region could be in channel along the SiC/SiO_2 interface after repetitive SC stress. In order to obtain the trap information, trap characterization was performed by using LFN method, and the LFN results show that the trap density increases with the SC cycles. The physical mechanism could be attributed to electrically active traps generated at SiC/SiO_2 interface and oxide layer due to the peak ionization rate, the perpendicular electrical field and high temperature during SC stress. The study may be useful to provide reference for converters design and fault protection of SiC power MOSFETs.

INDEX TERMS Repetitive short-circuit (SC), low-frequency noise (LFN), traps, silicon carbide (SiC) power MOSFETs.

I. INTRODUCTION

Silicon carbide (SiC) material has been recognized as a prime option for increasing the power density, system switching frequency and system efficiency of power electronics due to its superior properties [1]–[3]. In recent twenty years, SiC MOSFETs have been widely applied in power electronics device with the rapid improvement of material fabrication technology [4]. However, in most applications, SiC power MOSFETs can suffer from extreme operating conditions that result in degradation, such as low channel mobility [5], poor reliability [6] and so on. Therefore, it is important to explore the reliability of SiC power MOSFETs.

Power semiconductor devices are expected to function for short amount of times outside their designed safe-operating area without any impact on the device performance. Among of them, short-circuit (SC) operation is inevitable, and the SC capability is a crucial indicator of SiC power MOSFETs reliability [7]. Recently, some papers have been dedicated to the SC behavior of SiC power MOSFETs. The electrical properties of 1.2-kV/10-A SiC power MOSFETs under repetitive SC stress were reported, and the dominant mechanism was attributed to negative charges generated along the SiC/SiO2 interface of the channel region [8]. The robustness and electro-thermal instability of 1.2-kV SiC power

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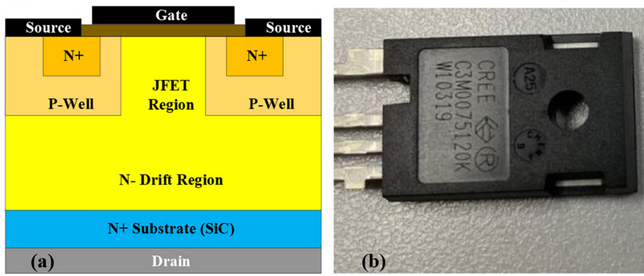

FIGURE 1. Device structure: (a) the schematic diagram of cross section and (b) photograph of 1.2-kV/30-A SiC power MOSFETs.

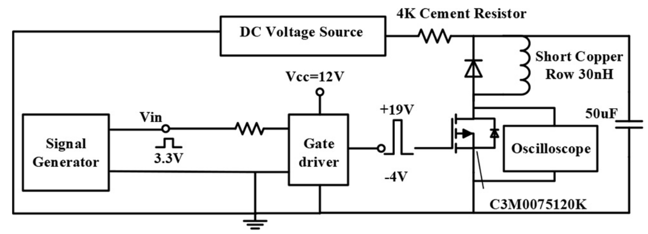

FIGURE 2. Schematic diagram of the test circuit.

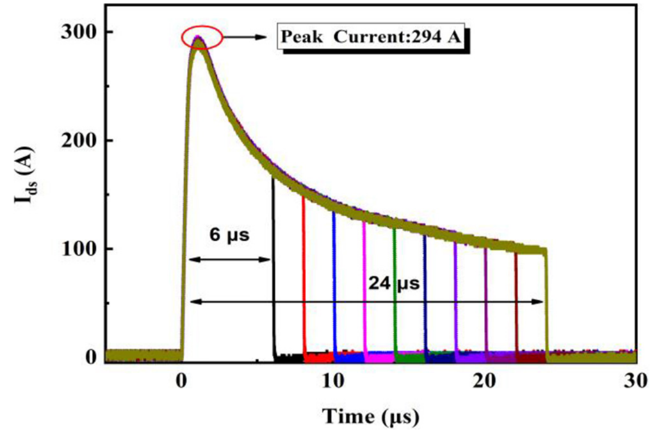

FIGURE 3. Current waveforms of the SiC power MOSFETs during the SC stress under the conditions of V_{gs} = 19 V and V_{DD} = 250 V.

MOSFETs were investigated under the SC stress, and it was found that the gate was weakness [9], [10]. Under repetitive 6-kV dc-link voltage stress, the on-state resistance (R_{dson}) increases significantly for the 10-kV/10-A 4H-SiC MOSFET [11]. There are also reports on the comprehensive SC ruggedness evaluation and numerical investigation of 1.2-kV SiC MOSFETs [12]. The gradual reduction on the gate-source voltage (V_{gs}) in SiC power MOSFETs was investigated during SC condition, which results in the increases of gate-source leakage current (I_{gss}) due to the smaller thicknesses of the gate oxide [13].

Low frequency noise (LFN) measurements are presented to be a powerful tool to evaluate the quality and reliability of Si and SiC based MOS transistor [14]–[16]. LFN of Si MOSFETs has been extensively studied [17]. The temperature-dependent LFN of 4H-SiC MOSFETs with nitride oxides was reported over the temperature range 85-510 K, and the $1/f$ noise decreases significantly with increasing measurement temperature [18]. LFN in 4H-SiC JFETs has been investigated, and these extremely low noise values were determined by the noise at the SiC/SiO_2 interface [19]. The $1/f$ noise in 4H-SiC MOSFETs with epitaxial channel has been investigated, and it was shown that the density of negative oxide traps are responsible for $1/f$ noise [20]. The bulk LFN has been investigated on the 4H-SiC polytype, and in the temperature range of 300-550 K the noise spectral density S is proportional to $1/f^{1.5}$ [21]. The noise power spectra for n-channel, depletion-mode MOSFETs fabricated in 6H-SiC material was measured from 1 Hz to 100 kHz at room temperature and the noise power spectra were found to be dependent upon the drain-source current (I_{ds}) density [22]. The LFN was studied in 4H-SiC MOSFETs in the frequency range from 1 Hz to 100 kHz, and the dependence of the normalized noise power spectra (S_I/I_{ds}^2) on I_{ds} at constant drain-source voltage (V_{ds}) was qualitatively different from typical dependence for n-channel Si MOSFETs [23]. However, to our best knowledge, very limited research efforts have been focused on the degradation analysis and physical mechanism of SiC power MOSFETs based on LFN measurements.

In this paper, the degradation behavior of the electrical characteristics was investigated, and trap analysis based on LFN was carried out for the commercial 1.2-kV/30-A SiC power MOSFETs under repetitive SC stress. The effect of repetitive SC stress on the gate oxide and body diode were explored. The corresponding physical mechanism for the effect of traps increasing after repetitive SC stress was also discussed. The results may provide useful reference for converters design and fault protection of SiC power MOSFETs.

II. EXPERIMENTAL

A commercial 1.2-kV/30-A SiC power MOSFET produced by Wolfspeed (C3M0075120K) was chosen as the target device. The schematic diagram of cross section and photograph of the typical device under test (DUT) was shown in Fig. 1. The electrical characteristics were measured by semiconductor device analyzer (Agilent B1505A). And LFN was measured by using SR785 dynamic signal analyzer, while filter and amplifier units were provided by Proplus 9812B. In order to apply repetitive SC stress on the DUT, a circuit shown in Fig. 2 was set up. Repetitive SC tests was performed under the V_{gs} of 19/−4 V and V_{ds} of 250 V. The gate pulse width (T_{sc}) of 20 μs and the interval time of 3 s between repetitive SC cycles were chosen to avoid overheating the device. The SC currents under different T_{sc} were captured by an oscilloscope (Tektronix DPO 5034) as shown in Fig. 3. At the beginning of the gate pulse, I_{ds} rise rapidly to a peak value of 294 A. Then it keeps decreasing during the stress time due to the increase of junction temperature, and it is in agreement with previous result [24].

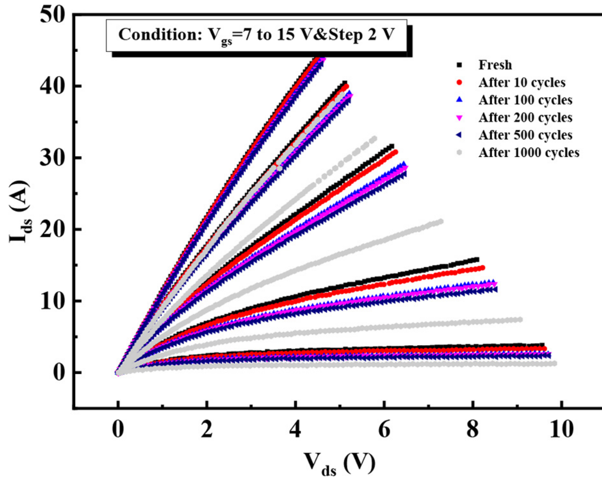

FIGURE 4. Output characteristics of 1.2-kV 30-A SiC power MOSFETs with the increase of SC cycles at V_{gs} = 7, 9, 11, 13 and 15 V.

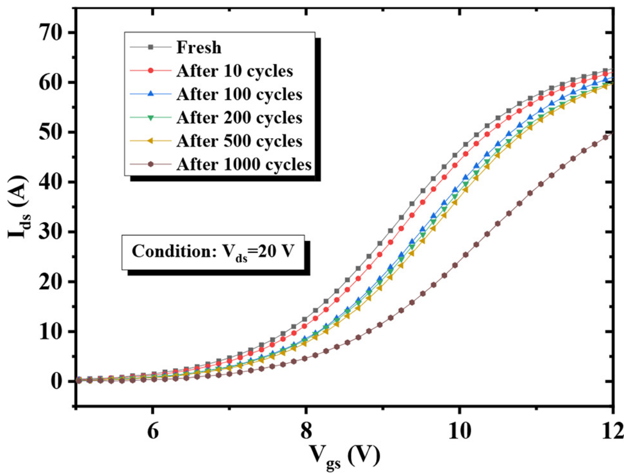

FIGURE 5. Transfer characteristics of 1.2-kV 30-A SiC power MOSFETs with the increase of SC cycles at V_{ds} = 20 V.

III. RESULTS AND DISCUSSION

A. EFFECT OF REPETITIVE SC STRESS ON ELECTRICAL CHARACTERISTICS

To explore the effect of repetitive SC stress on the electrical properties of SiC power MOSFETs, the output characteristics and the transfer characteristics were measured for the fresh devices and the ones after 1000 cycles of repetitive SC stress. the output characteristics of the DUT are plotted in Fig. 4, as for the SiC power MOSFETs after SC stress, the I_{ds} values obviously decrease with the increase of SC cycles at the same V_{gs}. Under the conditions of V_{gs} = 11 V and V_{ds} = 5V, the typical I_{ds} value decrease from 26.76 A to 22.64 A after 500 SC cycles. Moreover, under the same conditions, the typical I_{ds} value decrease from 26.76 A to 16.51 A after 1000 SC cycles. The transfer characteristics are shown in Fig. 5, the transfer characteristics curves shift positively with the increase of SC cycles.

Fig. 6 shows the SC cycles-dependent R_{dson} and V_{th} of SiC power MOSFETs. The values of the R_{dson} and V_{th} increase

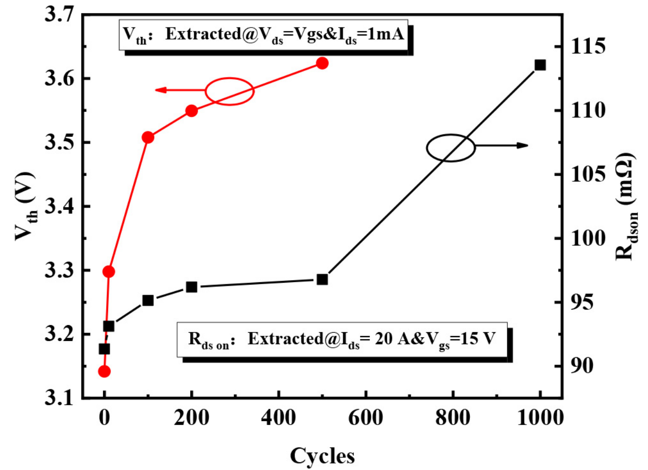

FIGURE 6. V_{th} variation and R_{dson} during the SC stress for a 1.2-kV 30-A SiC power MOSFETs.

with SC cycles. Under the conditions of $V_{ds} = V_{gs}$ and $I_{ds} = 1$ mA, the typical V_{th} value increase from 3.14 V to 3.62 V after 500 SC cycles. Under the conditions of $V_{gs} = 20$ V and $I_{ds} = 20$ A, the typical R_{dson} value increase from 91.34 mΩ to 113.55 mΩ after 1000 SC cycles. It indicates that the effect of SC stress on the device is notable, and the results are in agreement with previous results [8]. The total R_{dson} of power MOSFETs is composed of two parts: the channel resistance (R_{ch}), and the residual resistance (R_s). The R_s of power MOSFETs can be obtained from the dependence of R_{dson} on $(V_g - V_{th})^{-1}$ [25]. Taking the additional account of R_s, the entire R_{dson} of power MOSFETs can be expressed as:

$$R_{dson}=\frac{L}{\mu_n C_{ox} W} \times \frac{1}{V_g - V_{th}} + R_s \tag{1}$$

where L is the gate length, C_{ox} is the gate oxide capacitance, W is the gate width, and μ_n is the electron mobility. With the V_{th} increase the R_{dson} expressed positive correlation with the $(V_g\text{-}V_{th})^{-1}$. The increase of R_{dson} indicated degradation seems to be associated with the channel region, and continuous stressing leads to an overall increase in device R_{dson}, aluminum reconstruction and cavities at the contact interface between the aluminum surface metallization and source contacts maybe occurred during SC stress due to junction temperature increases [11].

Meanwhile, to explore the effect of repetitive SC stress on the gate oxide and the body diode, I_{gss} and the blocking characteristics of the device were also monitored and shown in Fig. 7 and Fig. 8. After 500 SC cycles, the I_{gss} and blocking characteristics remain good stability, while they greatly degrade after 1000 SC cycles of SC stress. The leakage current increases by orders of magnitude compare with the fresh DUT, which indicates that the gate oxide and the body diode suffer from catastrophic damage.

In order to trace the damage position, the C_g–V_g characteristics of the device after different SC stress cycles

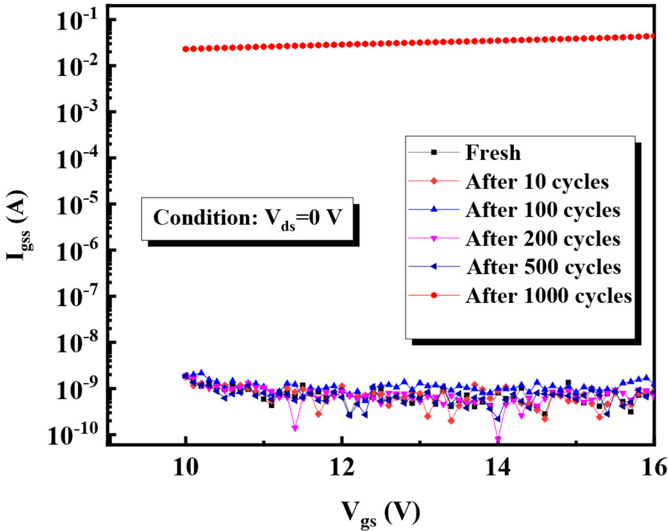

FIGURE 7. I_{gs}-V_{gs} characteristics of 1.2-kV 19-A SiC power MOSFETs with the increase of SC cycles.

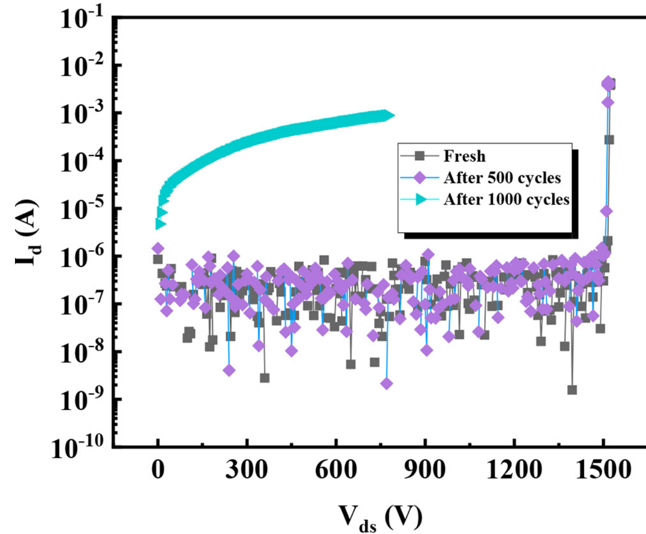

FIGURE 8. Blocking characteristics of the SiC power MOSFETs after SC stress.

are shown in Fig. 9 (due to the $I_{\rm gss}$ increases greatly by orders of magnitude the $C_{\rm g}$–$V_{\rm g}$ characteristics of the devicesafter 1000 SC cycles of SC stress cannot be measured). During the measurement, the gate was biased at a certain voltage while drain and source of the device are grounded. A 25 mV small AC voltage (V_{ac}) signal with 1 MHz frequency was added to the gate to detect $C_{\rm g}$. The $C_{\rm g}$–$V_{\rm g}$ curves of the device could be divided into five parts based on the value of $V_{\rm g}$. When the gate is strong positively biased, the channel is inversed and the JFET region is accumulated. With the decrease of $V_{\rm g}$, the channel turns out to deplete. Then the JFET region starts to deplete, when the channel is accumulated, the capacitance reaches the lowest value. Until the JFET region gets inversed, the whole capacitance increases again. The Five different surface situations of accumulation and depletion

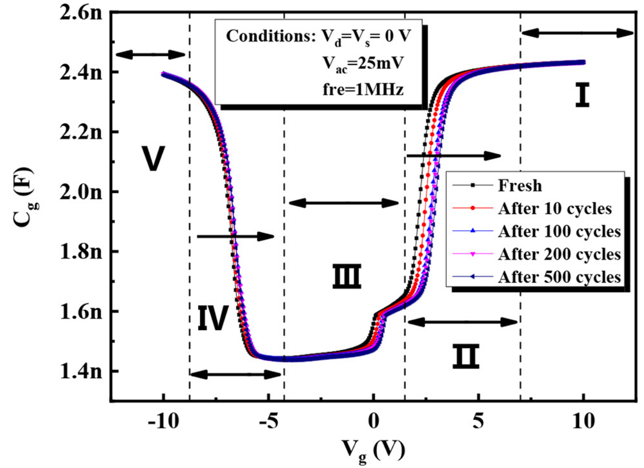

FIGURE 9. Variations of the C_g-V_g characteristic of the device under different SC cycles.

of JFET region and channel region are correspond to the five parts in Fig. 9. The $C_{\rm g}$ in part I, II, III and IV can respectively be expressed as [26]:

$$C_g = C_{oc} + C_{oj} = C_{ox} \tag{2}$$

where $C_{\rm oc}$ and $C_{\rm oj}$ represent for the oxide capacitances of the channel region and the JFET region, respectively.

$$C_g = \frac{1}{\frac{1}{C_{oc}} + \frac{1}{C_{dc}}} + C_{oj} \tag{3}$$

$$C_g = \frac{1}{\frac{1}{C_{oc}} + \frac{1}{C_{dc}}} + \frac{1}{\frac{1}{C_{oj}} + \frac{1}{C_{dj}}} \tag{4}$$

$$C_g = C_{oc} + \frac{1}{\frac{1}{C_{oj}} + \frac{1}{C_{dj}}} \tag{5}$$

where $C_{\rm dc}$ is the depletion capacitance of the channel region and C_{dj} is the depletion capacitance of the JFET region.

By the shifts of part I to part V in $C_{\rm g}$–$V_{\rm g}$ curve, the damage position and the types of the charges injected into the gate oxide can be obtained. From Fig. 9, there is obvious positive-shift on the part II while there is slight positive-shift on part III and part IV. This illustrates that during the repetitive SC cycles negative charges were injected into the gate oxide under channel region. However, the JFET region was slightly affected by stress. The results are consistent with the previous works [8].

B. EFFECT OF REPETITIVE SC STRESS ON LOW FREQUENCY NOISE

From the $C_{\rm g}$–$V_{\rm g}$ results mentioned above, the generated traps are mainly located in the gate oxide under channel region. LFN measurements are presented to be a valid method to characterization the defects and the density of interface states in channel region of semiconductor device. The spectral noise power density of the SiC power MOSFETs can be calculated based on the LFN results. According to the theory of 1/*f* noise, the 1/*f* noise is caused by random capture/release

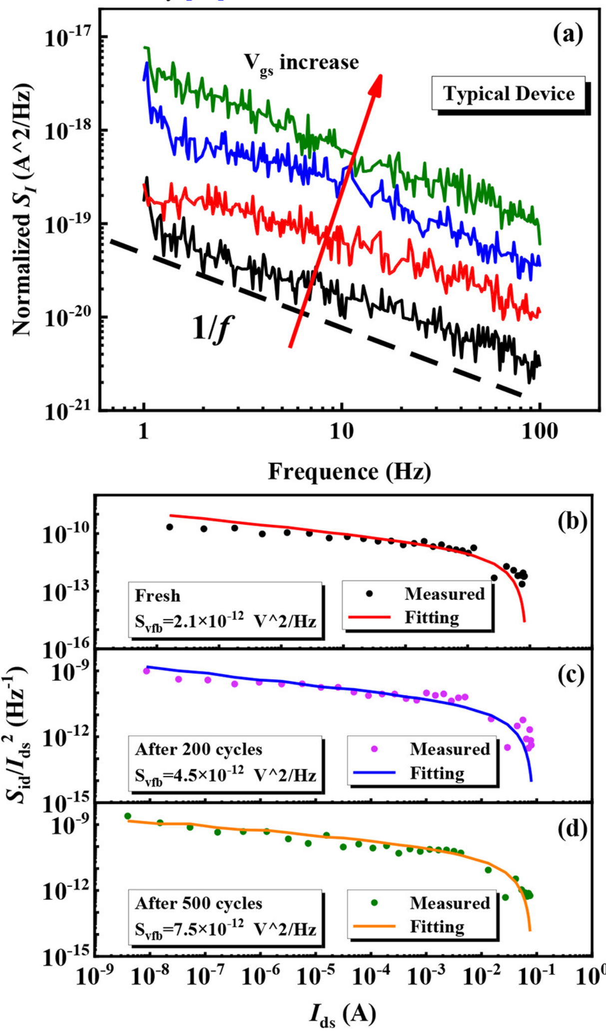

FIGURE 10. The characteristics of low frequency noise for SiC power MOSFETs: (a) the typical S_I/I^2 versus frequency for the fresh devices, and (b)-(d) the S_I/I^2 at 10 Hz versus I_{ds} for the fresh device, 200 and 500 SC cycles device, respectively.

of carriers by defects at the SiC/SiO2 interface. Therefore, according to the LFN characteristics before and after the SC stress of the device, the change in the density of defect states can be determined. To further explore the effect of SC stress on the defect in SiC power MOSFETs, the LFN power spectrum was measured under different gate bias voltages, and the current spectral noise density (S_I) was measured at low drain bias (V_{ds} = 100 mV) as shown in Fig. 10. The normalized S_I/I^2 is $1/f$ with the frequency in the range of 1 Hz to 100 Hz for the typical SiC power MOSFETs as shown in Fig. 10 (a). The normalized current spectral density S_I/I^2 taken at 10 Hz is plotted in Figs. 10 (b)-(d) versus the current of the fresh device, 200 and 500 SC cycles device, respectively. The number fluctuation model explains the $1/f$ noise by the charge trapping/detrapping of mobile carriers between interfacial traps and the channel, and the S_I/I^2 can be modeled by [27]:

$$S_I \Big/ I^2 = (g_m/I)^2 S_{vfb} \tag{6}$$

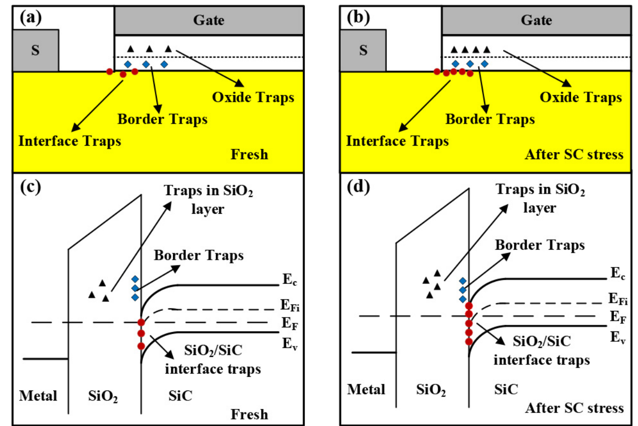

FIGURE 11. Schematic diagram of the physical mechanism for the effect of SC stress on SiC power MOSFETs: (a) traps at the SiC/SiO_2 of channel for the fresh device, (b) more traps for the device after the SC stress, (c) and (d) are corresponding to the energy band diagram of the device before and after SC stress, respectively.

where S_{vbf} as input-referred spectral noise density was adjusted here to achieve a good fit to the data, and g_m/I_d extracted from the measured characteristics. The S_{vfb} are 2.1×10^{-12}, 4.5×10^{-12} and 7.5×10^{-12} (V^2/Hz) for the fresh device, 200 and 500 SC cycles device, respectively. Then, it was possible to determine the density of traps (N_{it}) by:

$$S_{vfb} = q^2 kT\lambda N_{it} \Big/ WLfC_{ox}^2 \tag{7}$$

where λ is the tunneling attenuation coefficient (0.1 nm for SiO2), W and L are the gate width and length, respectively, and C_{ox} is the capacitance of SiO_2 per unit area. From the equation, as a first order estimate, the extracted N_{it} are 3.87×10^{17}, 8.28×10^{17} and 1.38×10^{18}cm^{-3}eV^{-1} for the fresh device, 200 and 500 SC cycles device, respectively.

C. MECHANISM OF SC STRESS ON SIC MOSFETS

To explain the degradation mechanism, the schematic diagram of the physical mechanism is shown in Fig. 11. The fresh device schematic diagram and energy band diagram are shown in Fig. 11 (a). At the near-interfacial SiC/SiO_2 of the fresh SiC power MOSFETs, defects generally can be grouped into three kinds: bulk oxide traps, interface traps, and border traps [14]. Carbon vacancy clusters in the near-interfacial SiO_2/SiC (interface traps) are the most common defect responsible for $1/f$ noise [28], they are located at shallow levels [29], and it is often believed that the SiC/SiO2 interface contains excess carbaon [30], [31]. Furthermore, the incompletely ionized N dopants from postoxidation NO processing could also result in fluctuations in carrier number [32], [33]. Therefore, these traps of the fresh devices could be detected by the LFN method as shown in Fig. 10 (b).

The schematic diagram and energy band diagram of the SC degraded devices are shown in Fig. 11 (b). As for the SiC power MOSFETs during SC stress, the channel region is suffered from a peak ionization rate and perpendicular electrical

field [34]. Meanwhile, high temperature also accumulation at the SiC/SiO_2 interface of the SiC power MOSFETs [35]. During SC stress, the bond of Si-C could be broken, and addition carbon vacancies could be generated. Furthermore, the Si=N bonds also broken. Thus, active traps would be formed. The results in the increase of defect, which is supported by the extracted N_{it} results as shown in Fig. 10 (b)-(d). Moreover, the negative charges tunnel directly into the intrinsic and the near-interfacial oxide traps could be activated [36], [37], and this leads to the I_{ds} decrease and positive shift of V_{th} as shown in Fig. 4 and Fig. 6.

IV. CONCLUSION

The degradation behavior and mechanisms of SiC power MOSFETs under repetitive SC stress were investigated. The repetitive SC stress leads to the degradation of the devices, such as the significantly increase of the R_{on} and V_{th}. Besides, the I_{gss} increase greatly and blocking characteristics of the SiC power MOSFET were deteriorated after 1000 cycles of SC stress. Moreover, C_g-V_g curves and LFN characteristics before and after SC stress were measured. The damage region was confirmed on channel region along the SiC/SiO_2 interface by the positive shift of C_g-V_g curves. Based on the LFN results, the trap density of SiC/SiO_2 interface and oxide layer gradually increase after repetitive SC stress. Due to the peak ionization rate, the perpendicular electrical field and high temperature on the channel region of gate oxide during SC stress, the physical mechanism could be attributed to electrically active traps generated at SiC/SiO_2 interface and in the oxide layer. The results of this study may be useful to provide reference for converters design and fault protection of SiC power MOSFETs.

REFERENCES

[1] M. Berkani, S. Lefebvre, and Z. Khatir, "Saturation current and on-resistance correlation during repetitive short-circuit conditions on SiC JFET transistors," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 621–624, Feb. 2013, doi: 10.1109/TPEL.2012.2215629.

[2] J. H. Sun, H. Y. Xu, X. K. Wu, S. Yang, Q. Guo, and K. Sheng, "Short circuit capability and high temperature channel mobility of SiC MOSFETs," in *Proc. Int. Symp. Power Semicond. Devices*, Sapporo, Japan, Jul. 2017, pp. 399–402, doi: 10.23919/ISPSD.2017.7988988.

[3] J. X. Wei, S. Y. Liu, J. Fang, S. Li, T. Li, and W. F. Sun, "Investigation on degradation mechanism and optimization for SiC power MOSFETs under long-term short-circuit stress," in *Proc. IEEE 30th Int. Symp. Power Semicond. Devices ICs*, Chicago, IL, USA, Jun. 2018, pp. 399–402, doi: 10.1109/ISPSD.2018.8393687.

[4] C. Abbate, G. Busatto, and F. Iannuzzo, "Unclamped repetitive stress on 1200 V normally-off SiC JFETs," *Microelectron. Rel.*, vol. 52, nos. 9–10, pp. 2420–2425, Oct. 2012, doi: 10.1016/j.microrel.2012.06.097.

[5] J. Spitz, M. R. Melloch, J. A. Cooper, and M. A. Capano, "2.6 kV 4H-SiC lateral DMOSFETs," *IEEE Electron Device Lett.*, vol. 19, no. 4, pp. 100–102, Apr. 1998, doi: 10.1109/55.663527.

[6] A. K. Agarwal, S. Seshadri, and L. B. Rowland, "Temperature dependence of Fowler–Nordheim current in 6H- and 4H-SiC MOS capacitors," *IEEE Electron Device Lett.*, vol. 18, no. 12, pp. 592–594, Dec. 1997, doi: 10.1109/55.644081.

[7] M. Trivedi and K. Shenai, "Failure mechanisms of IGBTs under short-circuit and clamped inductive switching stress," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 108–116, Jan. 1999, doi: 10.1109/63.737598.

[8] J. X. Wei *et al.*, "Comprehensive analysis of electrical parameters degradations for SiC power MOSFETs under repetitive short-circuit stress," *IEEE Trans. Electron Devices*, vol. 65, no. 12, pp. 5440–5447, Dec. 2018, doi: 10.1109/TED.2018.2873672.

[9] D. Othman, S. Lefebvre, M. Berkani, Z. Khatir, A. Ibrahim, and A. Bouzourene, "Robustness of 1.2 kV SiC MOSFET devices," *Microelectron. Rel.*, vol. 53, nos. 9–11, pp. 1735–1738, Sep. 2013, doi: 10.1016/j.microrel.2013.07.072.

[10] M. Riccio, A. Castellazzi, G. D. Falco, and A. Irace, "Experiment alanalysis of electro-thermal instability in SiC power MOSFETs," *Microelectron. Rel.*, vol. 53, nos. 9–11, pp. 1739–1744, Sep./Nov. 2013, doi: 10.1016/j.microrel.2013.07.014.

[11] E.-P. Eni *et al.*, "Short-circuit degradation of 10-kV 10-A SiC MOSFET," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9342–9345, Dec. 2017, doi: 10.1109/TPEL.2017.2657754.

[12] Z. Q. Wang *et al.*, "Temperature-dependent short-circuit capability of silicon carbide power MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1555–1566, Feb. 2016, doi: 10.1109/TPEL.2015.2416358.

[13] T.-T. Nguyen, A. Ahmed, T. V. Thang, and J.-H. Park, "Gate oxide reliability issues of SiC MOSFETs under short-circuit operation," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2445–2455, May 2015, doi: 10.1109/TPEL.2014.2353417.

[14] L. K. J. Vandamme, "Noise as a diagnostic tool for quality and reliability of electronic devices," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 2176–2187, Nov. 1994, doi: 10.1109/16.333839.

[15] D. M. Fleetwood, "1/*f* noise and defects in microelectronic materials and devices," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 4, pp. 1462–1486, Aug. 2015, doi: 10.1109/TNS.2015.2405852.

[16] Y. Liu, H. Y. He, R. S. Chen, Y.-F. En, B. Li, and Y.-Q. Chen, "Analysis and simulation of low-frequency noise in indium-zinc-oxide thin-film transistors," *IEEE J. Electron Devices Soc.*, vol. 6, no. 1, pp. 271–279, Jan. 2018, doi: 10.1109/JEDS.2018.2800049.

[17] M. von Haartman and M. Östling, *Low-Frequency Noise in Advanced MOS Devices*. Dordrecht, The Netherlands: Springer, 2007, doi: 10.1007/978-1-4020-5910-0.

[18] C. X. Zhang *et al.*, "Temperature dependence and postirradiation annealing response of the 1/f noise of 4H-SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 6, no. 7, pp. 2361–2367, Jul. 2013, doi: 10.1109/TED.2013.2263426.

[19] J. W. Palmour, M. E. Levinshtein, S. L. Rumyantsev, and G. S. Simin, "Low frequency noise in 4H-silicon carbide junction field effect transistors," *Appl. Phys. Lett.*, vol. 68, no. 19, pp. 2669–2671, May 1996, doi: 10.1063/1.116276.

[20] S. L. Rumyantsev *et al.*, "Si-like low-frequency noise characteristics of 4H-SiC MOSFETs," *Semicond. Sci. Technol.*, vol. 26, no. 8, Aug. 2011, Art. no. 085015, doi: 10.4028/www.scientific.net/MSF.717-720.1105.

[21] M. E. Levinshtein and S. L. Rumyantsev, "Low frequency noise in 4H silicon carbide," *J. Appl. Phys.*, vol. 81, no. 4, pp. 1757–1763, Feb. 1997, doi: 10.1063/1.364007.

[22] J. B. Casady, W. Dillard, R. W. Johnson, A. K. Agarwal, R. R. Siergiej, and W. E. Wagner, "Low frequency noise in 6H-SiC MOSFETs," *IEEE Electron Device Lett.*, vol. 16, no. 6, pp. 274–276, Jun. 1995, doi: 10.1109/55.790733.

[23] S. L. Rumyantsev *et al.*, "Low frequency noise in 4H-SiC metal oxide semiconductor field effect transistors," *J. Appl. Phys.*, vol. 104, no. 9, pp. 1–6, Nov. 2008, doi: 10.1063/1.3009664.

[24] A. Castellazzi, T. Funaki, T. Kimoto, and T. Hikihara, "Short-circuit tests on SiC power MOSFETs," in *Proc. Int. Conf. Power Electron. Drive Syst.*, Kitakyushu, Japan, Apr. 2013, pp. 1297–1300, doi: 10.1109/PEDS.2013.6527219.

[25] S. Chen, C. Cai, T. Wang, Q. Guo, and K. Sheng, "Cryogenic and high temperature performance of 4H-SiC power MOSFETs," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Long Beach, CA, USA, May 2013, pp. 207–210, doi: 10.1109/APEC.2013.6520209.

[26] J. X. Wei *et al.*, "Interfacial damage extraction method for SiC power MOSFETs based on C-V characteristics," in *Proc. Int. Symp. Power Semicond. Devices*, Sapporo, Japan, Jul. 2017, pp. 359–362, doi: 10.23919/ISPSD.2017.7988992.

[27] Y. Q. Chen *et al.*, "Effect of hydrogen on defects of AlGaN/GaN HEMTs characterized by low-frequency noise," *IEEE Trans. Electron Devices*, vol. 65, no. 4, pp. 1321–1326, Apr. 2018, doi: 10.1109/TED.2018.2803443.

[28] C. X. Zhang *et al.*, "Origins of low-frequency noise and interface traps in 4H-SiC MOSFETs," *IEEE Electron Device Lett.*, vol. 34, no. 1, pp. 117–119, Jan. 2013, doi: 10.1109/LED.2012.2228161.

[29] D. M. Fleetwood, T. L. Meisenheimer, and J. H. Scofield, "1/*f* noise and radiation effects in MOS devices," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 1953–1964, Nov. 1994, doi: 10.1109/16.333811.

[30] V. V. Afanas'ev, "Electronic properties of SiO_2/SiC interface," *Microelectron. Eng.*, vol. 48, nos. 1–4, pp. 241–248, Sep. 1999.

[31] S. Wang *et al.*, "Bonding at the SiC-SiO_2 interface and the effects of nitrogen and hydrogen," *Phys. Rev. Lett.*, vol. 98, no. 2, pp. 1–4, Jan. 2007.

[32] A. Carlo and B. Vincenzo, "Toward reliable density functional methods without adjustable parameters: The PBE0 model," *J. Chem. Phys.*, vol. 110, no. 13, pp. 6158–6170, Apr. 1999, doi: 10.1063/1.478522.

[33] A. Chatterjee, K. Matocha, V. Tilak, J. A. Fronheiser, and H. Piao, "Multiscale modeling and analysis of the nitridation effect of SiC/SiO_2 interface," *Mater. Sci. Forum SiC Rel. Mater.*, vols. 645–648, pp. 479–482, Apr. 2009, doi: 10.4028/www.scientific.net/MSF.645-648.479.

[34] X. T. Zhou. H. Y. Su, Y. Wang, R. F. Yue, G. Dai, and J. T. Li, "Investigations on the degradation of 1.2-kV 4H-SiC MOSFETs under repetitive short-circuit tests," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4346–4351, Nov. 2016, doi: 10.1109/TED.2016.2606882.

[35] J. A. Schrock *et al.*, "Failure analysis of 1200-V/150-A SiC MOSFET under repetitive pulsed overcurrent conditions," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1816–1821, Mar. 2016, doi: 10.1109/TPEL.2015.2464780.

[36] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "Basic mechanisms of threshold-voltage instability and implications for reliability testing of SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 316–323, Feb. 2015, doi: 10.1109/TED.2014.2356172.

[37] H. Yano, N. Kanafuji, A. Osawa, T. Hatayama, and T. Fuyuki, "Threshold voltage instability in 4H-SiC MOSFETs with phosphorus-doped and nitrided gate oxides," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 324–332, Feb. 2015, doi: 10.1109/TED.2014.2358260.