Received 1 December 2019; revised 11 January 2020; accepted 27 January 2020. Date of publication 30 January 2020; date of current version 19 February 2020.
The review of this article was arranged by Editor M. Liu.

Digital Object Identifier 10.1109/JEDS.2020.2970450

Analysis and Optimization of Threshold Voltage Variability by Polysilicon Grain Size Simulation in 3D NAND Flash Memory

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This work was supported in part by the National Key Research and Development Program of China under Grant 2018YFB1107700, and in part by the National Science and Technology Major Project of China under Grant 2017ZX02301002.

ABSTRACT The impact of linear correlation between lognormal distribution grain size mean and sigma along the polysilicon channel on threshold voltage (V_{th}) variability has been investigated in three dimensional (3D) NAND flash. The variety of grain size mean and sigma results in the unstable V_{th} variability. To obtain a stable V_{th} distribution with various grain size mean, the grain size mean dependent V_{th} variability sensitivity to the grain size sigma was used to optimize the linear correlation between grain size mean and sigma via TCAD simulation. The optimized linear correlation with stable V_{th} variability is obtained except for the "unbalance region" affected by the combination of grain boundaries and positions with these grain size mean and sigma values resulting in the slightly shrinking V_{th} variability. Our results strongly suggest that this approach could guide the direction of polysilicon crystallization optimization to obtain stable V_{th} distribution with the predicted linear correlation between grain size mean and sigma.

INDEX TERMS Lognormal distribution, 3D NAND, polysilicon channel, grain size.

I. INTRODUCTION

Three dimensional NAND (3D NAND) is the preferred solution combing device performance and high capacity storage to replace planar NAND flash memory [1]–[3]. To achieve further scaling and increase the density in 3D NAND Flash, more layers were stacked, while polysilicon as the material for the device channel leading to severe challenges and constraints. Polysilicon channel exhibits critical issues such as low effective channel mobility and threshold voltage (V_{th}) instability, caused by the existence of the grain boundary (GB) traps [4]. Although solutions with alternative channel materials were proposed, it is costly and immature to implement [5]–[7]. Therefore, it is critical to improving the device performance and variability by polysilicon channel engineering for 3D NAND flash memory. A promising approach to improve device performance and variability is polysilicon grain size engineering [8], [9]. Most studies were concerned about optimizing the average grain size, larger grain shows larger channel current as less GB traps, while larger grains with higher chance to have different grain condition in polysilicon channel lead to more variability [10]. Different grain size mean leads to different grain size sigma. Furthermore, there is limited insight focusing on the correlation between grain size mean and sigma in 3D NAND flash memory.

In this work, we found that a robust linear correlation between grain size mean and sigma in the vertical channel with lognormal grain size distribution. The impact of this linear correlation on V_{th} variability was investigated by TCAD simulation. The V_{th} variability sensitivity to the grain size sigma at each grain size mean was extracted and used to optimize the linear correlation between grain size mean and sigma to target V_{th} variability with better device performance and stable V_{th} distribution.

II. EXPERIMENTS AND SIMULATION

In our work, the experiment is based on charge trapping 3D vertical channel NAND flash test chips [11]. Fig. 1(a) shows

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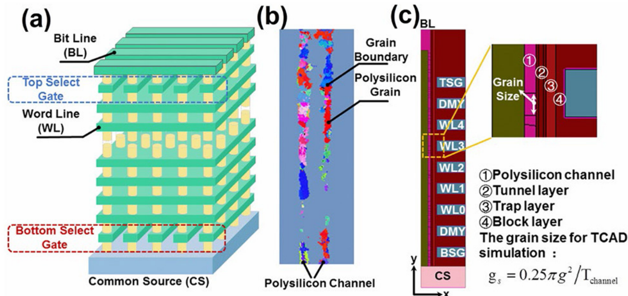

FIGURE 1. (a) Schematic diagram of 3D NAND flash structure. (b)The grains and grain boundaries are shown in the polysilicon channel structure observed by the planar TEM and PED technique. (c) The TCAD simulation structure, the gate stack consists of tunnel layer, trap layer and block layer, respectively.

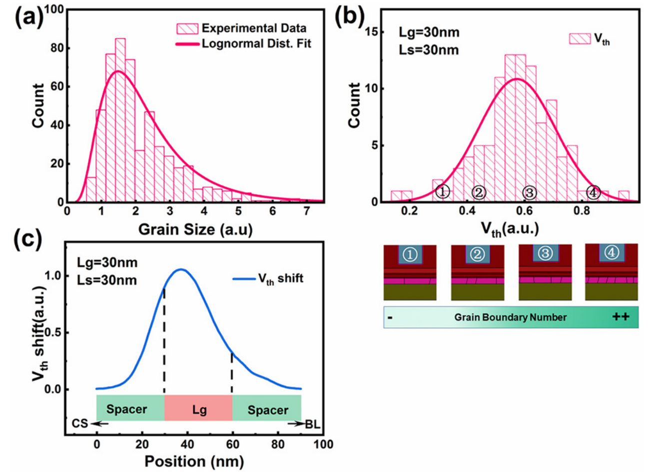

FIGURE 2. (a) The typical trend of polysilicon grain size distribution in vertical channel 3D NAND flash, observed by planar TEM and PED technique. The solid line represents the fit of the lognormal distribution of (1) to experimental data. (b) Distribution of V_{th} for lognormal grain size distribution by TCAD. (c) The V_{th} shift due to single GB at different channel positions in the initial state.

the schematic of the 3D NAND flash structure. The tested 3D NAND strings are composed of top select gate transistor (TSG), bottom select gate transistor (BSG), dummy cell (DMY), and memory cells (WL0∼WLn) along a channel hole. Grains and grain boundaries are shown in Fig. 1(b), observed by planar transmission electron microscopy (TEM) and precession electron diffraction (PED) technique. The equivalent grain size g of a grain relates to grain area A by $g = 2\sqrt{A/\pi}$. Sentaurus Sdevice simulator is used for simulation. The simulation structure of this device is shown in Fig. 1(c). The grain size for TCAD simulation $g_s = 0.25\pi g^2/T_{channel}$ is defined in the vertical direction since the grain size is larger than the channel thickness ($T_{channel}$) [12]. Furthermore, the drift-diffusion model, coulomb scattering mobility model, thermionic emission, and Shockley-Read-Hall recombination model are introduced in the polysilicon channel [13]. Other main simulation parameters are referenced in our previous work [14]. The GBs are created randomly with a lognormal grain size distribution defined by a grain size mean and sigma in polysilicon channel. Similarly, the GB angle is generated with a uniform random distribution within a given range. 100 simulation samples are used for each lognormal grain size distribution. The energy density of state of the GB interface trap used in this simulation is obtained by fitting the experimental data [14].

III. RESULTS AND DISCUSSION

A. THE IMPACT OF POLYSILICON GRAIN SIZE DISTRIBUTION

Fig. 2(a) shows the trend of polysilicon grain size distribution in vertical channel 3D NAND flash, observed by TEM and PED technique. This distribution is well approximated by the lognormal distribution [15]

$$f(\mathrm{g}) = \frac{1}{g\sigma_N\sqrt{2\pi}}\exp\left(-\frac{(\ln g - \mu_N)^2}{2\sigma_N^2}\right) \tag{1}$$

$$\mu_L = \exp\left(\mu_N + \frac{\sigma_N^2}{2}\right) \tag{2}$$

$$\sigma_L = \left[\left(\exp\left(\sigma_N^2\right) - 1\right)\exp\left(2\mu_N + \sigma_N^2\right)\right]^{1/2} \tag{3}$$

where μ_N and σ_N are the normal distribution mean and sigma in log scale, respectively. μ_L and σ_L are the lognormal distribution mean and sigma, respectively.

The occurrence of such lognormal grain size distribution in the vertical channel is mainly coming from the polysilicon crystallization mechanism [15]. Fig. 2(b) shows the impact of lognormal grain size distribution on cell V_{th} distribution by TCAD simulation with the same gate length (Lg) and spacer length (Ls). When the grain size is much smaller than Lg, it shows a larger V_{th} as the GB number increases. In this case, the V_{th} variability is mainly coming from the different number of GBs inside each cell. However, when the grain size increases, the V_{th} decreases as the GB number decrease under the Lg. The impact of the actual positions of these GBs should not be ignored. Fig. 2(c) shows the simulation of the V_{th} shift as a function of GB positions perpendicular to the memory string under the initial state. The GB creates a different height potential barrier with a different position. It needs a different gate bias to reduce the barrier that leads to different V_{th} [16]. Therefore, both the GBs number and the position of GBs serve as the V_{th} variability sources.

B. THE IMPACT OF THE CORRELATION BETWEEN GRAIN SIZE MEAN AND SIGMA IN VERTICAL CHANNEL

Fig. 3(a) shows the correlation between grain size mean and sigma of lognormal grain size distribution with the same polysilicon crystallization thermal process, observed by TEM and PED technique. A robust linear correlation is observed between grain size mean and sigma. The larger grain size mean relates a larger grain size sigma, indicating that larger grain size mean has more chance to have different grain conditions. The normalized value of grain size sigma to grain size mean is almost the same under the current polysilicon crystallization process. The occurrence of such correlation

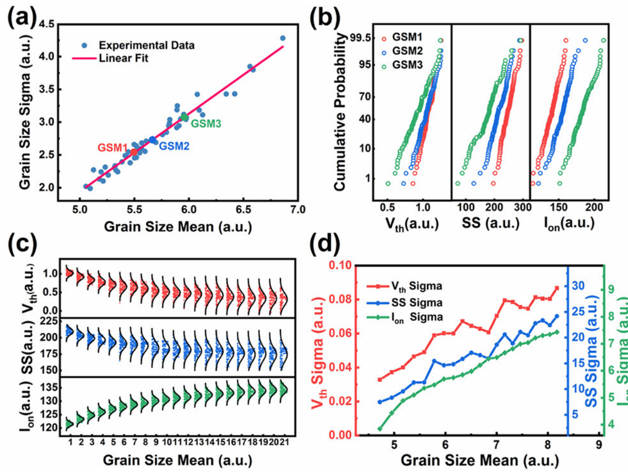

FIGURE 3. (a) The correlation between grain size mean and sigma. (b) V_{th}, SS, and I_{on} distribution measured on the polysilicon channel with different grain size distribution. GSM1 (grain size mean) < GSM2 < GSM3. (c) The TCAD simulation V_{th}, SS, and I_{on} distribution of devices with different grain size mean and sigma based on the correlation of Fig. 3(a). (d) The TCAD simulation V_{th}, SS and I_{on} distribution sigma extract from Fig. 3(c).

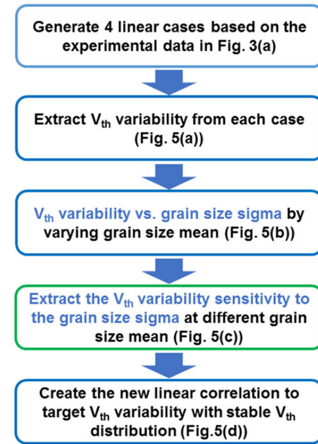

FIGURE 4. The flow chart for creating the new linear correlation of grain size mean and sigma.

is mainly due to the polysilicon crystallization conditions in 3D NAND Flash. The V_{th}, subthreshold swing (SS), and on-state current (I_{on}) statistical distribution measured on the polysilicon channel with different grain size distribution were extracted at room temperature, as shown in Fig. 3(b). It can be seen that larger grain size mean shows broaden distribution but have better performance. There is a trade-off between device performance and variability. Furthermore, we performed the device simulation using TCAD to investigate the impact of this linear correlation of grain size mean and sigma with the same polysilicon channel thickness. Fig. 3(c) shows the V_{th}, SS, and I_{on} distribution of devices with different grain size mean and sigma based on the linear correlation of Fig. 3(a). The device V_{th}, SS, and I_{on} performance improved as grain size mean increasing, while variability getting worse. This is comparable to the experimental data. Furthermore, the normalized value of grain size sigma to grain size mean is almost the same, while it leads to different V_{th}, SS and I_{on} distribution variability under various range of grain size mean, as shown in Fig. 3(d). The device V_{th} variability mainly comes from the grain conditions in the polysilicon channel. In this case, the impact of grain conditions on V_{th} variability is inconsistent under different grain size mean.

C. THE LINEAR CORRELATION BETWEEN GRAIN SIZE MEAN AND SIGMA OPTIMIZATION BY TCAD

The polysilicon channel grain size mean values in a large amount of vertical 3D NAND flash devices are within a specific range. Meanwhile, the linear correlation between grain size mean and sigma results in different V_{th} distribution variability. To obtain a tighten and stable V_{th} distribution, optimizing the linear correlation of grain size mean and sigma would be the fundamental solution in grain size engineering. An optimization approach is proposed to adjust the linear correlation of grain size mean and sigma with stable V_{th} distribution by TCAD, as shown in Fig. 4. The V_{th} variability sensitivity to the grain size sigma at each grain size mean was the focus of optimizing the linear correlation between grain size mean and sigma to target V_{th} variability. This approach can be explained as follows. Basing on the experimental linear correlation (Case1), another four linear correlation cases (Case2-5) were proposed for TCAD simulation. Then, the V_{th} variability was extracted from each case, as shown in Fig. 5(a). Fig. 5(b) indicates that the V_{th} variability trends up as grain size sigma increasing at the same grain size mean. The normalized value of grain size sigma to grain size mean leading to a fixed impact on V_{th} variability at same grain size mean. However, with grain size mean increasing, the effect of the normalized value of grain size sigma to grain size mean on V_{th} variability is getting weak. This is due to larger grain size mean with a higher chance to have more different grain conditions in polysilicon channel, leading to less impact of grain conditions on V_{th} variability sensitivity. The V_{th} variability sensitivity to the grain size sigma is strongly dependent on the grain size mean. Linear correlation is observed, as shown in Fig. 5(c). Then the V_{th} variability sensitivity to the grain size sigma can be used to optimize the linear correlation between grain size mean and sigma to target V_{th} variability. As illustrated in Fig. 5(d), we have successfully developed an approach creating the new linear correlation of grain size mean and sigma with V_{th} variability $\sim$ 60. Fig. 5(e) shows the V_{th}, SS, and I_{on} distribution of TCAD simulation with the new linear correlation of Fig. 5(d). The device performance improved as grain size mean increasing, while the device performance distributions are almost stable. It was expected that the new linear correlation with stable V_{th} variability could be obtained by optimizing the current polysilicon crystallization process.

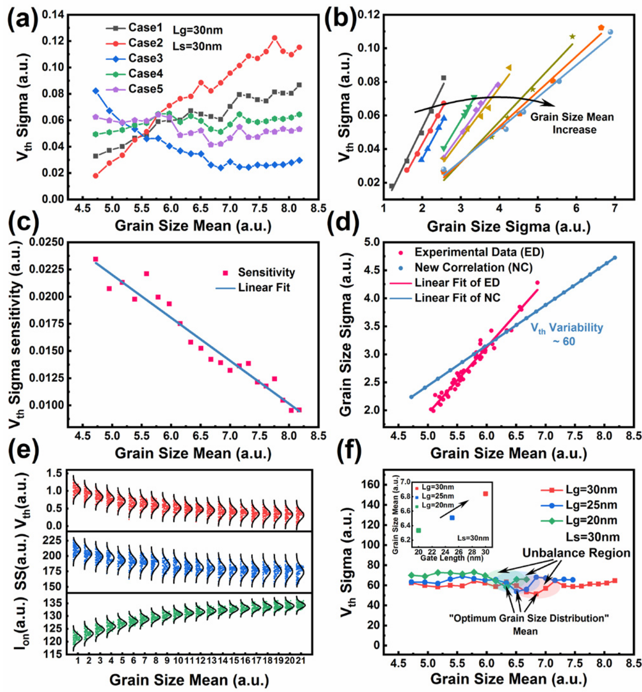

FIGURE 5. **(a) Case1 (based on the experimental data), Case2-5 were proposed for TCAD simulation. (b) The correlation between V_{th} variability and grain size sigma at different grain size mean. (c) The correlation between V_{th} variability sensitivity and grain size mean for simulated data (Fig. 5(b)) was extracted. Linear correlation is observed between V_{th} sensitivity and grain size mean. (d) The new linear correlation of grain size mean and sigma. (e) The V_{th}, SS, and I_{on} distribution of TCAD simulation with the new linear correlation. (f) Varying the gate length from 30nm to 20nm, the minimum V_{th} variability shifts to smaller grain size mean with gate length shrinks. Inset shows the minimum V_{th} variability is strongly dependent on the physical dimension of the gate length.**

An interesting phenomenon is observed, there is a region where the V_{th} variability trends down firstly and then trends up slightly shown in Fig. 5(f). It is the grain size mean and sigma with the combination of GB number and position that leading an unbalance region. Meanwhile, different grain size with the various GB position might result in the same V_{th}. As shown in Fig. 6(b), with the increasing of grain size mean and sigma, the number of grain sizes in different grain size ranges will change. The number of grain sizes leading to the same small range of V_{th} will increase firstly and then decreases. Its maximum value might appear at the point of the grain size mean and sigma with the minimum V_{th} variability in this optimized linear correlation, which leads to the tightest V_{th} distribution, as shown in Fig. 6(c). Therefore, this point in the optimized linear correlation is defined as the "optimum grain size distribution", as shown in Fig. 5(f). It can be explained that the better combination of GB number and position with this grain size mean and sigma leads to tightest V_{th} distribution. Moreover, the minimum V_{th} variability is strongly dependent on the physical dimension of the gate, as shown in the inset of Fig. 5(f). These grain sizes leading to the same small range of V_{th} are strongly gate length dependent. Therefore, the unbalance region is

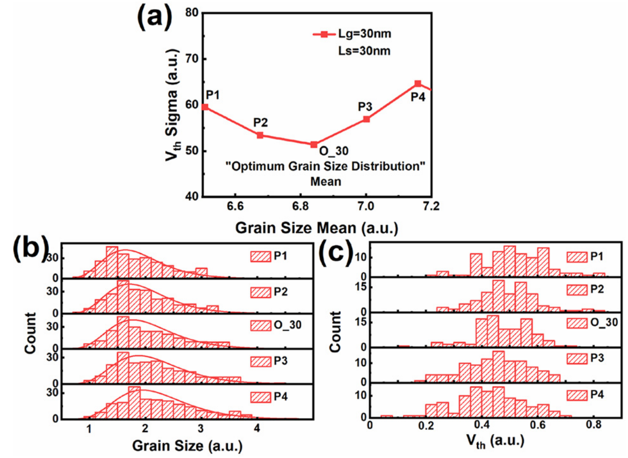

FIGURE 6. **(a) The correlation between V_{th} variability and grain size mean in the unbalance region with Lg=30nm and Ls=30nm. O_30 is the point with "optimum grain size distribution". P1, P2, P3 and P4 are the 4 points in the unbalance region. (b) The lognormal grain size distribution of different points in the unbalance region of Fig. 6(a). (c) The V_{th} distribution of TCAD simulation with the new linear correlation in unbalance region.**

different for the different Lg, and thus smaller Lg shows smaller "optimum grain size distribution" mean. Therefore, to obtain the stable V_{th} distribution, the grain size mean values smaller than the unbalance region will be the better choice considering that it has more stable V_{th} distribution and is unaffected by the "optimum grain size distribution", also suitable for more layers stacking with smaller Lg. This work provides an approach to predict the linear correlation between grain size mean and sigma with target V_{th} variability efficiently, which could be used for guiding the direction of polysilicon crystallization optimization to obtain better device performance and stable V_{th} distribution.

IV. CONCLUSION

In this work, we have investigated the impact of the linear correlation between grain size mean and sigma with log-normal grain size distribution on V_{th} variability in vertical channel 3D NAND flash. The normalized value of grain size sigma to grain size mean is almost the same in the linear correlation, while the impact of grain conditions with different grain size sigma on device V_{th} variability is inconsistent under different grain size mean. The V_{th} variability sensitivity to the grain size sigma at each grain size mean was the focus of our approach to optimize the linear correlation between grain size mean and sigma to target V_{th} variability. The stable V_{th} distribution was obtained with the extracted V_{th} variability sensitivity except for the "unbalance region" affected by the combines that grain boundaries and positions with these grain size mean and sigma values, resulting in the slightly shrinking V_{th} variability. This approach predicted the linear correlation between grain size mean and sigma efficiently, which could be used for obtaining better device performance and stable V_{th} distribution, and for guiding the direction of polysilicon crystallization process optimization.

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