Received 12 November 2019; revised 3 January 2020; accepted 16 January 2020. Date of publication 20 January 2020; date of current version 13 February 2020.
The review of this article was arranged by Editor Z. Zhang.

Digital Object Identifier 10.1109/JEDS.2020.2967897

$1/f^{\gamma}$ Low Frequency Noise Model for Buried Channel MOSFET

SHI SHEN (Student Member, IEEE), AND JIE YUAN (Senior Member, IEEE)

Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong

CORRESPONDING AUTHOR: S. SHEN (e-mail: sshen@connect.ust.hk)

This work was supported by RGC General Research Fund sponsored by the Research Grants Council of Hong Kong under Grant GRF 16206215.

ABSTRACT The Low Frequency Noise (LFN) in MOSFETs is critical to Signal-to-Noise Ratio (SNR) demanding circuits. Buried Channel (BC) MOSFETs are commonly used as the source-follower transistors for CCDs and CMOS image sensors (CIS) for lower LFN. It is essential to understand the BC MOSFETs noise mechanism based on trap parameters with different transistor biasing conditions. In this paper, we have designed and fabricated deep BC MOSFETs in a CIS-compatible process with 5 V rating. The $1/f^{\gamma}$ LFN is found due to non-uniform space and energy distributed oxide traps. To comprehensively explain the BC MOSFETs noise spectrum, we developed a LFN model based on the Shockley–Read–Hall (SRH) theory with WKB tunneling approximation. This is the first time that the $1/f^{\gamma}$ LFN spectrum of BC MOSFET has been numerically analyzed and modeled. The Random Telegraph Signal (RTS) amplitudes of each oxide traps are extracted efficiently with an Impedance Field Method (IFM). Our new model counts the noise contribution from each discretized oxide trap in oxide mesh grids. Experiments verify that the new model matches well the noise power spectrum from 10 to 10k Hz with various gate biasing conditions from accumulation to weak inversion.

INDEX TERMS Low frequency noise (LFN), buried channel (BC) MOSFET, oxide trap, random telegram signal (RTS), impedance field method (IFM).

I. INTRODUCTION

CMOS technology scaling enables high density IC integration and fast transistor operation. However, it brings rising concern about Low Frequency Noise (LFN) for the circuits such as CMOS image sensors (CIS) and memory cells which are demanding of Signal-to-Noise Ratio (SNR) and reliability [1], [2]. It is well known that LFN results from the cumulative effect of a large number of traps that distributed inside the MOSFET oxide or at the silicon-oxide interface [3]. The drain current fluctuation amplitude due to the trapping/de-trapping event from a single oxide trap increases with the shrinking device geometry [4]. For MOSFETs with a small channel area, it is possible to observe the Random Telegram Signal (RTS) noise, which is a particular type of LFN due to only a single dominant oxide trap [5]. Buried Channel (BC) MOSFETs are widely known to have lower LFN than normal Surface Channel (SC) MOSFETs due to the reduced interaction between channel carriers and the silicon-oxide interface [6]. With a negative gate-to-source voltage, the conducting channel is buried deeply from the interface by a vertical suppressing electrical field. Thus the possibility for channel carriers to get trapped by the oxide defects is reduced. It is commonly seen that BC MOSFETs are used as source followers for CCD and CMOS image sensors [2], [7].

It is essential to understand the LFN noise mechanism in BC MOSFETs. In [8], BC MOSFET was integrated with a CIS system for performance evaluation. The noise spectrum of the BC MOSFETs were measured without further numerical analysis. A BC FinFET based CIS scheme with reduced readout noise was developed in [9]. But only simulation was presented. The fabrication of BC MOSFETs in a CIS compatible process was reported in [6], and the noise characterization was performed on a single BC MOSFET with small channel. However, the results are not statistically representative since MOSFETs with small channel area have large variation in noise [10]. A compact statistical LFN model for BC MOSFETs along with experimental

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see http://creativecommons.org/licenses/by/4.0/

results was presented in [11]. The model is useful for circuit simulation. However, compact statistical noise model cannot explain noise contribution from traps since only empirical curve fitting was adopted similar to [12] and [13]. To gain a better understanding from a microscopic view, [4] developed an LFN simulator for SC MOSFETs that counts the noise contribution from discretized traps. However, in experimental validation, the Power Spectrum Density (PSD) results were shown only at 1k Hz without analysis on different biasing conditions, and the traps were assumed uniformly distributed in space and energy level. In reality, the traps are not uniformly distributed within energy and space, which results in $1/f^{\gamma}$ noise behavior rather than $1/f$ [14], [15]. As reported from [8], the measured LFN slope γ was 0.68 from the BC MOSFET noise spectrum. Thus there is a need for a numerical method to model the $1/f^{\gamma}$ behavior for BC MOSFETs with experimental validation that is statistically representative.

In this work, we introduce an LFN model based on the Shockley–Read–Hall (SRH) theory with WKB tunneling approximation. To the best of our knowledge, this is the first time that $1/f^{\gamma}$ noise has been analyzed and modeled for BC MOSFETs at various gate biasing conditions. This model is experimentally validated with BC MOSFETs fabricated in a 5V CIS compatible process.

The remaining of this paper is organized as follows: In Section II, the new LFN model is explained. The device description, characterization, experimental validation and discussion are provided in Section III.

II. LOW FREQUENCY NOISE MODEL

Based on the RTS noise theory [16], the MOSFET drain current noise spectrum contributed by a single oxide trap can be expressed by

$$S_{ID,i} = \frac{4\left(\alpha \cdot I_{RTS,i}\right)^2}{\left(\tau_{c,i} + \tau_{e,i}\right)\left[\left(\tau_{c,i}^{-1} + \tau_{e,i}^{-1}\right)^2 + (2\pi f)^2\right]} \quad (1)$$

where $I_{RTS,i}$ is the RTS current amplitude, $\tau_{c,i}$ is the trap capture time constant, $\tau_{e,i}$ is the trap emission time constant, f is the frequency and α is the unit-less fitting parameter for error correction. In this paper, any parameter with subscript i means it is associated to the ith trap. Fig. 1 shows the BC MOSFET being analysed. In our coordinates, x is the oxide depth direction, y is the channel length direction and z is the channel width direction.

In our method, RTS amplitudes of each trap are calculated with the IFM. In a finite-element numerical analysis, the local microscopic potential fluctuation inside the device mesh grid is caused by the capture or emission of an electron charge from the trap. To determine the impact of the local fluctuation on the drain contact current, the Green's functions are computed by assuming this fluctuation propagation response is linear [17]. Thus by solving only linear perturbation equations rather than drift-diffusion nonlinear equations, the RTS amplitude for traps at any gate oxide coordinates

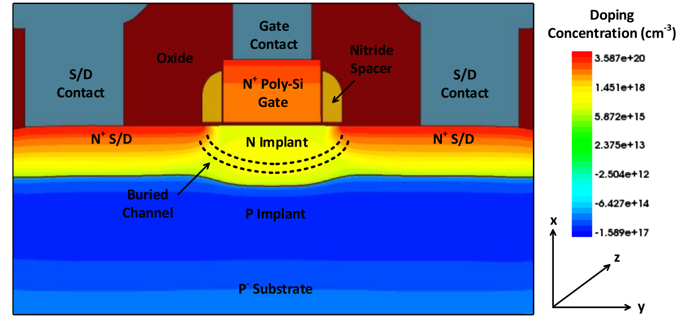


FIGURE 1. N-type channel BC MOSFET device geometry with designed implantation, indicated buried channel path and coordinate axis (device size not in scale).

can be obtained. The RTS amplitude can be calculated by

$$I_{RTS,i} = \sqrt{G_{\varphi}^{I}(x_i, y_i, z_i, f) \cdot q^2 \cdot G_{\varphi}^{I\,*}(x_i, y_i, z_i, f)} \quad (2)$$

where $G_{\varphi}^{I}(x_i, y_i, z_i, f)$ is the Green's functions of potential fluctuation in the oxide trap position (x_i, y_i, z_i) to drain current fluctuation at frequency f, and q is the electron charge.

The capture and emission time constant can be expressed based on the SRH theory [18]:

$$\tau_{c,i} = \frac{1}{\sigma_i\left(x_{t,i}, E_{t0,i}\right) \cdot v_{th} \cdot n_{int,i}} \quad (3)$$

$$\tau_{e,i} = \frac{1}{\sigma_i\left(x_{t,i}, E_{t0,i}\right) \cdot v_{th} \cdot n_{1,i}} \quad (4)$$

where σ_i is the trap capture cross-section that depends on both the trap oxide depth $x_{t,i}$ and intrinsic trap energy level in oxide $E_{t0,i}$, v_{th} is the thermal velocity, $n_{int,i}$ is the electron density at the silicon-oxide interface mesh grid that is closest to the oxide position, and $n_{1,i}$ is the imaginary electron density at the trap energy level

$$n_{1,i} = n_{int,i} \cdot exp\left[\frac{E_{t,i}\left(E_{t0,i}, x_{t,i}, y_i, z_i\right) - E_{Fn}(y_i, z_i)}{kT}\right] \quad (5)$$

where k is the Boltzmann constant, T is the absolute temperature, E_{Fn} is the interface electron quasi-Fermi energy level at the position (y_i, z_i) since a non-zero drain to source voltage will induce a different E_{Fn} along the channel length, and $E_{t,i}$ is the oxide trap energy level which is different from $E_{t0,i}$. For example, a sufficiently negative gate biasing voltage will create a vertical electrical field inside the oxide so as to elevate the energy level of an oxide trap to be higher than $E_{t0,i}$.

The tunneling process is also considered. Thus the trap capture cross-section is determined by both the intrinsic trap energy level $E_{t0,i}$ and trap oxide depth $x_{t,i}$:

$$\sigma_i\left(x_{t,i}, E_{t0,i}\right) = \sigma_{0,i}\left(E_{t0,i}\right) \cdot T\left(x_{t,i}\right) \quad (6)$$

where $\sigma_{0,i}(E_{t0,i})$ is the intrinsic trap capture cross-section, which is defined based on curve fitting explained in the next section. Any oxide trap with certain $E_{t0,i}$ will have an

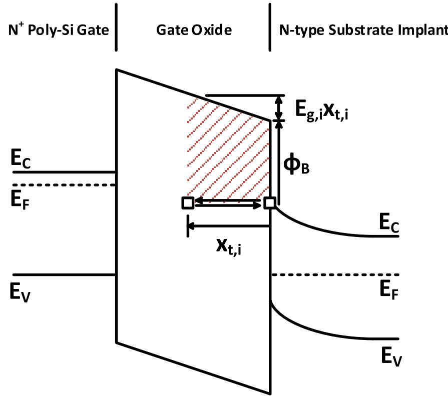


FIGURE 2. N-type channel BC MOSFET band diagram with electron tunneling indicator between conduction band and gate oxide.

associated $\sigma_{0,i}$. $T(x_{t,i})$ in (6) is the tunneling transmission coefficient [19] that is expressed as

$$T(x_{t,i}) = exp\left\{\frac{4\sqrt{2m_{e,ox}}}{3\hbar qE_{G,i}}\left[(\phi_B - x_{t,i}qE_{G,i})^{\frac{3}{2}} - (\phi_B)^{\frac{3}{2}}\right]\right\} \quad (7)$$

where ϕ_B is the potential barrier from the silicon conduction band to oxide conduction band, $\hbar$ and $m_{e,ox}$ are the reduced Planck constant and the electron tunnel mass in oxide respectively, $E_{G,i}$ is the gate oxide electrical field and it is different for each trap along the channel length since the drain-to-source voltage is non-zero. The positive direction for $E_{G,i}$ is defined as from gate to silicon substrate vertically. In this work, the shape of the tunneling potential barrier is treated as a trapezoid, rather than a rectangle for better accuracy since the oxide energy band is bent by applying the gate biasing voltage. The concept is shown in Fig. 2, in which the shadowed area is the potential barrier that the electron needs to overcome for direct tunneling. It can be concluded from (7) that the tunneling transmission coefficient decreases exponentially with the increased trap oxide depth. This value becomes one for a trap with zero oxide depth.

Once the drain current noise contribution from each individual trap is calculated, the total drain current noise can be calculated as the summation

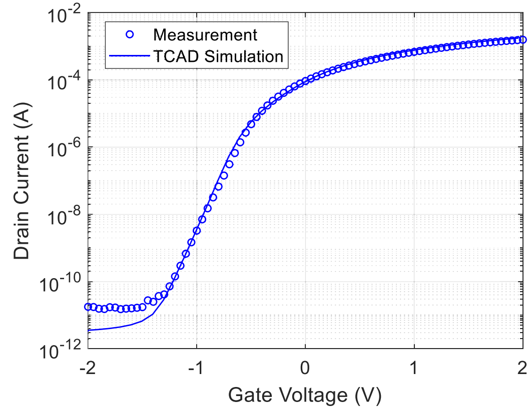
$$S_{ID} = \sum_i S_{ID,i} \quad (8)$$

Obviously, the total drain current noise changes when the gate biasing condition is altered.

III. RESULTS AND DISCUSSION

A. DEVICE FABRICATION

The BC MOSFETs were fabricated in the Nanosystem Fabrication Facility at HKUST by using a 520 μm thick 4-inch boron doped p-type wafer with <100> crystalline orientation. The substrate resistivity was around 15-25 Ohm*cm. In order to comply with the high performance wide dynamic range CIS design methodology [6], the n-type BC MOSFETs were fabricated



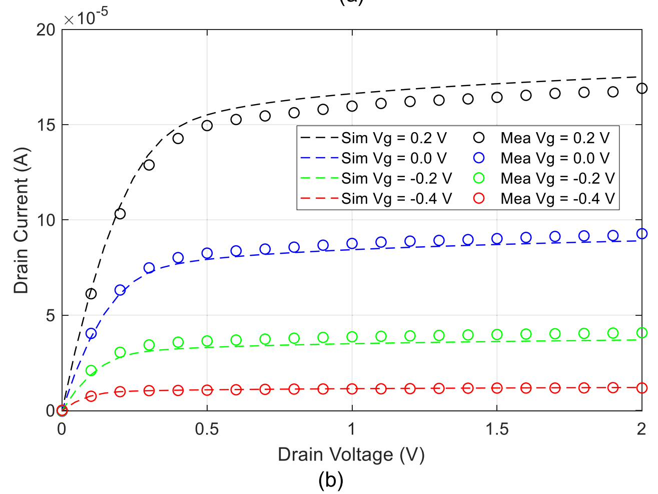


FIGURE 3. Comparison of measurement and TCAD simulation for (a) Id-Vg at $V_D = 2$ V, $V_S = V_B = 0$, (b) Id-Vd at $V_S = V_B = 0$.

with 15 nm thick gate oxide rated at 5 V and used as in-pixel source follower. To minimize the noise impact from Shallow Trench Isolation (STI), the active field was formed by the LOCOS process. Channel ion implantation was performed through a 25 nm thick sacrificial oxide for protection of the silicon surface. Two types of channel ion implantations were performed for a better gate transconductance and source follower voltage gain. Firstly, the boron (B11+) species with a dose of $5\times10^{12}/cm^2$ was implanted at the energy of 180k eV. Then the phosphorus (P31+) species with the dose of $2 \times 10^{12}/cm^2$ was implanted at the energy of 170k eV. Tilt angles were both 7°. Finally, the contact formation and metal wiring were done by aluminum sputtering. To minimize possible plasma induced oxide damage by the antenna effect, it was ensured that there was no plasma process after metals were formed. The sample device channel size is 21 μm in width and 2 μm in length. Large channel area MOSFETs give much better statistical representation than devices with small channel area [10].

B. DC CHARACTERIZATION AND CALIBRATION

The Id-Vg of the fabricated device was characterized by a wafer probe station with a Keysight B1500A Semiconductor Device Analyzer. In parallel, the

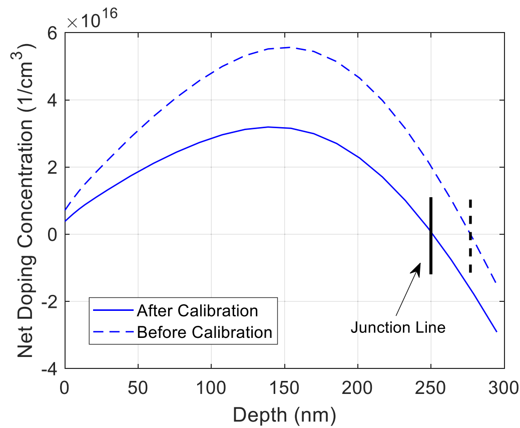


FIGURE 4. Net doping concentration profile from simulation by TCAD Sentaurus Sprocess. The profile is extracted from silicon-oxide interface to substrate vertically downward at center of the device.

fabrication process and DC conditions were simulated with TCAD Sentaurus. The simulation results were compared with the measurements. As expected, the DC of the fabricated device deviated from designed values due to various process factors. In order to match DC conditions for the noise simulation, the parameters of the device simulated in Sentaurus was calibrated. The 2nd channel ion implantation dosage was tuned to match the threshold voltage. The interface trap density was found to be $2\times10^{11}/(cm^2*eV)$ to match the subthreshold slope. The channel width is slightly modified to match the drain current level. After the calibration, the Id-Vg and Id-Vd curve of the fabricated and the simulated device matched well as shown in Fig. 3 below. A little higher off-state leakage current in Fig. 3(a) may result from the additional defect induced generation current.

The net doping concentration profile of the BC MOSFET obtained from TCAD Sentaurus Sprocess simulation is shown in Fig. 4. The net doping concentration at the silicon-oxide interface is around $1\times10^{16}/cm^3$. The peak doping concentration is about 5 times higher than the surface concentration and located at about 150 nm deep from the interface. The profiles before calibration and after calibration are displayed in comparison. The calibrated profile is a little lower than the initial design. The doping profile is sensitive to many parameters such as implantation energy/dose, implantation angle, sacrificial oxide thickness and thermal budget in Rapid Thermal Annealing (RTA).

Using a similar idea to [6], the doping profile is designed as a concave shape to optimize the gate transconductance (g_m). When the gate voltage is decreased, a depletion region beneath the interface is formed to separate the conducting channel from the silicon surface. The shallow depletion region forms easily because the doping concentration near surface is relatively low. Hence a decent g_m can be obtained since the channel vertical thickness reduces easily. As the gate biasing voltage becomes more negative, the depletion region reaches more than 100 nm. It is hard to increase the depletion depth further since the gate controllability over the channel is weak due to the small depletion capacitance in series with the gate oxide capacitance. However, the channel is very thin vertically at this time due to the depletion between the N-type channel implantation and P-type substrate. As we can observe from Fig. 4, the junction line is at around 250 nm. The buried channel is suppressed from both sides vertically as indicated in Fig. 1, and can be switched off. Thus a decent g_m is also guaranteed for low gate biasing voltage for the deep buried channel condition.

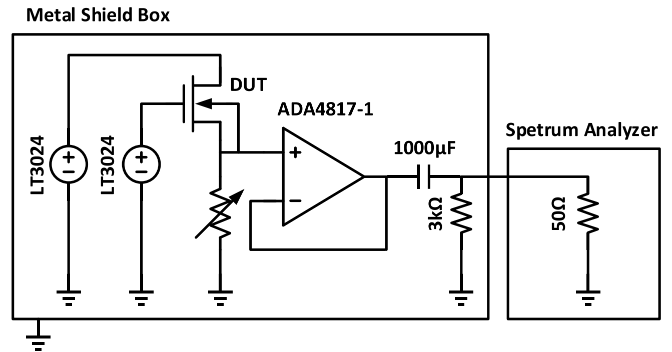


FIGURE 5. Noise measurement setup for the BC MOSFET. The noise PSD is measured by a spectrum analyzer.

TABLE 1. DC parameters of BC MOSFET.

V_{GS} (V)	I_D (μA)	g_m (μS)	Source Follower Gain (V/V)
+0.1	135.8	343.9	0.78
-0.1	68.8	225.6	0.84
-0.3	26.4	107.5	0.88
-0.5	5.4	42.4	0.94

C. TESTING SETUP

The noise spectrum of the fabricated BC MOSFETs was measured by an R&S FSW spectrum analyzer. The testing setup is shown in Fig. 5. During noise measurement, the BC MOSFETs were configured as source followers with a variable source resistor to achieve different V_{GS} conditions, while the gate and drain were fixed at 1.5 V and 5 V respectively. The source was connected to the body to eliminate the body effect. A low noise voltage regulator LT3024 was used for gate and drain biasing, which had a PSD of $3\times10^{-12}V^2/Hz$ at 10Hz and $2\times10^{-14}V^2/Hz$ at 10k Hz based on our measurement. For consideration of the driving capability and the bandwidth, a Low Noise Amplifier (LNA) ADA4817-1 was configured in unit gain feedback topology as the voltage buffer. The PSD of the input referred noise from the LNA was $4\times10^{-14}V^2/Hz$ at 10Hz and $3\times10^{-17}V^2/Hz$ at 10k Hz based on the datasheet. To isolate the DC from the spectrum analyzer, a 1000 μF electrolytic capacitor was used as a high pass filter which had a cutoff frequency much lower than 10 Hz. The device under test (DUT) with voltage regulator, LNA and filter were enclosed in a metal box to minimize impact from ambient electromagnetic interference.

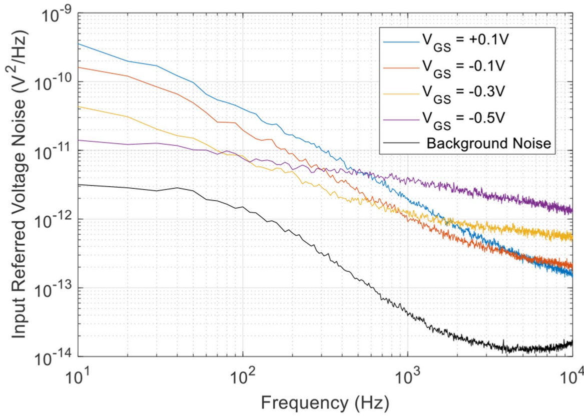


FIGURE 6. Measurement input referred voltage noise PSD for BC MOSFETs for different gate biasing conditions.

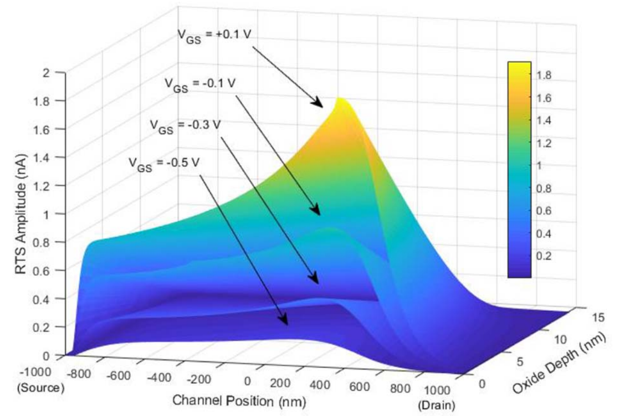


FIGURE 7. Oxide RTS amplitude distribution for different V_{GS} conditions based on IFM simulation.

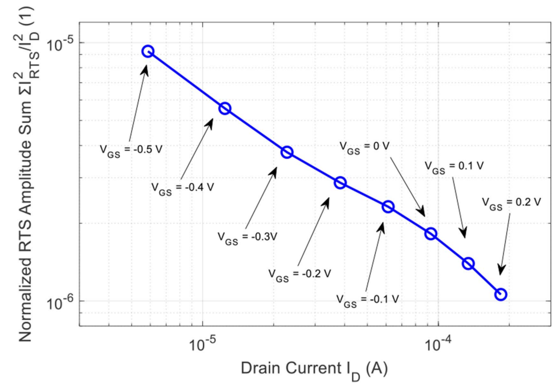


FIGURE 8. Simulated $\Sigma I_{RTS}^2/I_D^2$ versus drain current for $V_{DS} = 5V$.

D. NOISE MEASUREMENT

The output voltage noise was directly measured by the spectrum analyzer. The input referred noise was calculated based on (9) and is plotted in Fig. 6.

$$S_{V,input} = S_{V,output}/A^2 \tag{9}$$

where $S_{V,output}$ and $S_{V,input}$ are the measured output voltage noise PSD and calculated input referred voltage noise PSD. A is the source follower voltage gain. The background noise from the voltage regulator, source resistor, LNA and spectrum analyzer is subtracted from the results. DC parameters of the BC MOSFETs are listed in Table 1. Due to the doping profile designed in Fig. 4, the source follower gain remains decent from the accumulation region to the weak inversion region.

The patterns in Fig. 6 are similar to measurements in previous works [8] and [20]. The LFN slope factor γ is found to drop with a more negative gate biasing.

E. NOISE SIMULATION

With the same biasing voltages as in Table 1, DC conditions of the BC MOSFET was solved by Sentaurus Device. The device noise spectrum can be simulated with our low frequency noise simulator by using the exported DC information exported from Sentaurus Device. The constants used in our simulation are: thermal velocity $v_{th} = 1.5 \times 10^7 cm/s$, absolute temperature $T = 300K$, unitless fitting parameter $\alpha = 1.65$ and electron tunnel mass $m_{e,ox} = 0.5m_{e,0}$, where $m_{e,0}$ is the electron effective mass.

Based on the simulation method explained in the previous section, the simulated PSD of the input referred voltage noise can be obtained from (10) based on [21], where S_{ID} is calculated based on (8) and g_m is the gate transconductance extracted from device simulation.

$$S_{V,input} = S_{ID}/{g_m}^2 \tag{10}$$

The simulated RTS amplitude distribution in oxide is shown in Fig. 7, which exhibits a similar amplitude and distribution to that shown in [4] for the saturation condition. The RTS amplitude is independent of the channel width for a long channel device [4]. Hence, we ignored the channel width dimension in our simulations.

To determine whether the dominant noise source is due to Carrier Number Fluctuation (CNF) or Hooge Mobility Fluctuation (HMF) mechanism, usually the slope of S_{ID}/I_D^2 versus the drain current is analyzed [22]. However, the noise spectrum of our device is in the form of $1/f^{\gamma}$ where the noise slope factor γ changes with drain currents, it makes the slope of S_{ID}/I_D^2 versus the drain current frequency dependent. Instead, we use $\Sigma I_{RTS}^2/I_D^2$ to eliminate the impact of varying γ, which is equivalent to the method in [4]. It had been demonstrated that I_{RTS} will incorporate both the CNF and HMF mechanisms as analysis in (19) and (20) from [4].

The simulated $\Sigma I_{RTS}^2/I_D^2$ is shown in Fig. 8, where ΣI_{RTS}^2 means the summation of all I_{RTS}^2 inside the oxide mesh for each drain current condition. From Fig. 8, we can see that the $\Sigma I_{RTS}^2/I_D^2$ is inversely proportional to the drain current. This indicates the HMF effect dominates. It agrees with [22] as our device is a buried channel device with volume mode operation.

The RTS amplitude decreases if the oxide depth increases since the trap that is far away from the conducting channel will cause less drain current fluctuation. As the gate voltage

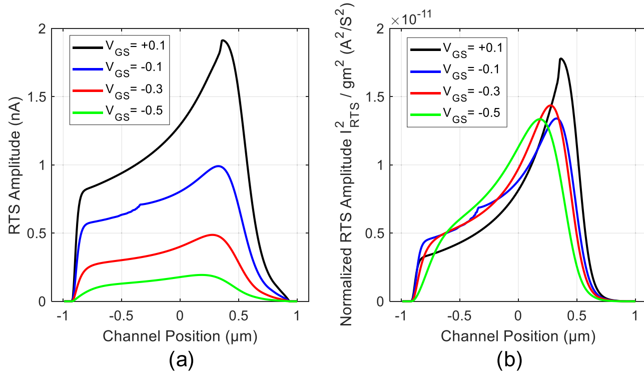


FIGURE 9. (a) Oxide RTS amplitude distribution at silicon-oxide interface for different V_{GS} conditions based on IFM simulation. (b) Normalized RTS amplitude distribution (I_{RTS}^2/g_m^2) at silicon-oxide interface.

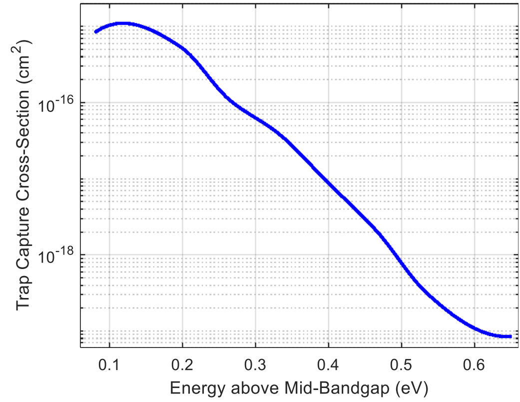


FIGURE 11. Trap capture cross-section distribution with energy used for simulation.

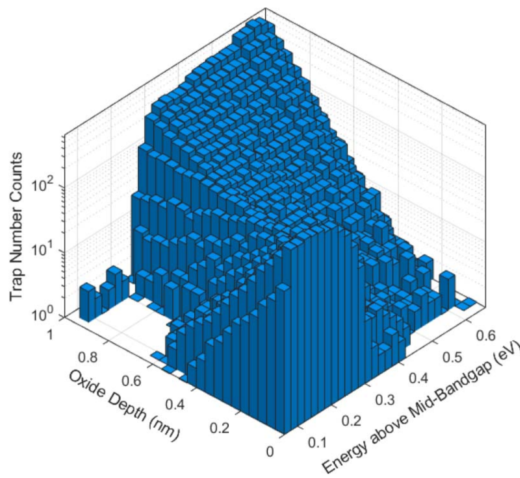


FIGURE 10. Histogram view of trap energy and oxide depth distribution.

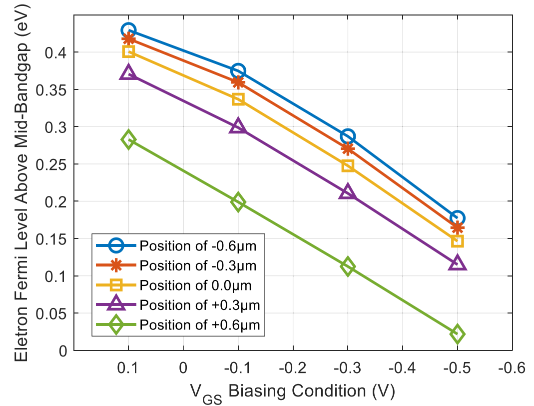


FIGURE 12. Interface electron quasi-Fermi level above mid-bandgap energy versus gate biasing conditions at different channel length positions from −1 μm (source) to +1 μm (drain).

becomes more negative, the channel is buried deeper with the decreasing RTS amplitude. To have a better understanding of how the RTS amplitude affects the input referred noise from different gate biasing conditions, a normalized view is plotted in Fig. 9 (b). Based on equations (1), (8) and (10), the normalization is in the form of (I_{RTS}^2/g_m^2) as it forms an indicator of how the RTS amplitude contributes to the PSD of the input noise voltage. We can observe that the impact from the RTS amplitude decreases with the V_{GS} changing from +0.1V to −0.1V, which is the moment that the channel has just been buried. The indicator value does not change much when V_{GS} further decreases from −0.1V to −0.5V. This is because the g_m significantly decreases for a low drain current.

In our noise simulation, the trap is randomly generated inside the channel area and within the energy band based on the trap density extracted from the DC calibration. Ultra-slow traps that fall out of the 10 Hz to 10k Hz frequency range of interest are not considered. Hence, only traps within 1 nm from the oxide surface are relevant. The information of the trap distribution and the trap capture cross-session distribution $\sigma_{0,i}(E_{t0,i})$ in (6) are obtained through curve fitting. The traps are found to follow an exponential distribution with energy level as shown in Fig. 10. The trap capture cross-section distribution is found to be in Fig. 11, which is similar to [23] and [24].

The silicon-oxide interface electron Fermi level at different channel length positions for different gate biasing conditions is shown in Fig. 12. It is important to know the Fermi level position since the noise contribution of a trap reaches maximum if its energy level is the same with the Fermi level [25]. Along the channel length direction from source to drain, the Fermi level decreases due to the non-zero drain to source voltage. For a more negative gate biasing condition, the Fermi level is lower due to a lower electron density at the interface. For the highest RTS amplitude position (around +0.3 μm) observed from Fig. 9, the Fermi level sweep range is around 0.1 eV to 0.4e V above mid-bandgap level based on Fig. 12. This well explains the fitting range of the trap energy level in Fig. 10 since the traps with higher RTS amplitude contributes more to the total noise PSD.

The simulated noise spectrum is shown in Fig. 13. In general, it matches the measured results well. The minor discrepancy could be due to different trap densities over the energy range in the fabricated device. Also based on

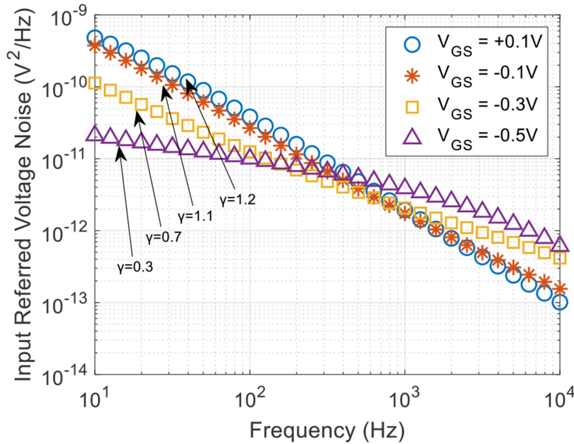


FIGURE 13. Simulated input referred voltage noise PSD for BC MOSFETs for different gate biasing conditions.

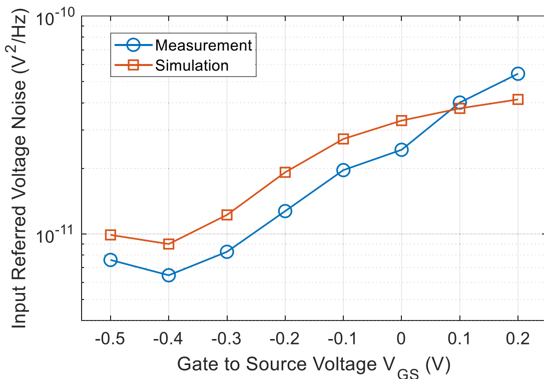


FIGURE 14. Comparison of simulated and measured input referred voltage noise power versus V_{GS} at 100 Hz for $V_{DS} = 5$ V.

the RTS amplitude contribution indicator (I_{RTS}^2/g_m^2) defined in Fig. 9(b), the wrongly estimated effective channel size (W or L) induced I_{RTS} and g_m error could result in additional discrepancies based on (10). The trap distribution in Fig. 10 explains the changing LFN slope γ in Fig. 6. For a more negative gate bias, the channel is buried deeper. The electron quasi-Fermi energy level at the Si/SiO2 interface is closer to mid-bandgap energy level. This means that, as the channel is buried deeper, more fast traps (traps close to the interface) will contribute to the noise, which will decrease the slope [10], [15].

The comparison of the simulated and measured input referred voltage noise power at 100 Hz are plotted against gate voltage in Fig. 14. The noise power drops about one decade when the gate to source voltage decreases from 0.2 V to −0.5 V. This is because the interactions between traps and carriers become slower as the channel is buried. Meanwhile, for a more buried channel condition, the Fermi level is more close the mid-bandgap level, less slow traps are activated. As we can observe from Fig. 10 in the manuscript, the trap number is small for the thick oxide low energy region.

The comparison of simulated and measured input referred voltage noise spectrum versus different drain voltage at

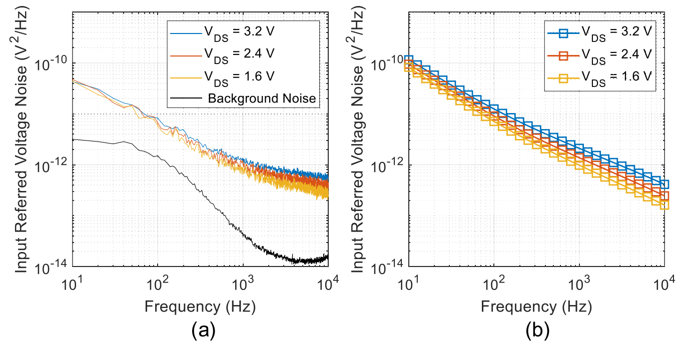


FIGURE 15. Comparison of measured (a) and simulated (b) input referred voltage noise power versus drain voltage for $V_{GS} = -0.3$ V.

$V_{GS} = -0.3$ V are plotted in Fig. 15. For the different drain voltage conditions, the gate voltage is maintained at 1.5 V, we change the drain biasing to achieve the V_{DS} conditions of 3.2 V, 2.4 V and 1.6 V. During the process, only a little tuning of source resistor is needed to achieve the constant $V_{GS} = -0.3$ V condition since the voltage gain from drain to source is extremely small. Observed from Fig. 15, for a smaller V_{DS} value the whole spectrum decreases a little while the noise slope factor γ slightly increases. The reason is that the RTS amplitude peaking in the saturation pinch-off channel position will decrease for a smaller V_{DS} condition, which is also observed in [4]. The reduced RTS amplitude peaking will lower the whole noise spectrum a little based on equation (1). Meanwhile, the peaking position is at around 400 nm channel position observed from Fig. 7. For this position at $V_{GS} = -0.3$ V, it can be found that the electron Fermi level is about 0.2 eV above mid-bandgap from Fig. 12. For this energy level, the most activated traps are fast traps (low oxide depth) as observed from Fig. 10. Less fast traps noise impact will decrease the noise spectrum amplitude in high frequency range. Thus, the noise slope factor γ increases.

IV. CONCLUSION

In this paper, a numerical model is developed for the LFN in BC MOSFETs. The noise model is based on SRH theory with the inclusion of WKB tunneling approximation. The RTS amplitude is calculated efficiently by Green's function based on IMF. The model is verified with BC MOSFETs fabricated in a CIS process. It matches well with the measurements.

With the new model, the $1/f^{\gamma}$ LFN of BC MOSFETs can be observed, and its mechanism can be quantitatively explained. It is found that the LFN slope γ decreases as the channel is buried deeper, which occurs because more fast traps are activated with a lower gate bias voltage.

REFERENCES

[1] C. M. Compagnoni, M. Ghidotti, A. L. Lacaita, A. S. Spinelli, and A. Visconti, "Random telegraph noise effect on the programmed threshold-voltage distribution of flash memories," *IEEE Electron Device Lett.*, vol. 30, no. 9, pp. 984–986, Sep. 2009.

[2] Y. Chen, X. Wang, A. J. Mierop, and A. J. P. Theuwissen, "A CMOS image sensor with in-pixel buried-channel source follower and optimized row selector," *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2390–2397, Nov. 2009.

[3] M. J. Uren, D. J. Day, and M. J. Kirton, "1/f and random telegraph noise in silicon metal–oxide–semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 47, no. 11, pp. 1195–1197, Dec. 1985.

[4] Y. Higashi *et al.*, "Unified transient and frequency domain noise simulation for random telegraph noise and flicker noise using a physics-based model," *IEEE Trans. Electron Devices*, vol. 61, no. 12, pp. 4197–4203, Dec. 2014.

[5] L. K. J. Vandamme and F. N. Hooge, "What do we certainly know about $1/f$ noise in MOSTs?" *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3070–3085, Nov. 2008.

[6] K. D. Stefanov, Z. Zhang, C. Damerell, D. Burt, and A. Kar-Roy, "Performance of deep-depletion buried-channel *n*-MOSFETs for CMOS image sensors," *IEEE Trans. Electron Devices*, vol. 60, no. 12, pp. 4173–4179, Dec. 2013.

[7] R. W. Brodersen and S. P. Emmons, "Noise in buried channel charge-coupled devices," *IEEE J. Solid-State Circuits*, vol. SSC-11, no. 1, pp. 147–155, Feb. 1976.

[8] X. Wang, P. R. Rao, and A. J. P. Theuwissen, "Characterization of the buried channel n-MOST source followers in CMOS image sensors," in *Proc. Int. Image Sensors Workshop*, Ogunquit, ME, USA, Jun. 2007, pp. 6–10.

[9] J. T. Ryu, S. B. Jeon, H. S. Koh, and T. W. Kim, "FinFETs with a deep buried channel to reduce the readout noise in CMOS image sensors," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 530–532, May 2016.

[10] T. H. Morshed, M. V. Dunga, J. Zhang, D. D. Lu, A. M. Niknejad, and C. Hu, "Compact modeling of flicker noise variability in small size MOSFETs," in *IEEE Int. Electron Devices Meeting (IEDM) Tech. Dig.*, 2009, pp. 719–722.

[11] N. Mavredakis, M. Bucher, P. Habas, A. Acovic, and R. Meyer, "Statistical compact modeling of low frequency noise in buried-channel, native, and standard MOSFETs," in *Proc. Int. Conf. Noise Fluctuations (ICNF)*, Jun. 2017.

[12] M. Malits, I. Brouk, Y. Nemirovsky, A. Birman, A. Lahav, and A. Fenigstein, "Low frequency noise in surface and buried channel nanometric CMOS transistors," in *Proc. IEEE Conv. Elect. Electron. Eng. Israel (IEEEI)*, Dec. 2014, pp. 1–5.

[13] Y. Omura and S. Sato, "Theoretical models for low-frequency noise behaviors of buried-channel MOSFETs," in *Proc. IEEE SOI 3D Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, Oct. 2017.

[14] P. Kushwaha *et al.*, "Characterization and modeling of flicker noise in FinFETs at advanced technology node," *IEEE Electron Device Lett.*, vol. 40, no. 6, pp. 985–988, Jun. 2019.

[15] Z. Celik-Butler and T. Y. Hsiang, "Spectral dependence of $1/f^{\gamma}$ noise on gate bias in *n*-MOSFETS," *Solid-State Electron.*, vol. 30, no. 4, pp. 419–423, Jun. 1987.

[16] M. J. Kirton and M. J. Uren, "Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency ($1/f$) noise," *Adv. Phys.*, vol. 38, no. 4, pp. 367–468, 1989.

[17] F. Bonani, G. Ghione, M. R. Pinto, and R. K. Smith, "An efficient approach to noise analysis through multidimensional physics-based models," *IEEE Trans. Electron Devices*, vol. 45, no. 1, pp. 261–269, Jan. 1998.

[18] W. Shockley and J. W. T. Read, "Statistics of the recombination of holes and electrons," *Phys. Rev.*, vol. 87, no. 5, pp. 835–842, Sep. 1952.

[19] M. Depas, B. Vermeire, P. W. Mertens, R. L. Van Meirhaeghe, and M. M. Heyns, "Determination of tunneling parameters in ultra-thin oxide layer poly-Si/SiO_2/Si structures," *Solid-State Electron.*, vol. 38, no. 8, pp. 1465–1471, Aug. 1995.

[20] C. Carruthers and J. Mavor, "Low-noise operation of buried channel MOS transistors," *IEEE Electron. Lett.*, vol. 23, no. 22, pp. 1173–1174, Oct. 1987.

[21] B. Razavi, *Design of Analog CMOS Integrated Circuits*. Boston, MA, USA: McGraw-Hill, 2001, pp. 224–225.

[22] G. Ghibaudo and O. Roux-dit-Buisson, "Low frequency fluctuations in scaled down silicon CMOS devices status and trends," in *Proc. Eur. Solid-State Device Res. Conf.*, Sep. 1994, pp. 693–700.

[23] H. Deuling, E. Klausmann, and A. Goetzberger, "Interface states in Si/SiO_2 interfaces," *Solid-State Electron.*, vol. 15, no. 5, pp. 559–571, May 1972.

[24] T. J. Tredwell and C. R. Viswanathan, "Interface-state parameter determination by deep-level transient spectroscopy," *Appl. Phys. Lett.*, vol. 36, no. 6, pp. 462–464, Jun. 1980.

[25] N. Zanolla, D. Šiprak, M. Tiebout, P. Baumgartner, E. Sangiorgi, and C. Fiegna, "Reduction of RTS noise in small-area MOSFETs under switched bias conditions and forward substrate bias," *IEEE Trans. Electron Devices*, vol. 57, no. 5, pp. 1119–1128, May 2010.