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Impact of Cycling Induced Intercell Trapped Charge on Retention Charge Loss in 3-D NAND Flash Memory

XINLEI JIA [1,2], LEI JIN [1,2,3], WEI HOU [1,2], ZHIYU WANG [1,2], SONGMIN JIANG [3], KAIWEI LI [3], DEJIA HUANG [3], HONGTAO LIU [3], WENZHE WEI [3], JIANWEI LU [3], AN ZHANG [3], AND ZONGLIANG HUO [1,2,3]

1 University of Chinese Academy of Sciences, Beijing 100049, China
2 Institute of Microelectronics of Chinese Academy of Sciences, Beijing 100029, China
3 Yangtze Memory Technologies Company, Ltd., Wuhan 430205, China

CORRESPONDING AUTHORS: L. JIN AND Z. HUO (e-mail: jinlei@ime.ac.cn; huozongliang@ime.ac.cn)

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ABSTRACT As the 3D NAND technology developing toward more and more stack layers, it is essential to shrink the gate length (Lg) and inter-gate space (Ls). However, one of key concerns of scaling Lg/Ls 3D NAND flash is post-cycling data retention characteristics. The impact of cycling induced intercell trapped charge on two primary charge loss mechanisms (vertical and lateral charge loss) was studied in this work. According to experimental analysis and TCAD simulation, it is found that, in vertically scaled 3D NAND, the vertical charge loss is deteriorated not only by the cycling induced tunnel oxide degradation (introducing interface/oxide traps), but also by the cycling induced intercell trapped charge (enhancing word-lines edge electric field), on account of the enhanced Poole-Frenkel effect and tunneling effect. On the other hand, the cycling induced intercell trapped charge can also suppress lateral charge migration. Therefore, the vertical charge loss, rather than the lateral charge migration, still can be the dominant factor for post-cycling retention characteristics in scaling Lg/Ls 3D NAND flash memory.

INDEX TERMS 3D NAND flash memory, data retention, intercell trapped charge, PE cycling.

I. INTRODUCTION

For the demand of higher bit density and lower bit cost, three-dimension (3D) NAND flash memory with vertical channel type cells has become the mainstream of non-volatile memory technology [1], [2]. Triple level cell (TLC) and quad level cell (QLC) technologies will further achieve larger data density [3]. However, as the 3D NAND technology develop toward more and more stack layers, the large aspect ratio of etching channel holes becomes the significant challenge. It is essential to shrink the gate length (Lg) and inter-gate space (Ls). On the other hand, the scaling of Lg and Ls can directly impact the trapped charge distribution and migration in the charge trapping layer. In particular, the charge trapping layer of 3D NAND flash are continuous along the channel hole which can lead to additional charge loss due to lateral charge migration [4], [5]. Therefore, it is important to clarify if lateral charge migration will turn much worse and figure out the dominant factor, vertical or lateral charge loss, in post-cycling retention characteristics of vertically scaled 3D NAND flash memory.

In this work, the impact of PE cycling on data retention mechanism (vertical and lateral charge loss) of charge trap based 3D NAND is studied. It is considered that, in vertically scaled 3D NAND flash, besides the tunnel oxide degradation, the naturally accumulating intercell trapped charge during PE cycling can deteriorate vertical charge loss, and suppress lateral charge migration. Therefore, the vertical charge loss is still the dominant factor in post-cycling retention characteristics.

II. DEVICE AND EXPERIMENTS

In this work, the experiment is based on 3D NAND flash test chips composed of continuous charge trapping layer and vertical poly-Si channel, which was reported in our

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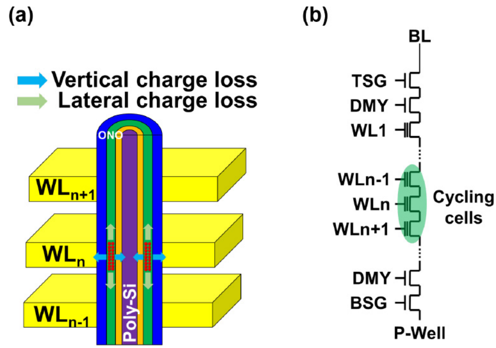

FIGURE 1. (a) The diagram of two charge loss mechanisms in 3D NAND. (b) Diagram of 3D NAND string. In this work, three adjacent WLs were chosen for PE cycling under PPP pattern at 85°C, for cycling stress.

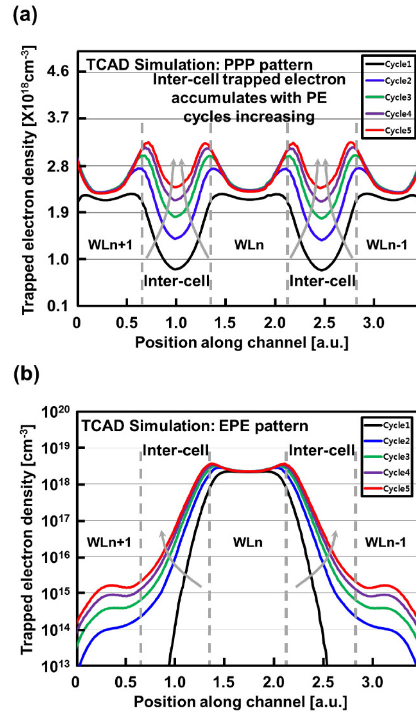

FIGURE 2. TCAD simulation result of trapped electron distribution in the erase state with PE cycles increasing under (a) PPP pattern and (b) EPE pattern.

previous work [1]–[3]. The test samples are divided into four groups (i.e., G1, G2, G3 and G4). In group G1 and G2, three adjacent word-lines (WL) in the string were chosen for PE cycling under program-program-program (PPP) pattern at 85°C, as shown in Fig. 1(b). G3 and G4 are used as the control group without PE cycling. Afterwards, erase-program-erase (EPE) pattern is built up in group G1 and G3. And PPP pattern is built up in group G2 and G4. Finally, after high temperature baking (125°C, 2hrs), WL_n V_t shift is measured on designed array test structure by semiconductor parameter analyzer.

In addition, Sentaurus Sdevice simulator is used for TCAD simulation. In charge trapping layer, the drift-diffusion model and charge trapping/de-trapping model are taken into account. Meanwhile, non-local tunneling (NLT) model through tunneling layer and blocking layer is considered [2]. The interaction between free carriers and trapped carriers is governed by carrier capture phenomenon calculated by Shockley-Read-Hall (SRH) theory and carrier emission contributed by thermal and Poole-Frenkel effect [4].

III. RESULTS AND DISCUSSION

The two charge loss mechanisms of data retention in 3D NAND are shown in the diagram of Fig. 1(a), which are lateral charge migration in the charge trapping layer and vertical charge loss through the tunneling and blocking oxide, respectively [6]. It is well known that PE cycling can degrade the tunnel oxide and deteriorate vertical charge loss by introducing interface/oxide traps, which have been studied intensively. On the other hand, PE cycling can also impact the charge distribution in the intercell region with continuous charge trapping layer [7].

Fig. 2 shows the simulation results of the trapped electron distribution in the erase state under PPP pattern and EPE pattern, with one to five PE cycles. The cell V_t is programed or erased to identical level in each PE cycle. The simulation results of EPE and PPP patterns all show that, as the PE cycling repeated, more and more electrons accumulated in the intercell region. It is caused by the different fringe electric field profiles in the tunnel oxide during PE operations [7].

In this work, the impact of PE cycling induced intercell trapped charge on post-cycling retention mechanism (vertical and lateral charge loss) in vertically scaled 3D NAND Flash is studied as follows. It should be noted that, Lg/Ls scaling range of 5-10nm is studied in this work. And all Lg/Ls splits are larger than 25nm in our TCAD simulation. On the other hand, instead of >1K PE cycles in TCAD simulator (unacceptable consumption of simulation time for more than 20 PE cycles), fixed-electrons are placed in the intercell region (to mimic intercell trapped charge after cycling) to investigate the influence of the intercell trapped charge and the amount of fixed-electrons is based on the simulation results of Fig. 2 in our simulation.

A. IMPACT OF PE CYCLING INDUCED INTERCELL TRAPPED CHARGE ON LATERAL CHARGE MIGRATION

In the industry, the lateral charge migration is commonly characterized by the difference between the retention V_t shifts of programmed WL_n cell in WL_{n-1}-WL_n-WL_{n+1} with EPE pattern and PPP pattern respectively [8]. It is because that, under EPE pattern, WL_n Vt shift is caused by both vertical and lateral charge loss. But under PPP pattern, WL_n Vt shift is mainly caused by the vertical charge loss [9], [10]. The WL_n V_t shifts are measured with over 20 single cells and extract its median value. Fig. 3 shows the experiment results of charge loss with and without PE cycling. It is interesting that, compared with memory cells without PE cycling, lateral charge migration is suppressed by 36% in cells undergo 3000 PE cycles.

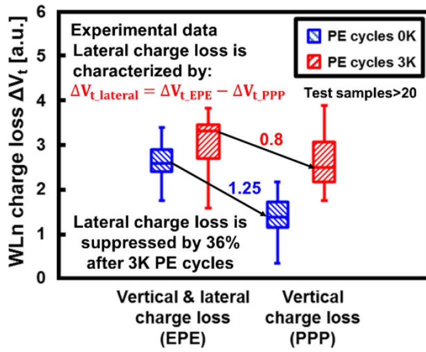

FIGURE 3. WL_n charge loss ΔV_t (125C 2hrs) of EPE and PPP pattern is measured (>20 samples) with and without PE cycling. For both cycled and fresh samples, V_t was programmed to identical level before retention bake.

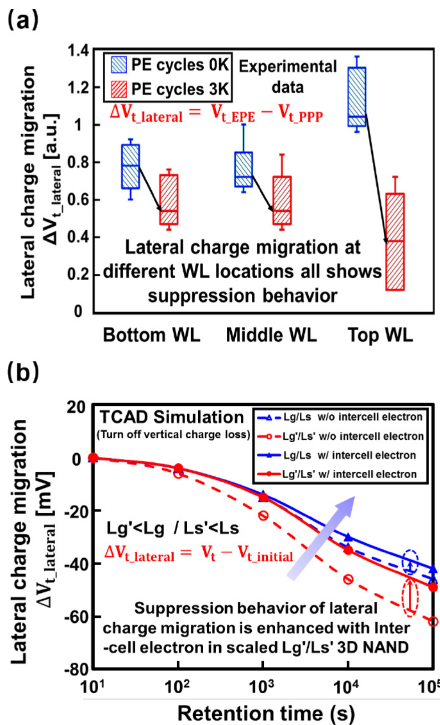

FIGURE 4. (a)Lateral charge migration $\Delta V_{t-lateral}$ of different WLs (>120 samples) with and without PE cycling, (b)TCAD simulation result of lateral charge loss with and without the inter-cell trapped charge in different Lg/Ls (Lg′<Lg and Ls′<Ls) 3D NAND flash.

Some studies indicate that lateral charge migration can be improved by intentionally introducing intercell trapped charge [11], [12]. Several approaches of introducing intercell trapped charge has been reported, such as, ① space program scheme consisting of all gate program, odd/even gate erase [11], and ② charge injection in all cells and then high temperature baking induced charge diffusion [12]. Therefore, it can be expected that, the post-cycling lateral charge migration shall be also affected by the cycling induced intercell trapped charge.

In Fig. 4(a), the WLs in different layer location and different samples (>120 samples) are measured. Lateral charge migration at bottom/middle/top WLs is suppressed by average about 30%. This indicates the lateral charge migration suppression after cycling is typical. In addition, For the fresh sample, the difference of lateral charge migration ($\Delta V_{t_lateral}$) among the top WL, middle WL and bottom WL can be attribute to the process difference of different WLs, such as the channel hole diameter and ONO gate stack films step coverage.

Lateral charge migration of programed WL_n cell with intercell trapped charge was further evaluated by TCAD (NLT model turned off). In order to eliminate the impact of vertical charge loss, NLT model is turned off during data retention simulation. Fig. 4(b) reveals the simulation results of the V_t shifts with and without inter-cell trapped charge in different Lg and Ls. In case of Lg/Ls, the lateral charge migration can be suppressed by the inter-cell trapped charge (from the blue dotted line to the blue solid line). And the influence of intercell trapped charge on lateral charge migration is enhanced with inter-cell trapped charge in scaled Lg′/Ls′ 3D NAND.

Therefore, the above results indicate that lateral charge migration will not turn much worse in vertically scaled 3D NAND flash memory on account of the suppression behavior by the naturally accumulating intercell trapped charge by PE cycling.

B. IMPACT OF PE CYCLING INDUCED INTERCELL TRAPPED CHARGE ON VERTICAL CHARGE LOSS

With the scaling of Lg/Ls in 3D NAND, the location of PE cycling induced intercell trapped charge will be much closer to the programed WL_n cell, which can impact the WL edge electric field. Therefore, it can be expected that, in scaling Lg/Ls 3D NAND, the post-cycling vertical charge loss shall be also affected by the cycling induced intercell trapped charge.

In order to verify the impact of intercell trapped charge on vertical charge loss by experiments, intercell trapped charge are introduced by odd/even erase operations [11]. It should be noted that, to eliminate the impact of tunnel oxide degradation by PE cycling, the odd/even erase operation is considered to be equivalent to accumulated intercell trapped charge after PE cycling. The intercell trapped charge is characterized by the threshold voltage difference ($\Delta V_{t_intercell}$) of WL_n and tied WL_n&WL_{n+1} [11]. The $\Delta V_{t_intercell}$ is measured with over 10 single cells. As shown in Fig. 5(a), the $\Delta V_{t_intercell}$ with odd/even erase is larger than that without odd/even erase, indicating that intercell trapped charges have been set up as expected. On the other hand, in order to eliminate the impact of lateral charge migration on V_t shift, after odd/even erase operation, the PPP pattern was built up to evaluate the vertical charge loss [9]. In Fig. 5(b), the V_t shift (contains only vertical charge loss) of WL_n with intercell trapped charge is about 27% larger than the case without intercell trapped charge. This result indicates that intercell trapped charge can deteriorate vertical charge loss.

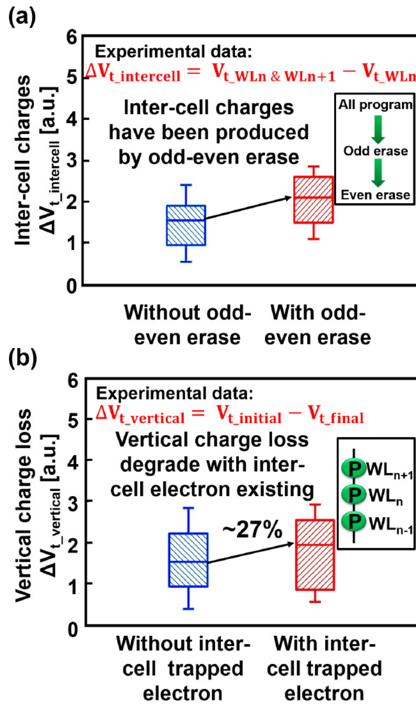

FIGURE 5. (a) Intercell trapped charges $\Delta V_{t\text{-}intercell}$ (>10 samples) with and without odd/even erase, (b) Vertical charge loss $\Delta V_{t\text{-}vertical}$ (>10 samples) with and without inter-cell trapped charge under PPP pattern.

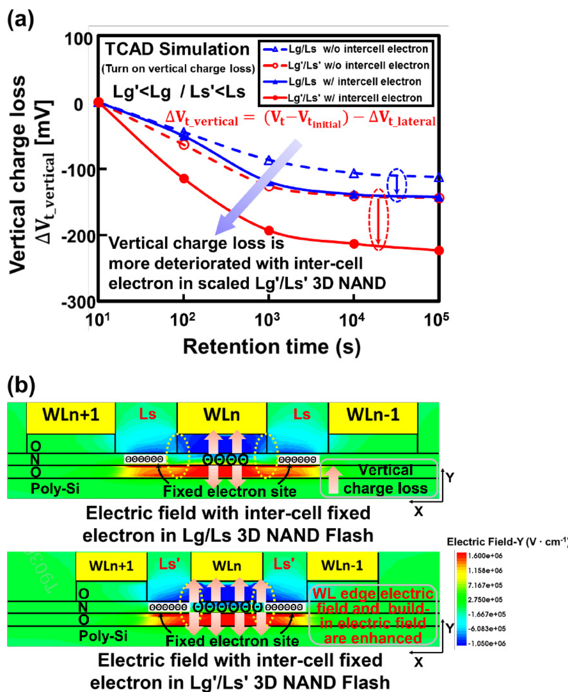

FIGURE 6. (a) TCAD simulation result of vertical charge loss with and without the inter-cell trapped charge in different Lg/Ls (Lg′<Lg and Ls′<Ls) 3D NAND flash, (b) the build-in electric field distribution with the scaling of Lg and Ls.

Vertical charge loss of programed WL_n cell with intercell trapped charge was evaluated by TCAD (NLT model turned on). As shown in the Fig. 6(a), in case of Lg/Ls, the inter-cell trapped charge can deteriorate the vertical charge loss (from the blue dotted line to the blue solid line). And the influence of inter-cell trapped charge on vertical charge loss will be more pronounced in scaled Lg′/Ls′ 3D NAND.

Fig. 6(b) shows that, in scaling Lg/Ls 3D NAND Flash, on account of the higher WL edge electric field and build-in electric field, the enhanced Poole-Frenkel effect and tunneling effect will lead to more emission of trapped charges and more vertical charge loss [13].

In summary, compared to the suppressed lateral charge migration caused by the cycling induced inter-cell trapped charge, the more deteriorated vertical charge loss caused by the additional enhancing WL edge electric field still can be the dominant in post-cycling retention characteristics of vertically scaled 3D NAND flash memory.

IV. CONCLUSION

In this work, the impact of PE cycling on data retention mechanism (vertical and lateral charge loss) is investigated in charge trap based 3D NAND flash test chips. During PE cycling, there are accumulated charges in the intercell regions of charge trapping layer. In addition to the generally tunneling layer degradation induced by PE cycling stress, it is found that intercell trapped charge can deteriorate vertical charge loss induced by the enhanced Poole-Frenkel effect and tunneling effect. Furthermore, the intercell trapped charge can also suppress the lateral migration of trapped charges in the programed cells during data retention. Therefore, the vertical charge loss induced by PE cycling, rather than the lateral charge migration, still can be the dominant factor of post cycling retention characteristics in the vertically scaled 3D NAND flash.

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