Received 17 June 2019; revised 20 August 2019, 16 October 2019, 22 November 2019, and 22 December 2019; accepted 28 December 2019.
Date of publication 1 January 2020; date of current version 17 January 2020. The review of this article was arranged by Editor A. Nathan.

Digital Object Identifier 10.1109/JEDS.2019.2963431

Novel Driving Methods of Gate Driver for Enhancement- and Depletion-Mode Oxide TFTs

JONGSU OH [1], KYUNG-MO JUNG [1], EUN KYO JUNG [1], JUNGWOO LEE [1], SOO-YEON LEE [2], KEECHAN PARK [3], JAE-HONG JEON [4], AND YONG-SANG KIM [1]

1 Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon 16419, South Korea
2 Department of Electrical and Computer Engineering, Seoul National University, Seoul 08826, South Korea
3 Department of Electronics Engineering, Konkuk University, Seoul 05029, South Korea
4 School of Electronics and Information Engineering, Korea Aerospace University, Goyang 10540, South Korea

CORRESPONDING AUTHOR: Y.-S. Kim (e-mail: yongsang@skku.edu)

ABSTRACT This paper introduces novel driving methods of the pull-down unit in a gate driver circuit for enhancement- and depletion-mode a-IGZO thin-film transistors (TFTs). The proposed gate driver circuit can achieve uniform output characteristics and effectively reduce the V_{OUT} ripple voltage because the threshold voltage (V_{TH}) of the pull-down units is compensated regardless of the a-IGZO TFT operation characteristics (enhancement mode: positive value of V_{TH}, depletion mode: negative value of V_{TH}). Many groups proposed the V_{TH} compensation method for pull-down TFTs in the gate driver circuit using a diode connection structure. However, the diode connection structure to extract the V_{TH} value cannot be applied in the depletion-mode oxide TFTs because TFT enters the turn-on state even when the V_{GS} value is 0 V. To solve this problem, we adopted the V_{TH} extraction period only once in one frame time. As a result, our circuit can compensate for V_{TH} of the pull-down unit in the enhancement mode and can be normally operated in the depletion mode. Adjunctively, two low signals (VGL1 and VGL2) and QC node were designed to prevent the leakage current path for Q and V_{OUT} nodes. To verify the threshold voltage tolerance for various stress conditions, we demonstrated the reliability of the circuit according to the threshold voltage change of the TFTs. The simulation result shows that all the V_{OUT} waveforms are maintained at +28 V (VGH) under the V_{TH} shift conditions from −7 V to +11 V; further, the rising time and falling time are less than 0.62 μs and 0.96 μs, respectively. Based on a 120-Hz ultra-high definition (UHD) graphics (3840×2160) display panel, the proposed circuit has uniform V_{OUT} characteristics compared to previous V_{TH} compensation circuit when ΔV_{TH} changes from −3 V to +11 V. When ΔV_{TH} changes from −4 V to −7 V, there is also no circuit malfunction, even with slight increase in the falling time and power consumption.

INDEX TERMS a-IGZO TFT, gate driver circuit, pull-down unit, enhancement mode, depletion mode, threshold voltage.

I. INTRODUCTION

Amorphous, indium gallium zinc oxide thin-film transistor (a-IGZO TFT) is one of the promising candidates for various next-generation display panels due to high mobility, low off-current level, and high uniformity compared to a-Si:H TFT [1]–[3]. In the IGZO structure, the crystal structure of InO_2 can increase the electron mobility because indium is formed in the 5s orbitals and oxygen is formed in the 2p orbitals in the band structure [4]. In addition, IGZO has a large bandgap, which can transmit the visible light due to its transparent property. Therefore, IGZO has good electrical and optical characteristics [5]–[8].

However, the electrical performance of an IGZO TFT can be degraded by the electrical bias stress or illumination stress by electron trapping in the gate dielectric or at the channel/dielectric interface in inverted stagger type structure [9]. Moreover, the IGZO TFT can be operated in the depletion mode with a negative threshold voltage [10]. When it is applied to an integrated circuit structure, such as the gate driver and pixel compensation circuit, circuit

malfunction can occur due to leakage current path. To solve this problem, many groups proposed gate driver circuits that can be operated in depletion-mode oxide TFTs. Kim *et al.* proposed a new type of gate driver circuit for a depletion-mode a-IGZO TFT [11]. They employed a series-connected two-transistor structure in which a negative voltage can be applied to V_{GS} of the depletion mode a-IGZO TFTs using only one low-power signal (VGL1). The result shows that the proposed circuit exhibited a uniform output pulse without V_{OUT} distortion. However, V_{OUT} malfunction can be also generated by driving capacity of TFTs although leakage current path is prevented by using negative V_{GS} value. In the conventional gate driver circuit structure, pull-down units suffer from performance degradation such as threshold voltage shift due to continuous bias stress [12]. It can directly affect the stability of the gate driver circuit such that output malfunction occurs. Therefore, the threshold voltage compensation structure is required to prevent the pull-down unit degradation. However, a diode connection structure to extract the V_{TH} value cannot be applied in the depletion-mode IGZO TFTs because the TFT enters the turn-on state even when the V_{GS} value is 0 V.

In this paper, we propose novel driving methods of the gate driver circuit for both enhancement- and depletion-mode a-IGZO TFTs. Despite the same circuit structure, the proposed circuit can be operated with different driving methods for the enhancement and depletion modes, respectively. The result shows that the proposed circuit has a large V_{TH} shift margin from -7 V to $+11$ V. Moreover, uniform output characteristics can be obtained because the pull-down units to charge or discharge the V_{OUT} peak voltage have almost the same capability regardless of the V_{TH} conditions.

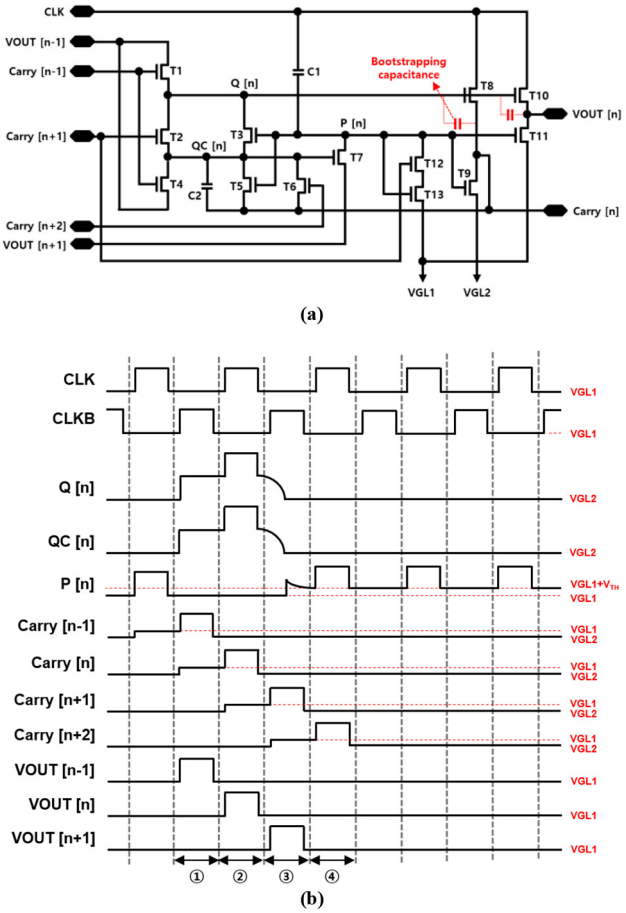

FIGURE 1. Proposed gate driver circuit to realize the novel V_{TH} compensation methods for both enhancement- and depletion-mode a-IGZO TFTs: (a) circuit schematic and (b) timing diagram.

II. PROPOSED GATE DRIVER CIRCUIT AND OPERATION

Fig. 1 shows the schematic for our proposed gate driver circuit for 1 stage, and the voltage timing diagram. The proposed circuit is composed of 13 TFTs, two capacitors, two low-voltage signals (VGL1 and VGL2), and two CLK bus lines (CLK and CLKB). The CLKB signal is used in the n+1 stage instead of CLK to realize V_{OUT} n+1 and Carry n+1 signals. All CLKs and V_{OUT} signals are operated within a swing range from -5 V to $+28$ V. Moreover, Carry signals are operated with the swing range from -13 V to $+28$ V. It has four operation periods, as shown in Fig. 1 (b). For application to the depletion-mode IGZO TFTs, we designed a QC node into the new circuit first [13]. The V_{OUT} degradation can be generated in the depletion-mode IGZO TFTs because the TFT enters the turn-on state even when the V_{GS} value is 0 V. The Q node leakage current paths, which occur in Sections I and II, are three points [T1, T2, and T3 in Fig. 1 (a)]. To solve this problem, the QC node can prevent the leakage current path for Q node because the V_{GS} value of T2 and T3 in the bootstrapping period is less than 0 V, based on the Q node. The leakage current path of T1 can also be eliminated by using Carry n-1 signal ($V_{GS\_T1} = -8$ V). As a result, pre-charging and bootstrapping voltage of the Q node can be respectively maintained by VGH-V_{TH_T1} and VGH-$V_{TH\_T1}+\Delta V$ for both the enhancement- and depletion-mode IGZO TFTs.

Meanwhile, the V_{TH} compensation function of the pull-down units is important in the gate driver circuit because V_{TH} can be varied by electrical bias stress or uniformity standard deviation in the TFT manufacturing process [14]. It means that the discharging capacity for the V_{OUT} node can be changed, which causes nonuniform V_{OUT} characteristics such as falling time, output voltage level, and ripple voltage by CLK [T9 and T11 in Fig. 1 (a)]. To realize outstanding circuit reliability, it is necessary for the V_{TH} compensation structure in the pull-down units to overcome TFT degradation due to continuous bias stress.

Fig. 2 (a) shows the conventional V_{TH} extraction method for the pull-down unit using 3T1C (Ta, Tb, Tc, and C1) circuit configuration [15], [16]. In 3T1C conventional circuit structure, Ta, Tb, and Tc are input TFT, V_{TH} compensation TFT, and pull-down TFT, respectively. Moreover, Ta, Tb, and Tc perform the same functions as T7, T12, and T13, as shown in Fig. 2 (c). The conventional V_{TH} compensation circuit for the pull-down unit should have three CLK signals

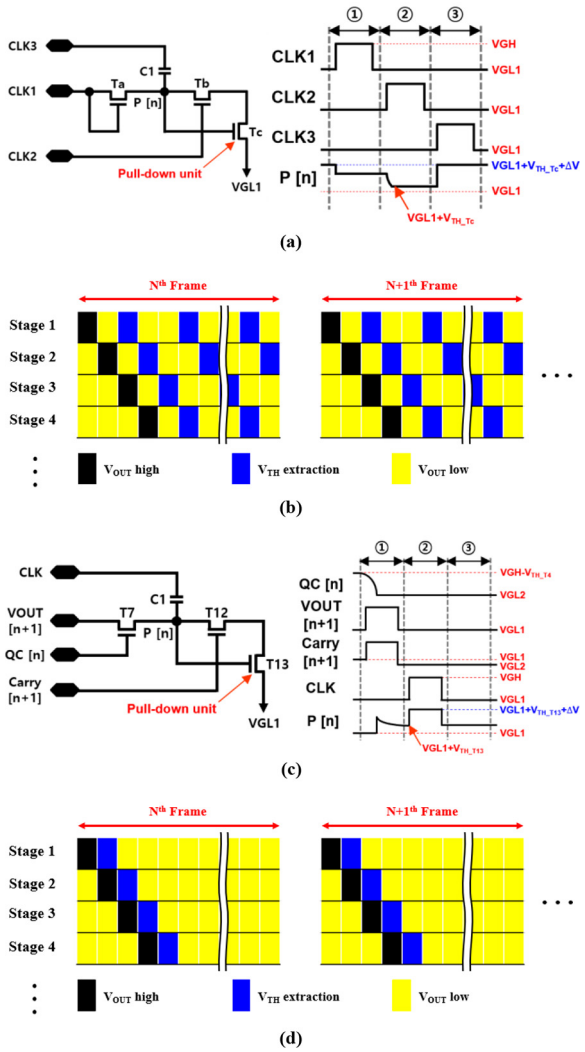

FIGURE 2. **Method of threshold voltage extraction for the pull-down unit: (a) conventional threshold voltage compensation circuit structure and timing diagram, (b) threshold voltage extraction method of conventional circuit, (c) proposed threshold voltage compensation circuit structure and timing diagram, and (d) threshold voltage extraction method of proposed circuit.**

(CLK1, CLK2, and CLK3) because the V_{TH} compensation operation is composed of three parts: initialize period, V_{TH} extraction period, and V_{TH} compensation period, as shown in Fig. 2 (a). When CLK1 has VGH voltage, the P node, which is the gate node of the pull-down unit, is charged by VGH-V_{TH_Ta} in the initialization period of Fig. 2 (a). In the V_{TH} extraction period, Tb is in the turn-on state due to CLK2, which connects the gate-drain node of Tc based on the VGL1 node to extract V_{TH} using the diode connection structure. At this time, C1 can store VGL1+V_{TH_Tc}, which is V_{TH} of the pull-down unit. Moreover, the V_{TH} extraction process is repeated when CLK2 is VGH (blue part: as shown in Fig. 2 (b)), and the V_{TH} compensation (VGL1+V_{TH_Tc}+ΔV) progresses as in Section III. When the depletion-mode IGZO TFT is applied to the conventional V_{TH} compensation circuit structure, the V_{TH} extraction and operation of the pull-down unit are impossible because VGL1 is applied to the P node regardless of CLK1 and CLK2. If the diode connection structure of the pull-down unit is formed by CLK2 (Tb), the V_{GS} value of Tc is 0 V; it means that Tc is continuously in the turn-on state. As a result, the V_{TH} extraction becomes impossible because the P node has the VGL1 voltage.

To solve the V_{TH} extraction problem for the depletion mode IGZO TFTs, we newly designed the extraction time using a similar conventional circuit structure. Fig. 2 (c) and (d) show our proposed V_{TH} compensation circuit structure and V_{TH} extraction method for the depletion-mode IGZO TFTs. In the proposed method, the V_{TH} extraction is only one time based on one frame time. In Section III of Fig. 1 (b), T7, which is the input TFT, is turned on (conventional circuit: Ta) by the QC node and V_{OUT} n+1. Therefore, T13 (conventional circuit: Tc) is in the turn-on state for a short time, which can extract V_{TH} of T13 because T12 (conventional circuit: Tb) is turned on by Carry n+1. At this time, the leakage paths for the P node are not generated because all the V_{GS} values of T7 and T12 are less than 0 V despite V_{GS} of T13 being 0 V. After the V_{TH} extraction time, the V_{TH} compensation and extraction holding are repeated by CLK and C1. As a result, our circuit can compensate V_{TH} of the pull-down unit in the enhancement mode and can be normally operated in the depletion-mode IGZO TFTs. All the operation details are provided in the following four sections.

A. PRE-CHARGE PERIOD

As shown in Section I of Fig. 1 (b), V_{OUT} n-1 and Carry n-1 have VGH voltages. Since T1 and T4 are turned on by Carry n-1, VGH-V_{TH_T1} and VGH-V_{TH_T4} are applied to the Q and QC nodes, respectively. Moreover, VGL1 is applied to the P node through T7 to turn-off T3, T5, T9, T11, and T13. Therefore, the Q and QC node maintains the pre-charging status without any other voltage degradation.

B. BOOTSTRAPPING PERIOD

In Section II, CLK has a VGH voltage. Since the VGH voltage of CLK is applied to the drain of T8 and T10, the Q node of the floating state is bootstrapped by the parasitic capacitance between the gate and drain of T8 and T10. It allows the VGH voltage to be applied to the V_{OUT} n and Carry n signals while the Q node bootstrapping period. It can overdrive T8 and T10, thus preventing the voltage from being lost by the V_{TH} of the pull-up units (T8 and T10). Moreover, the VGH voltage of the Carry n signal can bootstrap the QC node using C2. As a result, the Q node bootstrapping voltage effectively maintains VGH-V_{TH_T1}+ΔV because V_{GS} of T2 and T3 is very low negative value by QC node bootstrapping voltage. Meanwhile, the gate and drain voltages of T1 are VGL2 and VGL1, respectively. It can also prevent the leakage path for the Q node because V_{GS} of T1 has a negative value based on the Q node. A similar operation is performed for the QC node. All V_{GS} of T2, T3, T4, T5, and T6 are less

than 0 V. Therefore, both the Q node and QC node voltages are not degraded despite the depletion-mode operation.

C. RESET & V_{TH} EXTRACTION PERIOD

In Section III, the circuit operation can be divided into two sections; QC node turn-on state and QC node turn-off state. Shortly before the CLK changes from VGH to VGL1, the QC node can drive T7 in order to operate T13 for a while. Since T13 in the turn-on state for a short time, V_{TH} of T13 can be extracted by T12. The Carry n+1 signal is in the turn-on state, which can drive T12 to form the diode connection structure for T13. At this time, VGL1+V_{TH_T13} can be stored in C1. Moreover, when T12 is turned off, V_{GS} of T12 is less than 0 V. Therefore, the extracted V_{TH} value can be maintained in C1 without the voltage degradation. It can be assumed that V_{TH} of T13 is the same value as that of V_{TH} of T9 and T11 because the gate bias stresses for T9, T11, and T13 are almost same due to the P node. Therefore, we can realize the V_{TH} extraction for the pull-down unit regardless of the operation mode for the IGZO TFTs.

D. V_{TH} COMPENSATION PERIOD

In the previous reset and V_{TH} extraction period, the extracted V_{TH} value is stored in the P node using C1. When the CLK signal is changed from VGL1 to VGH after the V_{TH} extraction, the P node voltage is raised by the coupling effect of C1. As a result, the pull-down units of the proposed gate driver circuit effectively discharge the V_{OUT} n and Carry n signals to VGL1 and VGL2 voltages whenever CLK has the VGH voltage. Moreover, the extracted V_{TH} value is continuously conserved by C1 during 1 frame time. It means that the V_{TH} compensation of the pull-down units is successfully performed regardless of the IGZO TFT operation mode because the diode connection is not needed to extract the V_{TH} value except for reset and the V_{TH} extraction period.

III. RESULTS AND DISCUSSIONS

We simulated the operation of the proposed gate driver circuit using the simulation program SmartSpice. The proposed circuit was composed of 13 TFTs and two capacitors. The simulation was performed using the a-IGZO TFT model, as shown in Fig. 3. The transfer characteristics showed that the threshold voltage of the a-IGZO TFT used in the simulation was +0.5 V and the field-effect mobility was 31 $cm^2/V{\cdot}s$.

We used a 120-Hz ultra-high definition (UHD) graphics (3840 × 2160) display panel and set the 1H time (one-line time) and one-frame time to 3 μs and 8.3 ms, respectively. Based on the I-V characteristics of the IGZO TFT, as shown in Fig. 3, we shifted the V_{TH} value in accordance with the TFT operation mode (enhancement mode: positive V_{TH} value and depletion mode: negative V_{TH} value). Table 1 lists the design parameters of the proposed gate driver circuit. To simulate the driving characteristics of the circuit operation, we simulated the last ten stages in a gate driver circuit with 2160 stages. It should be noted that the preceding

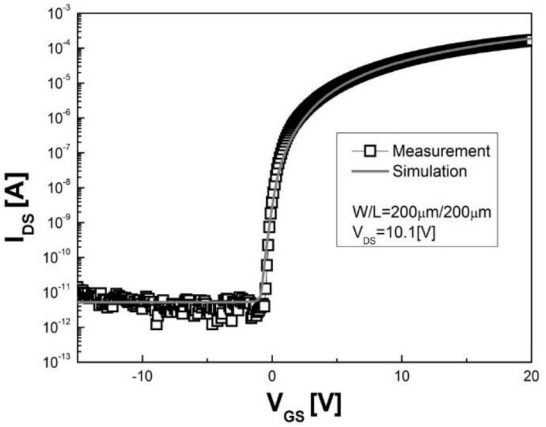

FIGURE 3. Measured and simulated transfer characteristics of a-IGZO TFT.

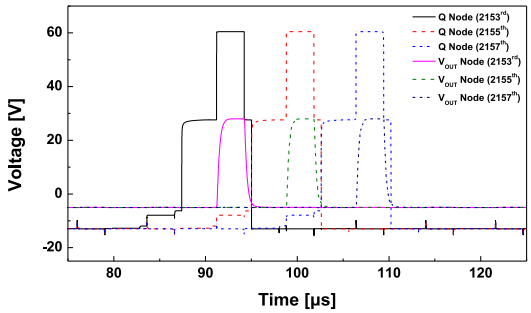

FIGURE 4. The simulated Q node and V_{OUT} node voltage waveforms for 2153rd, 2155th, and 2157th stage (V_{TH} = +0.5 V).

2150 stages were emulated using an equivalent circuit consisting of a resistor and capacitor. Also, we attached a 4-kΩ resistor and a 150-pF capacitor to each V_{OUT} node to emulate the gate line load for the simulation.

Fig. 4 illustrates the simulated Q node and V_{OUT} node voltage waveforms of 2153rd, 2155th, and 2157th stage with a transistor threshold voltage of +0.5 V in the proposed gate driver circuit. At this time, V_{OUT} characteristics are the signals which are applied to the farthest pixel based on the gate driver circuit location (V_{OUT_end}). Thus, we confirm that the Q node voltage is maintained at +27.5 V and +60.5 V in the pre-charge and bootstrapping periods, respectively. In addition, all V_{OUT} voltage waveforms were maintained at +28 V without any voltage degradation and both the rising time (t_r) and falling time (t_f) of the V_{OUT} output from 10% to 90% were 0.57 μs each. Because the ripple voltages for the V_{OUT} node of the 2153rd, 2155th, and 2157th stages were not generated, the stable voltage was supplied to the switch TFT of the pixel circuit without multi-output and voltage degradation. Therefore, this shows that high reliability can be realized through the proposed circuit structure.

To verify the operation characteristics of the enhancement mode and depletion mode IGZO TFTs, we confirmed the Q node, P node, and V_{OUT} characteristics according to the threshold voltage change of TFT through SmartSpice simulation. Fig. 5 shows the simulated voltage waveforms for

TABLE 1. Design parameters of the proposed gate driver circuit.

PROPOSED GATE DRIVER CIRCUIT	
L of all TFTs	5 μm
W of T1 and T2	100 μm
W of T3	5 μm
W of T4 and T13	35 μm
W of T5	130 μm
W of T6	350 μm
W of T7, T9, and T11	500 μm
W of T8	200 μm
W of T10	1000 μm
W of T12	50 μm
C1	3.5 pF
C2	1 pF
CLK Voltage	-5 V ~ +28 V
CLK Duty Ratio	40 %
VGL1	-5 V
VGL2	-13 V
Bootstrap Capacitance (T8)	2.9 fF
Bootstrap Capacitance (T10)	14.5 fF

L = TFT channel length, W = TFT channel width
1 Frame time = 8.3 ms
Frame frequency= 120 Hz (UHD resolution)

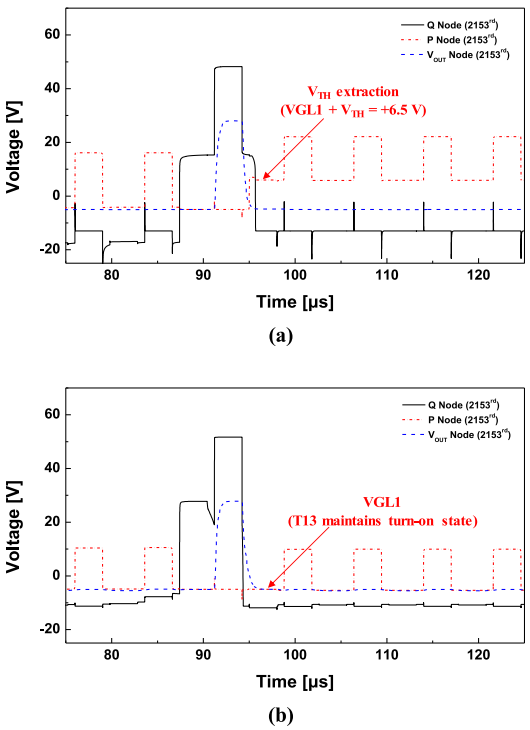

FIGURE 5. The simulated voltage waveforms for both enhancement mode and depletion mode oxide TFTs: (a) $\Delta V_{TH} = +11$ V ($V_{TH} = +11.5$ V) and (b) $\Delta V_{TH} = -7$ V ($V_{TH} = -6.5$ V).

both enhancement mode and depletion mode IGZO TFTs. All the V_{OUT} characteristics mean V_{OUT_end} signals based on the gate driver circuit location. It indicates the application of different operation principles for the negative and positive the threshold voltages of IGZO TFT despite the same circuit structure. Fig. 5 (a) shows the Q node, P node, and V_{OUT} characteristics for the enhancement mode IGZO TFTs. In the proposed circuit, the shift margin of positive V_{TH} is

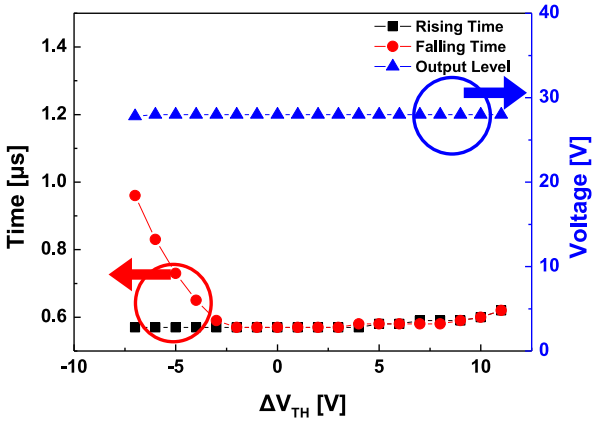

FIGURE 6. 2153rd V_{OUT} output peak voltage, rising time, and falling time characteristics for V_{TH} variations.

+11 V (actual $V_{TH} = +11.5$ V). The result indicates that the extracted V_{TH} of pull-down unit is +11.5 V because the P node voltage is +6.5 V in the V_{TH} extraction period (VGL1 = −5 V). Next, the P node is driven by AC-type depending on the CLK voltage. Therefore, the ripple voltage of the V_{OUT} node can be successfully suppressed by the V_{TH} compensation of the pull-down unit. In addition, V_{OUT} output characteristics show that the output level, rising time, and falling time are +28 V, 0.62 μs, and 0.62 μs, respectively. The rising time and falling time are almost same in the enhancement mode IGZO TFTs because the charging or discharging of the V_{OUT} node is performed by T10, which is the same as the TFT using Q node. Therefore, the proposed circuit can realize uniform output pulse to obtain high reliability. Fig. 5 (b) shows the Q node, P node, and V_{OUT} characteristics for the depletion mode IGZO TFTs. The simulation was performed when the V_{TH} of all TFTs is −7 V (actual $V_{TH} = -6.5$ V), which is the largest negative V_{TH} margin, similar to the enhancement mode. If the VGL2 value is under −13 V, the negative V_{TH} margin can be increased because the voltage difference between VGL1 and VGL2 is −8 V. The result shows that the P node is maintained at −5 V in the V_{TH} extraction period because $V_{GS} = 0$ V for T13. In the reset and V_{TH} extraction period, Q node, QC node, and V_{OUT} reset are performed by T2, T5, and T6, respectively. Therefore, the circuit can be normally driven without any voltage degradation. The V_{OUT} characteristics show that the output level, rising time, and falling time are +27.8 V, 0.57 μs, and 0.96 μs, respectively. Although the output level and falling time degraded slightly, the circuit operation was conducted without any difficulty. Consequently, we can obtain a large V_{TH} tolerance in the proposed circuit under the V_{TH} shift conditions from −7 to +11 V based on the UHD graphics display panel.

Fig. 6 shows the 2153rd V_{OUT} output peak voltage, rising time, and falling time characteristics for V_{TH} variations. Because the V_{TH} tolerance of the proposed circuit varies from −7 to +11 V, as mentioned above, we verified the V_{OUT} characteristics within the V_{TH} shift margin. The result

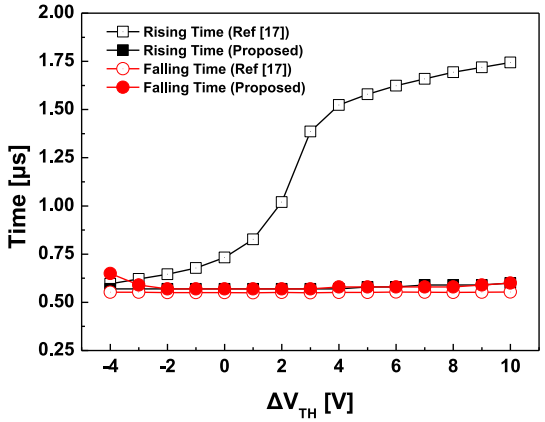

FIGURE 7. Comparison of normalized rising time and falling time between conventional and proposed circuits for the 2153rd stage.

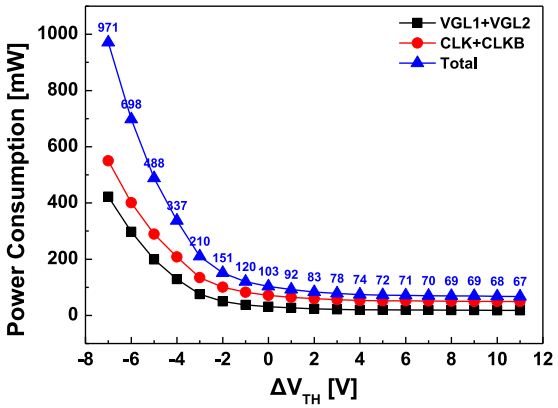

FIGURE 8. Simulation results of power consumption for DC bus line (VGL1 and VGL2) and AC bus line (CLK and CLKB) as a function of threshold voltage shift value.

indicates that the rising time and output level have the same value based on 0 V of ΔV_{TH} (t_r = 0.57 μs, output level = +28 V). When ΔV_{TH} is changed from 0 V to less than -4 V, the falling time increases, as illustrated via the red line in Fig. 6, because the V_{OUT} discharging capacity of T10 is decreased by the voltage of the Q node. However, T11 is in the turned-on state because V_{GS} = 0 V when P node is VGL1. Therefore, the proposed circuit can compensate the V_{TH} of the pull-down unit in the enhancement mode and it can be normally operated in the depletion mode.

Fig. 7 indicates the comparison of normalized rising time and falling time between the conventional and proposed circuits for the 2153rd stage. Seo *et al.* proposed a robust gate driver circuit capable of compensating the threshold voltage shift of oxide TFTs irrespective of the enhancement and depletion modes [17]. The conventional circuit ensures the robust operation over a wide range of threshold voltage shifts, varying from −4 to +10 V. To evaluate the V_{OUT} characteristics of the proposed circuit using the conventional circuit, similar simulation conditions are considered (RC load of CLK and V_{OUT}, voltage level, and 1H time). The result shows that the normalized rising time and falling time changed by 137.9% (ΔV_{TH} = +10 V) and 18.7% (ΔV_{TH} = −4 V) in the conventional circuit, respectively, as shown in Fig. 7, because the structure of the conventional circuit uses the pull-down unit over-driving method to obtain the V_{TH} shift margin. However, when V_{TH} is shifted, the rising time can be changed because it can be affected by all values of the Q node pre-charge and bootstrapping voltages. The proposed circuit, meanwhile, can relatively obtain uniform V_{OUT} characteristics as well as V_{TH} compensation.

Fig. 8 shows the simulation results of the power consumption for the DC bus line (VGL1 and VGL2) and AC bus line (CLK and CLKB) as a function of threshold voltage shift values. When the TFT is operated by the depletion mode, leakage current is generated in T8 (CLK), T9 (VGL2), and T11 (VGL1). Therefore, the power consumption in the DC and AC lines gradually increases as the negative V_{TH} shift value increases. The total power consumption is 102.62 mW when the V_{TH} has its initial value. Also, power consumption gradually decreases when positive V_{TH} shift value increases. It means that abnormal circuit operation is not observed even though V_{TH} is shifted by +11 V because power consumption caused by leakage path is not generated.

IV. CONCLUSION

In this work, we proposed novel driving methods for the pull-down unit in the gate driver circuit for both enhancement and depletion modes a-IGZO TFTs. To realize high circuit reliability, it is necessary to adopt a V_{TH} compensation structure for pull-down units. However, a diode connection structure to compensate V_{TH} for pull-down units cannot be operated in the depletion mode IGZO TFTs because V_{GS} = 0 V. Moreover, three or more CLK bus lines are required in the V_{TH} compensation structure. To solve this problem, we adopted the V_{TH} extraction period once for each frame time. Consequently, the proposed circuit was found to compensate the V_{TH} of the pull-down unit in enhancement mode and can be normally operated in the depletion mode. We verified the reliability of the circuit according to the threshold voltage change in the TFTs. The simulation result shows that all V_{OUT} waveforms were maintained at +28 V under the V_{TH} shift conditions varying from −7 to +11 V. Additionally, the rising time and falling time were found to be lesser than 0.62 and 0.96 μs, respectively. Based on the 120-Hz UHD graphics (3840 × 2160) display panel, the proposed circuit was found to exhibit uniform V_{OUT} characteristics as compared to the previous V_{TH} compensation circuit where ΔV_{TH} varied from −3 to +11 V. When ΔV_{TH} varied from −4 to −7 V, no circuit malfunction was observed even if the falling time and power consumption were slightly increased.

REFERENCES

[1] T. Kamiya, K. Nomura, and H. Hosono, "Origins of high mobility and low operation voltage of amorphous oxide TFTs: Electronic structure, electron transport, defects and doping," *J. Display Technol.*, vol. 5, no. 12, pp. 468–483, 2009.

[2] J.-H. Kim *et al.*, "Bias and illumination instability analysis of solution-processed a-InGaZnO thin-film transistors with different component ratios," *Thin Solid Films*, vol. 645, pp. 154–159, Jan. 2018.

[3] J. H. Na, M. Kitamura, and Y. Arakawa, "High field-effect mobility amorphous InGaZnO transistors with aluminum electrodes," *Appl. Phys. Lett.*, vol. 93, no. 6, 2008, Art. no. 063501.
[4] G. H. Kim, B. D. Ahn, H. S. Shin, W. H. Jeong, H. J. Kim, and H. J. Kim, "Effect of indium composition ratio on solution-processed nanocrystalline InGaZnO thin film transistors," *Appl. Phys. Lett.*, vol. 94, no. 23, 2009, Art. no. 233501.
[5] G. J. Lee, J. Kim, J.-H. Kim, S. M. Jeong, J. E. Jang, and J. Jeong, "High performance, transparent a-IGZO TFTs on a flexible thin glass substrate," *Semicond. Sci. Technol.*, vol. 29, no. 3, 2014, Art. no. 035003.
[6] C.-W. Chien *et al.*, "High-performance flexible a-IGZO TFTs adopting stacked electrodes and transparent polyimide-based nanocomposite substrates," *IEEE Trans. Electron Devices*, vol. 58, no. 5, pp. 1440–1446, May 2011.
[7] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488–492, 2004.
[8] E. Fortunato, P. Barquinha, and R. Martins, "Oxide semiconductor thin-film transistors: A review of recent advances," *Adv. Mater.*, vol. 24, no. 22, pp. 2945–2986, 2012.
[9] T.-C. Chen *et al.*, "Investigating the degradation behavior caused by charge trapping effect under DC and AC gate-bias stress for InGaZnO thin film transistor," *Appl. Phys. Lett.*, vol. 99, no. 2, 2011, Art. no. 022104.
[10] B. Kim *et al.*, "New depletion-mode IGZO TFT shift register," *IEEE Electron Device Lett.*, vol. 32, no. 2, pp. 158–160, Feb. 2011.
[11] B. Kim *et al.*, "A depletion-mode a-IGZO TFT shift register with a single low-voltage-level power signal," *IEEE Electron Device Lett.*, vol. 32, no. 8, pp. 1092–1094, Aug. 2011.
[12] C.-L. Lin, C.-D. Tu, C.-E. Wu, C.-C. Hung, K.-J. Gan, and K.-W. Chou, "Low-power gate driver circuit for TFT-LCD application," *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1410–1415, May 2012.
[13] J.-H. Kim, J. Oh, K. Park, and Y.-S. Kim, "IGZO TFT gate driver circuit with large threshold voltage margin," *Displays*, vol. 53, pp. 1–7, Jul. 2018.
[14] J.-M. Lee, I.-T. Cho, J.-H. Lee, and H.-I. Kwon, "Bias-stress-induced stretched-exponential time dependence of threshold voltage shift in InGaZnO thin film transistors," *Appl. Phys. Lett.*, vol. 93, no. 9, 2008, Art. no. 093504.
[15] C.-L. Lin and Y.-C. Chen, "A novel LTPS-TFT pixel circuit compensating for TFT threshold-voltage shift and OLED degradation for AMOLED," *IEEE Electron Device Lett.*, vol. 28, no. 2, pp. 129–131, Feb. 2007.
[16] Z. Hu *et al.*, "TFT integrated gate driver with V_{TH} shift compensable low-level holding unit," in *SID Symp. Dig. Tech. Papers*, vol. 47. San Francisco, CA, USA, 2016, pp. 134–137.
[17] J. Seo, S.-J. Song, D. Kim, and H. Nam, "Robust low power DC-type shift register circuit capable of compensating threshold voltage shift of oxide TFTs," *Displays*, vol. 49, pp. 65–71, Sep. 2017.

JONGSU OH received the Diploma degree in information and communication engineering from Sungkyunkwan University, Suwon, South Korea, in 2015, where he is currently pursuing the Doctoral degree with the Nano Electronics and Microfluidic Sensors Laboratory. His current research interests include LTPS/oxide semiconductors, flexible thin-film transistors, and gate driver circuits.

KYUNG-MO JUNG is currently pursuing the master's degree with the Nano Electronics and Microfluidic Sensors Laboratory, Sungkyunkwan University, Suwon, South Korea. His current research includes the fabrication and characterization of oxide semiconductors, and flexible thin-film transistors.

EUN KYO JUNG is currently pursuing the master's degree with the Nano Electronics and Microfluidic Sensors Laboratory, Sungkyunkwan University, Suwon, South Korea. His current research interests include the design and analysis of gate driver circuits and pixel circuits.

JUNGWOO LEE is currently pursuing the master's degree with the Nano Electronics and Microfluidic Sensors Laboratory, Sungkyunkwan University, Suwon, South Korea. Her current research interests include oxide semiconductors, gate driver circuit, and pixel circuit.

SOO-YEON LEE received the B.S. and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 2009 and 2013, respectively. She worked as a Senior Engineer with Samsung Display from 2013 to 2019. Since 2019, she has been an Assistant Professor with Seoul National University. Her major areas of research include device analysis using MATLAB and TCAD and AMOLED compensation pixel circuit design for simultaneous emission driving.

KEECHAN PARK received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1997, 1999, and 2003, respectively. He worked as a Senior Engineer with Samsung Electronics from 2003 to 2007. Since 2007, he has been a Professor with Konkuk University. His research areas include the design of display panels, circuit integration using TFTs, and device characterization.

JAE-HONG JEON received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1995, 1997, and 2001, respectively. He worked as a Senior Engineer with Samsung Electronics from 2001 to 2005. He is currently a Professor with Korea Aerospace University. His research areas include the stability of thin film devices and circuits for display panels.

YONG-SANG KIM received the B.S. and Ph.D. degrees in electrical engineering from Seoul National University in 1988 and 1994, respectively. Since 2013, he has been a Professor with the Department of Electrical and Computer Engineering, Sungkyunkwan University. He was also a Professor with Myongji University from 1995 to 2013. He is currently the Director of the Nano Electronics and Microfluidic Sensor Laboratory, Sungkyunkwan University, where he has several research works focused on oxide TFTs, transistor-based biosensor, organic solar cells and solution-processing technologies for organic electronic devices. His research interests include the design, fabrication and characterization of AMLCD and AMOLED TFT Backplane with a-Si:H TFTs, a-IGZO TFTs, and LTPS TFTs, also through numerical simulation using TCAD and SmartSpice. Another specific topic in his research activities involves the gate scan driver circuit for display backplane and compensation circuit for AMOLED pixel circuit design.