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Fabrication of CMOS Invertors in Si Thin-Film-Transistors by Laser Doping Using a Chemical Solution Coating

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ABSTRACT We demonstrated that p- and n-type activation layers can be formed in Si films by laser doping with H_3PO_4 solution and Al_2O_3 sol coating. The phosphorus and aluminum concentrations at the laser doped region were found to be over 10^{19} cm^{-3} in Si films. In addition, generations of the activation carriers for n- and p-type layers were confirmed by Hall effects measurement. In this study, the characteristic of CMOS invertors fabricated by laser doping are presented.

INDEX TERMS Low temperature poly Si (LTPS), thin-film-transistor (TFT), excimer laser annealing (ELA), laser doping, chemical solution coating.

I. INTRODUCTION

Low-temperature poly-Si (LTPS) thin-film transistors (TFTs) have attracted significant attention as devices with high definition for flat panel displays (FPDs). An additional benefit of using LTPS is that CMOS circuits can be formed on substrates such as glass and even plastics for peripheral logic circuits on the panel. Several techniques for creating LTPS thin films have been developed so far. In particular, excimer laser annealing (ELA) is recognized as a promising process that enables the crystallization of amorphous Si (a-Si) at low temperature without any damages to substrates, and it is commercially applied for manufacturing liquid crystal displays (LCDs) and organic light-emitting diodes (OLEDs) [1]–[3].

However, one issue remains with regard to LTPS TFT fabrication. The ion implantation and high-temperature annealing (~500 °C) processes, which are used in creating source/drain contacts for TFTs, can't be applied for flexible substrates due to their heat resistances only up to ~300 °C [4]. Recently, laser doping has been studied in order to achieve a simplified and cost-effective process without using high-temperatures. Various laser doping methods have been reported, for example, gas immersion laser doping (GILD) in a dopant gas ambient (i.e., BF_3, or PF_5) [5]–[6], laser doping based on the ablation of Al_2O_3 thin films deposited on the substrate [7], and laser doping with phosphosilicate (PSG) or borosilicate glass (BSG) [8]–[9]. These doping methods have been studied mainly for creating pn junctions in solar cells.

In our previous study, phosphorus was doped onto Si films immersed in H_3PO_4 solution by laser doping, and a phosphorus concentration of over 10^{19} cm^{-3} was confirmed [10]. Moreover, a H_3PO_4 solution coating process was established to prevent the generation of bubbles, which led to optical scattering during irradiation [11]. In particular, formation of low-resistance in-source/drain contacts is required in TFTs for good electrical properties. The laser doping method involving a coating process is expected to meet the above requirements at low temperature and costs.

With regard to laser light sources, the KrF excimer laser has several advantages in laser doping owing to its short wavelength of 248 nm. These advantages include a high absorption rate of Si (~10^6 cm^{-1}) and high energy efficiency that induces complete melting even at a short pulse wave (~ns). The diffusion coefficient of phosphorus in liquid-phase Si is much higher (10^{-4}–10^{-3} cm^2/s) than that

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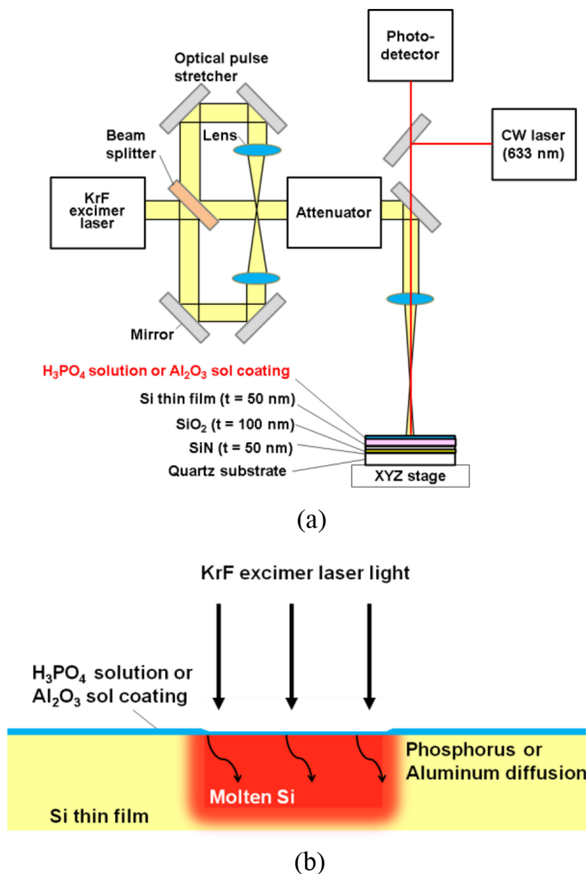


FIGURE 1. (a) Schematic of excimer-laser doping setup and in-situ observation system. (b) Concept of the phosphorus or aluminum doping of Si films by laser irradiation.

of solid-phase Si (10^{-12}–10^{-10} cm^2/s) [12]. It was also reported that phosphorus and boron dopants were diffused and incorporated into crystalline Si using a Nd:YAG laser of 355 nm [13]. In this study, we propose a notable doping method using a KrF excimer laser with a coating of H_3PO_4 solution (n-type) and Al_2O_3 sol (p-type) in order to form source/drain contacts in n- and p-MOS TFTs for CMOS LTPS TFT fabrication, including the laser crystallization of a-Si films.

II. EXPERIMENTAL METHODS

A. LASER DOPING SYSTEM

Figure 1 (a) shows a schematic of the KrF-excimer laser [Gigaphoton, Inc., wavelength: 248 nm, pulse duration (full width at half-maximum (FWHM): 10 ns] doping system. An optical delay system was used in this setup for optimized laser crystallization. The shot repetition rate of the laser was 100 Hz, whereas the spot size on the surface of the sample was 800 μm × 500 μm. The sample was scanned in the short-axis direction of the laser beam; the number of laser shots was fixed at 20 per location. Figure 1 (b) shows a concept of laser doping of Si film with H_3PO_4 solution or Al_2O_3 sol coating. Phosphorus in H_3PO_4 solution or aluminum in Al_2O_3 sol diffuse into molten Si irradiated with KrF excimer laser. H_3PO_4 solution or Al_2O_3 sol was coated on the surface of Si films as following steps: Initially, the laser crystallization was conducted at a fluence of 400 mJ/cm^2 and 20 shots. (1) diluted-hydrofluoric-acid cleaning (10 s), (2) pure-water cleaning, (3) ultraviolet (UV) treatment (10 s), (4) dipping into H_3PO_4 solution or Al_2O_3 sol (10 s), and (5) pure-water cleaning (10 s). The UV treatment in step 3 was performed using KrF excimer laser irradiation (100 mJ/cm^2 and 20 shots). This UV laser treatment enhanced the hydrophilicity of the surface of the a-Si film. The reason why 100 mJ/cm^2 and 20 shots were selected for the UV treatment was to induce surface oxidation and hydrophilic of Si without melting. The pure-water cleaning in step 5 removed any excess H_3PO_4 solution or Al_2O_3 sol. A continuous-wave (CW) laser with a wavelength of 633 nm was used to probe the center of the region irradiated by the KrF excimer laser. The reflected probe light from the poly-Si surface was monitored using a photo-detector during laser irradiation.

After the doping process, the specific resistivity, depth profiles of the phosphorus and aluminum concentrations, carrier concentration, and Hall mobility were measured. The specific resistivity was determined from the sheet resistance (measured by a four-point probe) and the film thickness (50 nm). The phosphorus and aluminum depth profiles were measured using secondary-ion mass spectrometry (SIMS); in addition, the contact resistivity of the doped Si was investigated with Al/Ti electrodes using the transmission line model (TLM). Finally, we report the characteristics of n-MOS, p-MOS, and CMOS TFTs fabricated by laser doping.

B. TFT FABRICATION

Figure 2 shows a schematic of the top-gate transistor fabrication process. The process flow is as follows. First, a-Si (50 nm) films were deposited onto a quartz substrate by low-pressure CVD at 550 °C. Subsequently, ELA was conducted in a fluence range of 400 mJ/cm^2 and 20 shots. The crystallization of 400 mJ/cm^2 and 20 shots was optimized for largest crystal grain size from scanning electron microscope (SEM) image at irradiated region. After laser irradiation and poly-crystallization, the Si film was patterned by photolithography and wet etched with a mixture of HF, HNO_3, and H_2O. For the gate insulator, a SiO_2 film (100 nm) was deposited, and contact holes were opened at the source/drain regions with buffered HF. The coating process progressed with H_3PO_4 solution or Al_2O_3 sol, and laser doping at 400 mJ/cm^2 and 20 shots was performed.

The SiO_2 film pattern was used for local doping only to the source/drain, thus preventing doping of the channel region. Then, the gate insulator of the SiO_2 film was removed with buffered HF. The SiO_2 film was re-deposited, and a TiN (150 nm) electrode film was deposited and patterned. Next, a dielectric film of SiO_2 (∼200 nm) was deposited by atmospheric pressure CVD at 400 °C. The contact holes were opened by wet etching, and the contact metal of the Al

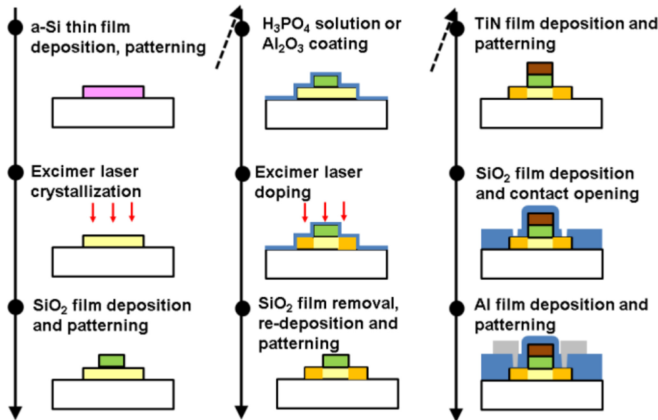


FIGURE 2. Schematics of top-gate transistor fabrication process by laser doping with coating of chemical solution.

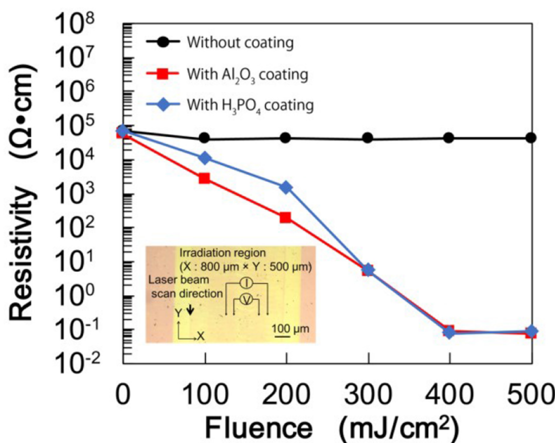


FIGURE 3. Resistivity of Si doped with H_3PO_4 solution coating (blue line) and Al_2O_3 sol coating (red line) up to 500 mJ/cm^2 and 20 shots.

films was deposited and patterned. The H_2 sintering was performed at 400 °C for 0.5 h.

III. RESULTS

Figure 3 shows the specific resistivity of the Si doped with H_3PO_4 solution coating (blue line) and Al_2O_3 sol coating (red line) at different fluences up to 500 mJ/cm^2 and 20 shots. At first, surface cleaning with HF solution of 1% and laser annealing and poly-crystallization were carried out at a fluence of 400 mJ/cm^2 and 20 shots, with scanning in the short-axis direction. The resistivity decreased as the laser fluence increased. Finally, a minimum resistivity value of ∼0.08 Ω ·cm was observed at a doping condition of 400 mJ/cm^2 and 20 shots in both solution coatings. Ohmic contacts were also confirmed with tungsten probes, which indicated that the conductive layer was formed. It is known that a lower specific resistivity corresponds to a higher dopant concentration [14]. Thus, these results show that phosphorus and aluminum were incorporated into the Si film by laser irradiation. As previously reported, we actually observed the reflectance and melting condition of Si during irradiation by employing in-situ monitoring based on a 633 nm CW laser [11]. It is thought that laser doping is a phenomenon derived from the melting of Si, and complete melt of Si was seen at the fluence of 400 mJ/cm^2. The temperature of ∼1400 °C at the maximum was estimated on the surface based on temperature simulations of Si films irradiated with one pulse at a fluence of 400 mJ/cm^2, and this was sufficient for the melting of Si. The resistivity of the laser-doped region without any coatings was measured for comparison, and the resistivity showed no changes despite the laser fluence. This result indicated that the H_3PO_4 and Al_2O_3 coatings actually contributed to the low resistivity.

Figure 4 (a) and (b) show the phosphorus and aluminum depth profiles measured by SIMS for the irradiated areas of 400 mJ/cm^2 and 20 shots. The phosphorus and aluminum concentrations in the Si films were found to be uniform (over 10^{19} cm^{-3}). These concentrations are equivalent to an ion dose of $\sim 10^{14}$ cm^{-2}. This value is reasonable or small for contact formation in TFTs since the dose level is required to be approximately 10^{14}–10^{15} cm^{-2} for ion implantation. A longer pulse duration or increased shot number might provide a higher impurity concentration because these are also thought to be effective parameters [15]. The oxygen over 10^{21} cm^{-3} was also measured at the Si surface of doped regions. This is possibly attributes to surface oxidation of Si induced by laser irradiation.

We also measured the aluminum depth profile in un-doped region for comparison. As shown in figure 4 (c), the aluminum concentration showed almost background level. This indicated that aluminum was incorporated into Si by laser irradiation.

The Hall mobility (μ) of the Si films after laser doping was found to be 61 cm^2/Vs (at the H_3PO_4 condition) and 13 cm^2/Vs (at the Al_2O_3 condition) at 400 mJ/cm^2 and 20 shots based on the Van der Pauw method [16]. This means that activated dopants were generated by laser doping. Additionally, either an n-type or p-type layer was distinguished from the gradient of IV linear. The carrier concentrations (n) calculated by Hall measurements were 1.5×10^{18} cm^{-3} (at the H_3PO_4 condition) and 8.9×10^{18} cm^{-3} (at the Al_2O_3 condition). This is one order of magnitude smaller than the impurity concentrations. The most probable reason for this is that carrier traps were produced by the laser irradiation and crystal defects. As reported earlier, carriers tend to be captured in trapping sites at the grain boundaries [17], [18]. We also measured the contact resistivity between the doped region and Ti/Al electrodes by the TLM method. Resistivity of 8.5×10^{-5} Ω·cm^2 and 1.8×10^{-3} Ω·cm^2 were obtained for laser doping of 400 mJ/cm^2 and 20 shots with H_3PO_4 solution coating and Al_2O_3 solution coating, respectively. It is generally said that the allowable contact resistivity is approximately 10^{-6} Ω·cm^2 [19]. We think that a higher active doping density and lower metal-semiconductor barrier height are required for lower contact resistivity.

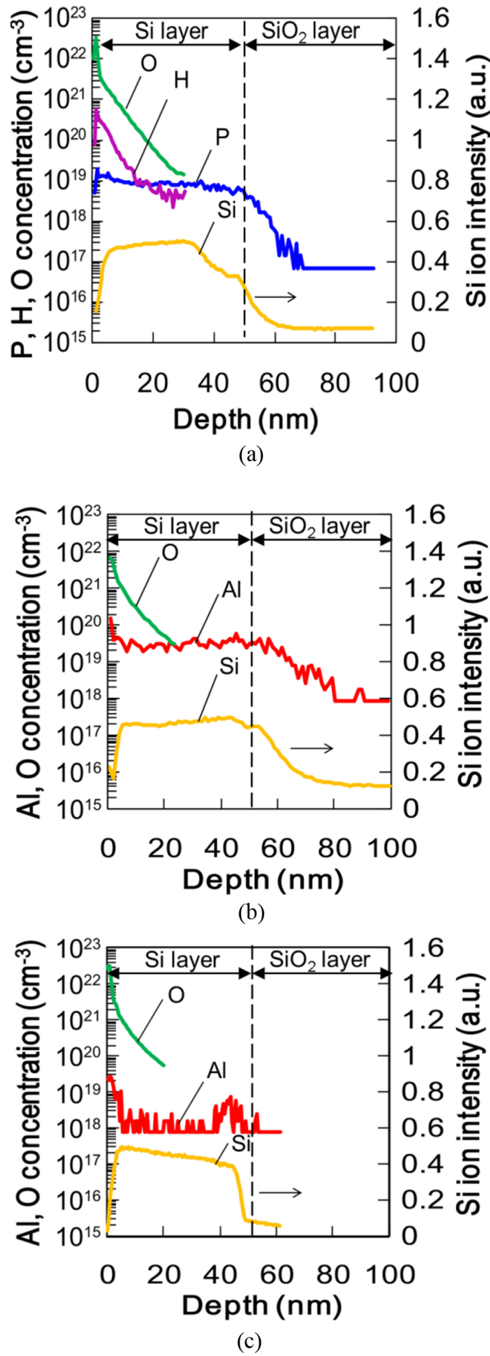


FIGURE 4. Phosphorus (a) and aluminum (b) depth profiles in laser -doped region irradiated with fluence of 400 mJ/cm² and 20 shots. (c) Aluminum depth profile in un-doped region for comparison.

Figure 5 (a)-(d) show the transfer curves [drain current (I_D)-gate voltage (V_G) and I_D-drain voltage (V_D)characteristics] of the n- and p-MOS TFTs fabricated by laser doping with H_3PO_4 solution (n-MOS) and Al_2O_3 sol (p-MOS) at the condition of 400 mJ/cm^2 and 20 shots. The laser doping of 400 mJ/cm^2 and 20 shots was optimized for lowest resistivity. The gate length (L) was 20 μm, and the width (W) was 30 μm. A V_D of 15 V for the n-MOS TFT and −15 V for the p-MOS TFT were applied to the

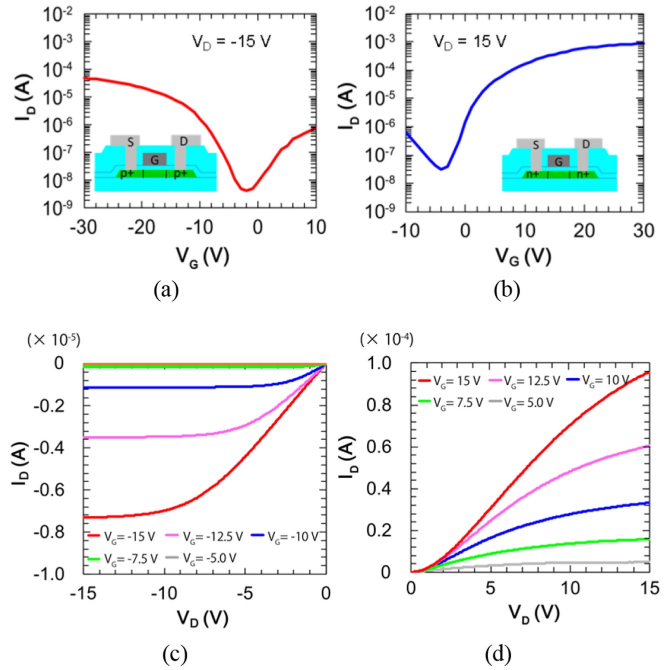


FIGURE 5. $I_D - V_G$ curves for p-MOS TFT at $V_D = -15$ V (a) and n-MOS TFT at $V_D = 15$ V (b) fabricated with fluence of 400 mJ/cm² and 20 shots. $I_D - V_D$ curves for p-MOS TFT from −15 V to −5 V of V_D (c) and n-MOS TFT from 5 V to 15 V of V_D (d).

I_D–V_G curves. From the I_D–V_G curves in Fig. 5(a) and (b), it is clear that on/off operations of TFTs with the changes in gate voltage were successfully obtained in both chemical coating conditions. Here, the field-effect mobility (μ_{FE}) in the saturated region is based on the transfer curves. The equation for μ_{FE} is as follows:

$$\mu_{FE} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_D}}{\partial V_D}\right)^2 \tag{1}$$

where C_i is the gate oxide capacitance (3.5 × 10^{-8} F/cm^2). The μ_{FE} was found to be 64 cm^2/Vs for the n-MOS transistor and 8 cm^2/Vs for the p-MOS transistor at the maximum.

As shown in Fig. 5(c) and (d), the I_D–V_D curves for n- and p-MOS TFTs show good following performance with increasing gate voltage. The threshold voltages (V_{th}) and sub-threshold swings (SS) were −1.0 V and 1.65 V/dec for the n-MOS TFT, −7.0 V and 2.1 V/dec for the p-MOS TFT, respectively. The drain current of the n-MOS TFT was greater by a degree of magnitude than that of the p-MOS TFT. This is also seen in Si single-crystal MOSFETs and is probably attributed to the difference in properties between electron and hole carriers [20]. Therefore, a larger channel region is required for a p-MOS TFT in order to achieve better CMOS operation. The average standard deviation of field effect mobility fabricated by laser doping method were 47 cm^2/Vs and 20 % for n-type TFTs (N=8), and 5.3 cm^2/Vs and 22 % for p-type TFTs (N=8). We also evaluated the TFTs fabricated by ion implantation (ion source : As+ (n-type), energy : 140 keV, dose level : 5×10^{15} cm^2) and high temperature annealing (550 °C, 1h), and the average and

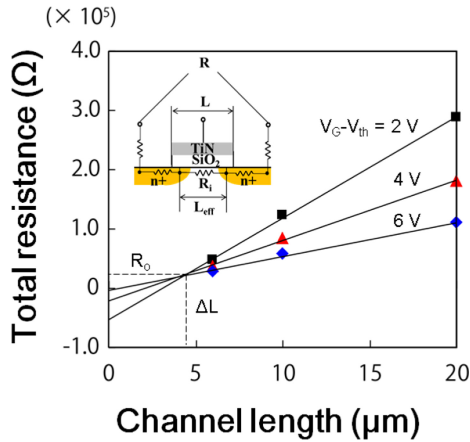


FIGURE 6. Total channel resistance *R* vs. channel length *L* (= 6 μm, 10 μm, and 20 μm) for n-MOS TFT.

standard deviation of field effect mobility were 41 cm^2/Vs and 17 % (N=8). This result shows that the performance of laser doped TFTs was reasonable.

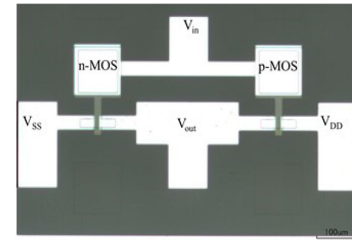
We investigated the effective channel length L_{eff} for n-MOS TFT at the laser-doped of 400 mJ/cm^2 and 20 shots to evaluate the influence of lateral diffusion of phosphorus dopants. Figure 6 shows the measured total resistance R changing the channel length L of 6 μm, 10 μm and 20 μm applying various bias voltages of $V_G - V_{th} = 2$ V, 4 V, and 6 V. Here, the total resistance R and the effective channel length L_{eff} are given by: [21]

$$R = R_i + R_o \tag{2}$$

$$L_{eff} = \Delta L + L \tag{3}$$

where R_i is an intrinsic channel resistance and R_o is an extrinsic resistance including all other resistance. The ΔL is the parameter caused by source/drain diffusion, and can be determined from the intersection point of R-L linear as shown in figure 6. The ΔL was assumed to be – 4.1 μm. Therefore, in the case of $L = 20$ μm, the L_{eff} is calculated to be 15.9 μm. This L_{eff} is very significant in fabrication of short channel TFTs. The R_o was found to be 19.5 kΩ from the R-L relations, and the R_i was calculated to be 1.1 kΩ, indicating that the extrinsic resistance is dominant parameter in source/drain resistance.

Figure 7(a) shows an optical microscopy image of the CMOS TFT composed of n-MOS and p-MOS fabricated by laser doping at the condition of 400 mJ/cm^2 and 20 shots. The gate electrodes were connected for the input voltage (V_{in}) with Al. The source of n-MOS and the drain of p-MOS were connected with Al for the output voltage (V_{out}). Figure 7 (b) shows schematics of CMOS TFT fabrication process by laser doping with coating of chemical solution. Figure 7(c) shows the transient of the $V_{in} - V_{out}$ characterization at $V_{DD} = 15$ V and $V_{SS} = 0$ V. We used a function generator for input signals with the square-wave amplitude of 15 V peak-to-peak and a frequency of 100 Hz. It was revealed that the V_{out} signal changed to a high-level voltage of 13.5 V when V_{in} was 0 V, including inverted V_{in} waves when V_{in} was 15 V. The reason that the maximum voltage differs between the V_{in} and V_{out} might be attributed to the off-current of n-MOS TFT.



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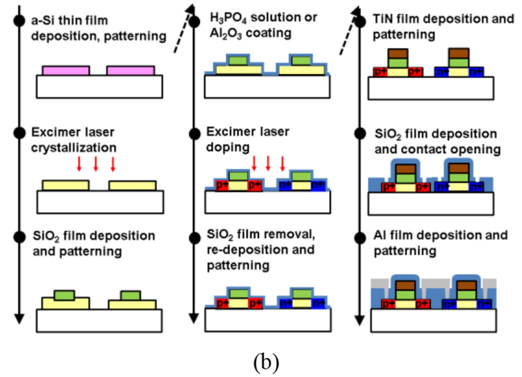
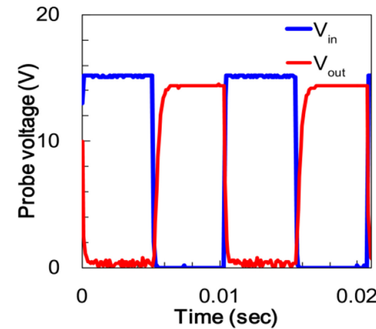
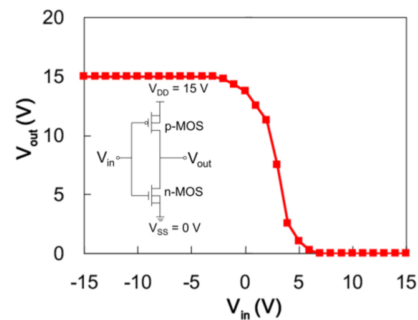


(b)



(c)



(d)

FIGURE 7. (a) Optical microscopy image of CMOS inverter. (b) Schematics of CMOS TFT fabrication process by laser doping with coating of chemical solution. (c) Transient characteristics for inverter applying V_{in} amplitude of peak-to-peak at 15 V and frequency 100 Hz at V_{DD} = 15 V and V_{SS} = 0 V. (d) V_{in}-V_{out} characteristics for inverter with V_{in} ranging from −15 V to 15 V.

Figure 7(d) shows the typical V_{in}-V_{out}characteristics of the CMOS inverter. The inverter characteristic with rail-to-rail operation was observed. One of the significant performance indicators for CMOS inverters is low power consumption. Therefore, a low off-current of LTPS TFTs of ∼pA is required. As recognized in the conventional process of LTPS TFTs, the high electric-field concentration in the termination of the source/drain may lead to a high off-current even in the laser doping process. The formation of a channel offset region or multiple gate structure relaxing the electric field would be effective toward solving this problem [22]. The laser doping method is an advanced technology for controlling the dopant concentration and depth profiles. Therefore, it is possible to form the lightly doped drain (LDD) structure in a channel region for LTPS TFTs [23].

IV. CONCLUSION

In conclusion, we demonstrated that dopant implantation and activation can be simultaneously performed using KrF excimer laser irradiation with the melt of Si thin films coated with H_3PO_4 solution and Al_2O_3 sol. High phosphorus and aluminum concentrations over 10^{19} cm^{-3} were observed in Si films. Additionally, we presented n- and p-MOS TFT operations with reasonable field effect mobility. The details of TFT performance and related characteristics are not completely clear, and we are investigating the relationships between laser parameters (laser fluence and shot number) and TFT performances (mobility and threshold voltage). The proposed laser doping method will be cost-effective and contributive not only for displays but also various applications such as NAND flash memories, SRAMs (Static Random Access Memories), and image sensors.

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REFERENCES

[1] T. Goto *et al.*, “LTPS thin-film transistors fabricated using new selective laser annealing system,” *IEEE Trans. Electron Devices*, vol. 65, no. 8, pp. 3250–3256, Aug. 2018.

[2] K. Imokawa *et al.*, “Novel and highly reliable XeF and KrF excimer laser annealing for reducing the cost of flat panel display equipment,” *J. SID*, vol. 48, no. 1, pp. 1532–1535, 2017.

[3] P. C. van der Wilt, “Excimer-laser annealing: Microstructure evolution and a novel characterization technique,” in *Proc. SID*, 2014, pp. 149–152.

[4] T. Sameshima, N. Andoh, and Y. Andoh, “Activation behavior of boron and phosphorus atoms implanted in polycrystalline silicon films by heat treatment at 250°C,” *Jpn. J. Appl. Phys.*, vol. 44, no. 3, p. 1186, 2005.

[5] G. K. Giust and T. W. Sigmon, “Self-aligned aluminum top-gate polysilicon thin-film transistors fabricated using laser recrystallization and gas-immersion laser doping,” *IEEE Electron Device Lett.*, vol. 18, no. 8, pp. 394–396, Aug. 1997.

[6] J. Boyce *et al.*, “Laser doping and crystallization of amorphous silicon thin films,” in *Proc. Mater. Res. Soc.*, vol. 358, 1994, p. 909.

[7] D. Walter, A. Fell, M. Ernst, E. Franklin, and K. Weber, “Electronic properties of Al p^+ surfaces formed by laser doping from aluminium oxide precursors: Implications for PERC cell design and performance,” *Energy Procedia*, vol. 77, pp. 321–330, Aug. 2015.

[8] C. Kim, S. Jung, J. Jeon, and M. Han, “Low temperature laser-doping process using PSG and BSG films for poly-Si TFTs,” in *Proc. Mater. Res. Soc. (MRS)*, vol. 621, 2000, pp. Q8.4.1–Q8.4.5.

[9] S. Fernandez-Robledo, S. Kluska, J. Greulich, and J. Nekarda, “Selective boron emitters using laser-induced forward transfer versus laser doping from borosilicate glass,” *IEEE J. Photovolt.*, vol. 7, no. 5, pp. 1254–1263, Sep. 2017.

[10] A. Suwa, N. Tanaka, T. Sadoh, D. Nakamura, and H. Ikenoue, “Characterization of Si thin films doped by wet chemical laser processing,” *J. SID*, vol. 48, no. 1, pp. 430–432, 2017.

[11] K. Imokawa *et al.*, “Low-temperature and low-cost excimer laser doping for poly-Si thin-film transistor fabrication,” in *Proc. SPIE Laser Based Micro Nanoprocess. XIII*, 2019, Art. no. 109060J.

[12] J. P. Garandet, “New determinations of diffusion coefficients for various dopants in liquid silicon,” *Int. J. Thermophys.*, vol. 28, no. 4, pp. 1285–1303, 2007.

[13] A. Ogane, K. Hirata, K. Horiuchi, Y. Nishihara, A. K. Takahashi, and T. Fuyuki, “Laser-doping technique using ultraviolet laser for shallow doping in crystalline silicon solar cell fabrication,” *Jpn. J. Appl. Phys.*, vol. 48, no. 7R, 2009, Art. no. 071201.

[14] M. M. Mandurah, K. C. Saraswat, and T. I. Kamins, “Phosphorus doping of low pressure chemically vapor-deposited silicon films,” *J. Electrochem. Soc.*, vol. 126, no. 6, pp. 1019–1023, 1979.

[15] J. B. Boyce, P. Mei, and R. T. Fulks, “Laser processing of polysilicon thin-film transistors: Grain growth and device fabrication,” *Physica Status Solidi*, vol. 166, no. 2, pp. 729–741, 1998.

[16] L. J. van der Pauw, “A method of measuring specific resistivity and hall effect of discs of arbitrary shape,” *Phillips Res. Rep.*, vol. 13, pp. 1–9, Feb. 1958.

[17] S. Higashi, K. Ozaki, K. Sakamoto, Y. Kano, and T. Sameshima, “Electrical properties of excimer-laser-crystallized lightly doped polycrystalline silicon films,” *Jpn. J. Appl. Phys.*, vol. 38, no. 8, p. L857, 1999.

[18] J. W. Y. Seto, “The electrical properties of polycrystalline silicon films,” *J. Appl. Phys.*, vol. 46, no. 12, p. 5247, 1975.

[19] A. Scorzoni and M. Finetti, “Metal/semiconductor contact resistivity and its determination from contact resistance measurements,” *Mater. Sci. Rep.*, vol. 3, no. 2, pp. 79–137, 1988.

[20] A. J. Walker and P. H. Woerlee, “A mobility model for MOSFET device simulation,” in *Proc. 18th Eur. Solid-State Device Res. Conf. (ESSDERC)*, Montpellier, France, 1988, pp. 265–268.

[21] K. Terada and H. Muta, “A new method to determine effective MOSFET channel length,” *Jpn. J. Appl. Phys.*, vol. 18, no. 5, p. 953, 1979.

[22] A. A. Orouji and M. J. Kumar, “Leakage current reduction techniques in poly-Si TFTs for active matrix liquid crystal displays: A comprehensive study,” *IEEE Trans. Device Mater. Rel.*, vol. 6, no. 2, pp. 315–325, Jun. 2006.

[23] C.-W. Lin, C.-H. Tseng, T.-K. Chang, C.-W. Lin, W.-T. Wang, and H.-C. Cheng, “A novel laser-processed self-aligned gate-overlapped LDD poly-Si TFT,” *IEEE Electron Device Lett.*, vol. 23, no. 3, pp. 133–135, Mar. 2002.

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