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Simulation of CMOS APS Operation and Crosstalk in SPICE With Generalized Devices

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ABSTRACT We present SPICE simulations of a CMOS APS pixel element consisting of the optical sensor with the sensing circuit. The photodiode is simulated at the physics level by means of the so-called Generalized Devices, without any predefined compact model. Conversely, regular compact models are used for MOSFETs present in the circuit. Modeling with Generalized Devices takes into account in SPICE simulations both the layout and the physics of the photodiode, i.e., drift-diffusion transport, optical generation and recombination of excess carriers, capacitive effects and surface recombination. Moreover, electrical coupling between two adjacent pixels, i.e., the electrical crosstalk, is well predicted by the network of Generalized Devices. This approach is supported by TCAD Sentaurus simulations and opens the way to full SPICE simulation of Active Pixel Sensor from the circuit down to the semiconductor level within the same circuit simulation tool.

INDEX TERMS APS, image sensor, optoelectronics, photodiode, SPICE, generalized devices, minority carriers.

I. INTRODUCTION

The concept of Generalized Devices which takes into account minority carriers and related effects was first presented in [1], then extended and used to predict the impact of minority carriers injection in HV-CMOS integrated circuits in [2], [3]. Recently, following this approach, Rossi *et al.* [4], [5] included light-semiconductor interaction in these elements and demonstrated full SPICE simulation of passive photo-sensors and solar cells without any specific compact model and without introducing empirical parameters. In this work, we apply this modeling strategy to a CMOS Active Pixel Sensor (APS), simulating both the operation of a single pixel, including the photodiode and the circuit, and the crosstalk between adjacent pixels.

APS are specific architectures that include a photodiode and a read-out in-pixel circuit to measure the intensity of light. In common SPICE simulations each element, including the photodiode, comes with its compact model and related empirical parameters, all being specific to the fabrication process [6], [7]. Based on Generalized Devices introduced in [4], it was shown that a pn junction under illumination can be *physically simulated* in circuit simulators (SPICE-based softwares) without any predefined model and without fitting parameters, taking into account the layout and the semiconductor technological parameters. Still, the circuit is simulated with regular compact models. In addition to be *model independent*, this unique approach gives more flexibility to designers who can optimize the parameters of the photodetector at the layout level and assess the impact of the semiconductor parameters on pixel performances directly during SPICE simulations, thus avoiding time-consuming and costly fabrication process modifications.

In addition to the pixel sensitivity, this simulation strategy permits the prediction of crosstalk between pixels, another key parameter to describe the performance of an image sensor. The crosstalk in APS originates when a pixel at dark behaves as if it were impinged by light. While the optical crosstalk could originate if photons reach a *dark pixel* due to light beam scattering in the optical microlenses, the electrical crosstalk happens when carriers photogenerated in the illuminated pixel diffuse further towards neighbor pn junctions and produce a signal [8]. Such a crosstalk

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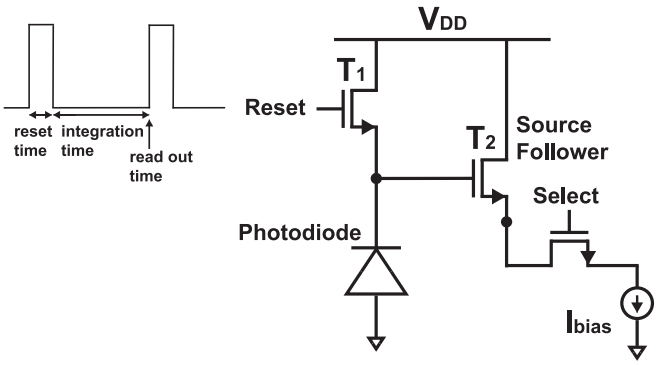

FIGURE 1. Architecture of a 3T-APS pixel.

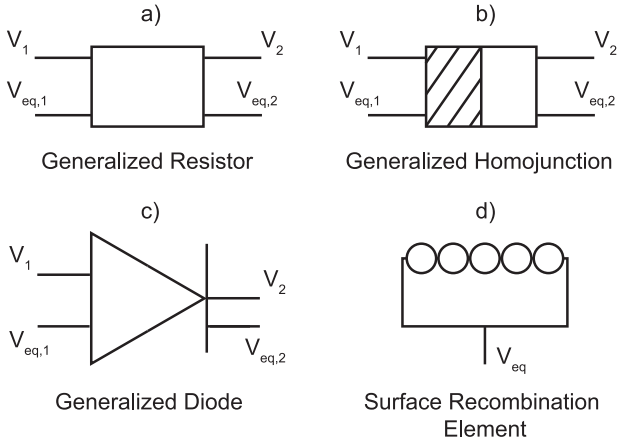

FIGURE 2. Generalized Devices.

is becoming a critical factor in new technologies as it gets worsened when pixels shrink, seriously damaging the sensor resolution [9]. Crosstalk modeling, especially electrical crosstalk, is thus mandatory to optimize pixel design. However, developing an analytical model is challenging [8] and only few analytical and semianalytical models can be found in literature [8]–[11]. Instead, in this paper we adopt a different approach using the Generalized Devices and demonstrate that electrical crosstalk can be predicted using SPICE simulations only, allowing fast design optimization including the circuit without the need to rely on TCAD simulations.

II. RECALLING APS AND GENERALIZED DEVICES PRINCIPLES

For sake of clarity, the essentials of a 3T-APS sensor and Generalized Devices are recalled in this section.

A. ARCHITECTURE AND PRINCIPLE OF AN APS PIXEL

A typical 3T-APS pixel architecture is shown in Fig. 1 [12], [13]: each APS pixel is composed of a photodiode and three MOSFETs. Prior to the measurement, the photodiode is reverse biased up to V_{DD}-V_{TH} [6] by means of T1 during the reset time, which increases the depletion charge density of the junction capacitance. Next, during the integration time, T1 is switched off. The photogenerated electron-hole pairs that are separated by the electric field in the depletion region are drifted away, resulting in a discharge of the photodiode capacitance. This will decrease the potential on the gate of T2. Therefore, the discharge time will depend on the optically-generated excess carriers, i.e., will depend on the light intensity. The output signal of the pixel, provided by the source follower transistor T2, is sampled at the end of the integration time (i.e., readout time, see Fig. 1). The select transistor, which can be omitted in our case, is part of the row and column selection circuits to access specific pixels in an image sensor. In fact, in CMOS imagers, voltage signals are readout one row at a time in a manner similar to a random access memory [14].

B. BASICS OF GENERALIZED DEVICES

The concept of Generalized Lumped Devices [4], [5] is now discussed briefly. A total of four Generalized Devices, presented in Fig. 2, are used to simulate injection, propagation (by drift-diffusion), recombination (bulk recombination as well as surface recombination) and generation (including optical generation) of excess carriers in a piece of semiconductor.

Among these elements are the Generalized Resistance, the Generalized Homojunction and the Generalized Diode which are characterized by two additional nodes that are used to simulate equivalent voltages, proportional to the excess carrier density, and equivalent currents, proportional to the excess carrier gradient. The last device is the Surface Recombination Element, single pin ended, accounting for surface recombination effects (more details can be found in [5]). The Finite Difference Method (FDM) is used to convert the set of drift-diffusion and continuity partial differential equations in a system of linear equations that can be mapped on a mesh. The linearized equation are embedded in the model describing the Generalized Devices, each corresponding to a mesh rectangle. As explained above, excess carrier concentrations and gradients are represented in the model with electrical quantities, so that they can be simulated by standard SPICE-like software. In particular, the physical model of each Generalized Device is translated into an equivalent electrical circuit and coded in Verilog-A. For instance, the equivalent circuit of the Generalized Diode is reported in Fig. 3.a. The model is divided in two parts: the Total Current Circuit (TCC) that simulates the real voltages and currents, and the Minority[1] Carrier Circuit (MCC) that simulates the equivalent voltages and currents. These two subcircuits are coupled together so that any variations in equivalent voltages and currents affect real voltages and real currents, and vice versa. The two orange rectangles in Fig. 3.a represent the *resistive* part of the diode (and in fact the equivalent

1. The term Minority is used here for continuity with previous works, but the term Excess would be more correct as it simulates both minority and majority excess carriers concentration and gradient.

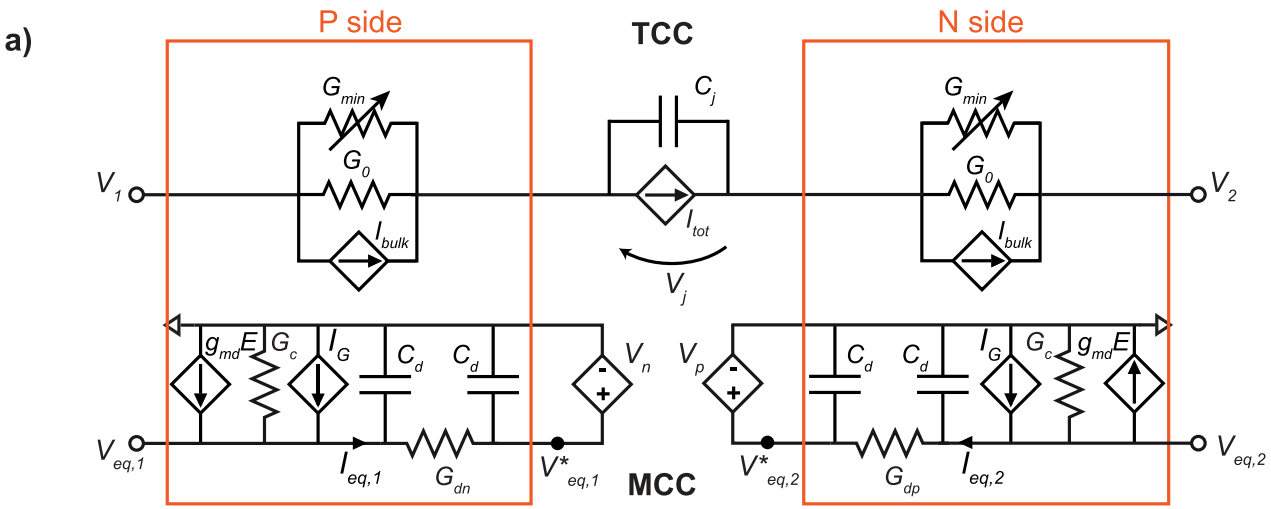

FIGURE 3. a) Equivalent circuit of the Generalized Diode. b) Expressions for the calculation of circuit elements (as a function of geometrical and technological parameters).

circuit is the same as the Generalized Resistor one) that are interconnected by the space charge region. The space charge region is described by a compact model, that is the analytical exponential law of the diode that link carrier concentrations and voltages (see [4, Appendix]), which is embedded in the voltage and current sources. Conversely, the neutral region is part of the lumped network and depends on the mesh. In fact, all the elements present in the TCC and MCC describing the neutral regions (in the orange rectangles in Fig. 3.a) have geometrical parameters that depend on the mesh size. The TCC includes a constant resistance (G_0) which represents the standard doping dependent resistance of the substrate, a variable resistance (G_{min}) that takes into account the modulation of the conductivity due to the excess minority carriers, and a current source (I_{bulk}) which is a correction term used to model the difference between majority and minority diffusion currents. In addition, the MCC includes a conductance (G_d) depending on the diffusivity that regulates the diffusion current, a conductance (G_c) depending on the electron-hole pairs lifetime (Shockley–Read–Hall model) that regulates the minority carriers recombination in the discretized volume and a current source (I_D) which holds for the excess carriers generation rate. Finally, drift is also present in the MCC through current sources ($g_{md}E$) depending on the potential drop. Importantly, diffusion capacitances (C_d) and junction capacitances (C_j) are also implemented. All the formulas to calculate these parameters are reported in Fig. 3.b (note that A and $W_{n/p}$ are the geometrical size of the mesh rectangle). In conclusion, this model, as well as for the other Generalized Devices, is fully physics based and uses only geometrical, technological and physical parameters related to the semiconductor structure, hence it does not need any fitting parameter.

A proper meshing strategy is crucial to obtain accurate simulations with low computational time. The rule is that mesh size must be lower than the diffusion length of carriers in the semiconductor. Moreover, in presence of photogeneration, i.e., near the surface, mesh must be refined to correctly linearize the exponential characteristics of light absorption. Mesh optimization has been carried out in [4] and a rule of thumb has been proposed: the mesh size should be one fifth of the diffusion length when photogeneration is negligible, whereas one fifth of the absorption length (α^{-1}) of impinging light for regions where light absorption impacts the free carrier concentration (between the surface and about $4\alpha^{-1}$ for illuminated regions).

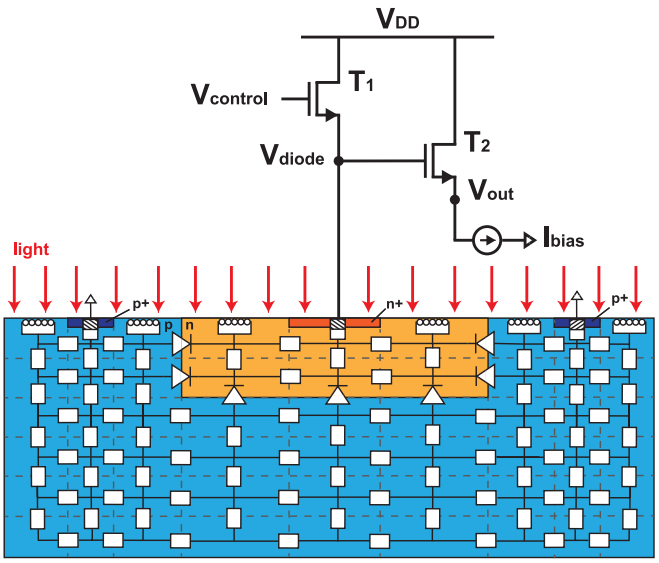

FIGURE 4. Equivalent APS circuit with Generalized Devices.

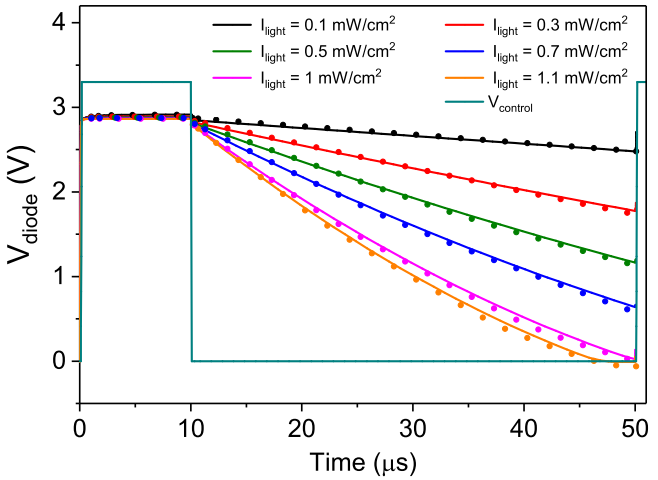

FIGURE 5. Time dependence of the voltage at the cathode of the pn junction under illumination for different light intensities. Results obtained with the Generalized Devices model are plotted with solid lines while TCAD simulations results are plotted with symbols.

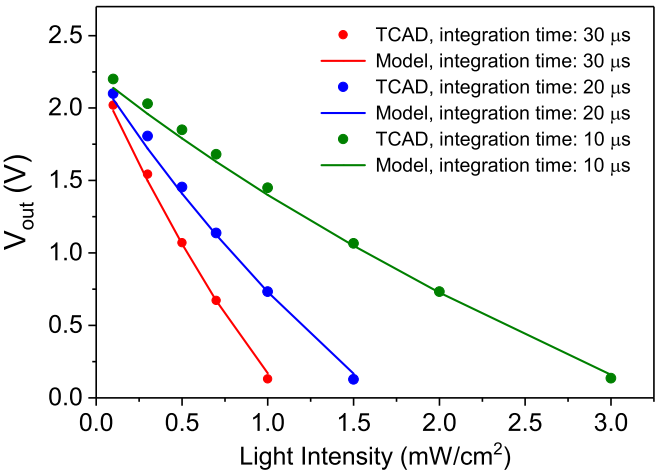

FIGURE 6. APS output voltage at the source of T2 as a function of illumination intensity for different integration times.

III. SPICE SIMULATION OF A SINGLE PIXEL

In this section, the 3T-APS pixel is simulated using the Generalized Devices approach. The photodiode is modeled as a network of Generalized Resistors, Diodes, Homojunctions and Surface Recombination Elements, whereas standard compact models are used for the transistors. The structure of the photodiode with a sketch of the mesh, following the meshing principle presented in Section II-B, and the APS circuitry is shown in Fig. 4. The n-well of the photodiode has an area of 30 μm^2, it is 3 μm deep and doped at 10^{16} cm^{-3}. The p-substrate is doped at 10^{16} cm^{-3}. Highly doped regions (10^{19} cm^{-3}) are used for Ohmic contacts. A monochromatic light with a wavelength of 600 nm (red light) is used for illumination. Regarding the circuit, the two transistors T1 and T2 are simulated using the BSIM3 compact model (a 0.18 μm CMOS technology is considered) and both have a channel length and width of 180 nm and 240 nm respectively. The bias voltage (V_{DD}) and bias current (I_{bias}) are set to 3.3 V and 1 μA. Fig. 5 shows the voltage on the cathode of the photodiode (connected to the gate of T2) for different illumination intensities during reset and integration times. The model (solid lines) is in good agreement with the numerical simulations (dots) performed with Sentaurus TCAD software for validation. Importantly, the same physical and technological parameters were used in both cases. In fact, as stated in the previous section, Generalized Devices do not need any fitting parameter and use only quantities related to the geometry and to the semiconductor characteristics, such as the doping, the mobility, the lifetime, etc. It must be underlined that the computation time required for the SPICE simulation of the structure using the Generalized Devices approach is about three orders of magnitude lower with respect to the computation time required for the TCAD numerical simulation of the same structure using the same hardware. Nevertheless, SPICE simulations predict accurately the transient discharge of the photodiode capacitance upon illumination, as well as the saturation of the signal for high light intensities. Indeed, for a given integration time, there is a particular value of the light intensity that fully discharges the capacitance (i.e., zero voltage at the cathode of the photodiode). Note that for higher illumination densities, this zero voltage is reached before the end of the integration time, which would require shorter integration periods.

Given that the photodiode and the circuit are co-simulated in SPICE, not only the photodiode sensor is simulated at the semiconductor level, but also the output voltage of the APS circuit is predicted. The different curves in Fig. 6 represent the output voltages readout after different integration time. Again, the results obtained with the model match quite well TCAD simulations, including the slightly non-linear dependence. Decreasing the integration time, higher light intensities could also be detected, but this will also

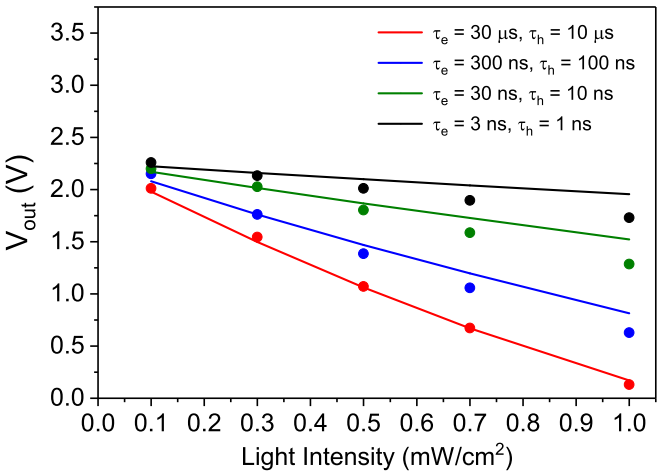

FIGURE 7. Impact of electron lifetime (τ_e) and hole lifetime (τ_h) on the APS output voltage for an integration time of 30 μs (solid lines for model results and symbols for TCAD simulations).

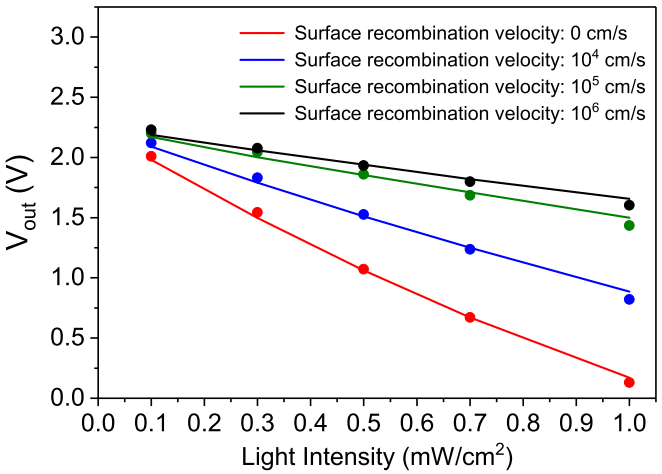

FIGURE 8. Impact of the surface recombination velocity on the APS output voltage for an integration time of 30 μs (solid lines for model results and symbols for TCAD simulations).

degrade the resolution for lower intensities. Therefore, the integration time is critical and depends on the range of illumination foreseen. Using the proposed modeling approach, this kind of technological-versus-circuit optimization can be carried out during SPICE simulations.

IV. PREDICTING THE IMPACT OF KEY PHYSICAL PARAMETERS ON PIXEL EFFICIENCY

Since the Generalized Devices approach relies on geometrical and physical parameters only, this can also be used to study the how those parameters affect the output voltage, and so the overall APS performance.

A. IMPACT OF BULK LIFETIME ON THE OUTPUT SIGNAL

The recombination lifetime plays an important role when dealing with optoelectronic devices since the collection efficiency of photogenerated carriers can drop dramatically when the carrier lifetime is small, i.e., in the ns range for instance. The lifetime of electrons and holes in the semiconductor substrate was varied from 30 μs for electrons and 10 μs for holes, down to 3 ns for electrons and 1 ns for holes. As it can be noticed in Fig. 7, the mismatch increases for shorter lifetimes. This is because the diffusion length decrease with decreasing lifetime, thus requiring a finer mesh for an accurate linearization, as explained in Section II-B. The simulations reported in Fig. 7 predict a limited range of the output voltage variation when decreasing the carriers lifetimes. To overcome this issue, the integration time should then be increased in order to obtain a steeper slope for the output voltage-light intensity dependence.

B. ACCOUNTING FOR SURFACE RECOMBINATION

Another important semiconductor parameter that must be taken into account when dealing with optoelectronics is the surface recombination velocity. In fact, surface recombination can significantly degrade the photodiode performances, as light absorption peaks at the semiconductor surface [15].

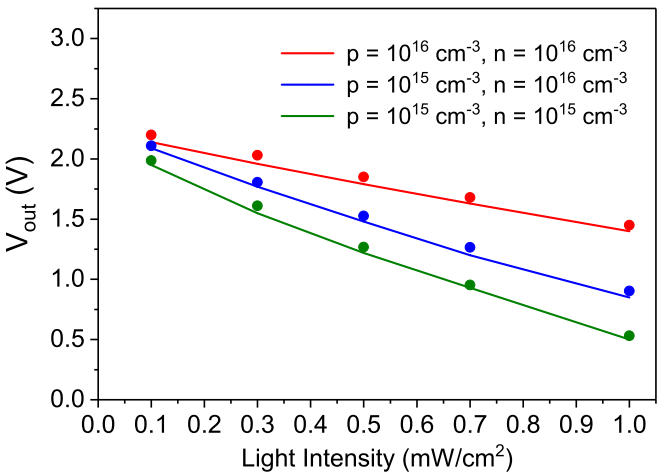

FIGURE 9. Impact of the p-substrate and n-well doping densities on the APS output voltage for an integration time of 10 μs (solid lines for model results and symbols for TCAD simulations).

Typical values of surface recombination velocities for bare silicon wafers are 10^3 to 10^5 cm/s, depending on the fabrication process, doping type and concentration. Note that a value of 10^6 cm/s can be considered as an infinite surface recombination velocity [16], [17]. Simulations including surface recombination velocities based on the Generalized Devices and TCAD simulations presented in Fig. 8 confirm that this feature can also be tracked during SPICE simulations.

C. IMPACT OF THE DOPING CONCENTRATION

The output voltage of the APS is analyzed for different doping levels of the p-type substrate and n-well. The doping affects the depletion region, and so the capacitance of the photodiode which translate light into an electrical quantity. As such, it has a key role in the operation of the pixel sensor, in addition to modify the built-in voltage. Fig. 9 shows the results obtained with the Generalized Devices model and TCAD simulations. For lower doping densities, the depletion

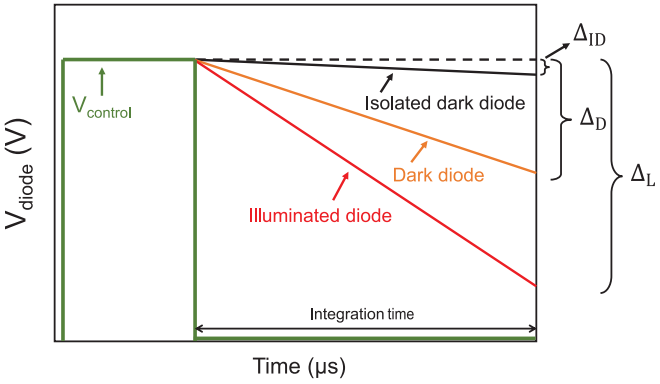

FIGURE 10. Definitions of voltage drops (Δ_L, Δ_D and Δ_{ID}) on the cathode of the photodiodes in case of illuminated pixel, dark pixel and isolated dark pixel.

region increases and the photodiode capacitance decreases. Therefore, keeping the same reverse bias voltage during reset mode, the stored charge is lower. Since for a given light intensity the electron-hole pairs generation will not change, the charge in the junction capacitance and the resulting voltage on the cathode of the photodiode will decay faster, resulting in a lower output voltage of the APS sensor at the end of the integration time, 10 μs in this case. Note that for the intensity of light used in this work, longer integration times would totally discharge the capacitance of the photodiode when the doping densities are set to 10^{15} cm^{-3} (same for n and p type), meaning that the output signal would saturate, as discussed in Section III.

V. CROSSTALK BETWEEN ADJACENT PIXELS

As already stated above, crosstalk originates when carriers photogenerated in a pixel (i.e., illuminated) diffuse towards a neighbor pn junction, thus producing an additional output signal (note that the neighbor pixel can also be illuminated). Before analyzing crosstalk, we must agree on a sound definition since different denotation can be found in literature [8], [18]. In our analysis, we propose to define crosstalk as follows:

$$CTK(\%) = \frac{\Delta_D - \Delta_{ID}}{\Delta_L - \Delta_{ID}} \times 100$$

where Δ_L and Δ_D are the differences in the output voltage taken at the beginning and the end of the integration time for the illuminated pixel and dark pixel respectively (i.e., the non-illuminated pixel in the neighborhood of the illuminated pixel subjected to crosstalk), and Δ_{ID} is the difference in the output voltage between the beginning and the end of the integration time for an isolated dark pixel (i.e., the voltage drop is only due to the thermal current of the pn junction). The definitions of Δ_L, Δ_D and Δ_{ID} are graphically explained in Fig. 10.

Adopting this definition, the crosstalk between two pixels is simulated using the Generalized Devices modeling approach and compared with Sentaurus TCAD simulations. The structure of interest is reported in Fig. 11. The pixel on the right side (pixel 2) is illuminated while the pixel on the left side (pixel 1) receives no light at all. This configuration represents the worst case scenario when dealing with crosstalk since photodiodes are separated by the minimum dimension as there is no in-pixel electronics between them [8]. Fig. 11 sketches the network of Generalized Devices used to model the pixels architecture which is connected to the compact models for the APS circuit. It is important to note that the network of Generalized Devices interconnects the dark and illuminated pixels and can thus simulate the propagation of photogenerated carriers from one pixel to the other. This is the key feature enabling prediction of crosstalk between pixels. Moreover, as already stated above, there is no need of any fitting parameters, as the model is physics based and only uses geometrical and technological parameters.

A. FRONT-SIDE ILLUMINATION

In this section, crosstalk is simulated in case of a front side illumination of the pixel 2 (see Fig. 11). Each pixel has the same dimensions than the one simulated in Section III, and the distance between the pn junction is set to 30 μm. Fig. 12 shows the time evolution of the voltage on each photodiode during the integration time. The reset signal ($V_{control}$) for the integration time is the same for both pixels. Moreover, the time dependence of the voltage for an isolated photodiode at dark (isolated structure with no collection of photogenerated carriers from neighbor pixels, i.e., only subjected to thermal generation) is also plotted in Fig. 12. The model (solid lines) is in good agreement with the TCAD simulations (symbols) performed on the same structure. The crosstalk predicted with the model is about 11%, while for TCAD it is of 7.9%. This means that the network of Generalized Devices can simulate not only the photogeneration of carriers in the illuminated pixel, but also their propagation and collection towards each pn junction with enough accuracy for a fair evaluation of crosstalk simulated at the output node of the photodiodes.

B. BACK-SIDE ILLUMINATION

In recent years, the demand for higher resolution camera has led to dramatic pixel shrinkage. As a consequence, the percentage of pn junction area exposed to impinging light (not shadowed by metallic interconnections) decreased by a great amount. To solve this issue, state-of-the-art CMOS image sensors are using back-illuminated pixel technology. The back-side illumination requires the thinning of the active silicon layer (where photogeneration takes place) in order to avoid excessive crosstalk. In fact, as it will be explained in paragraph 3, crosstalk strongly depends on the silicon layer thickness. Papers in recent literature report that for pixel sizes of 1 μm to 3 μm, the silicon thickness is about 3-4 μm [19]–[25]. Following this analysis, we discuss simulation of crosstalk when considering a pixel size of 3 μm, a silicon thickness of 4 μm, a pn junction width and depth

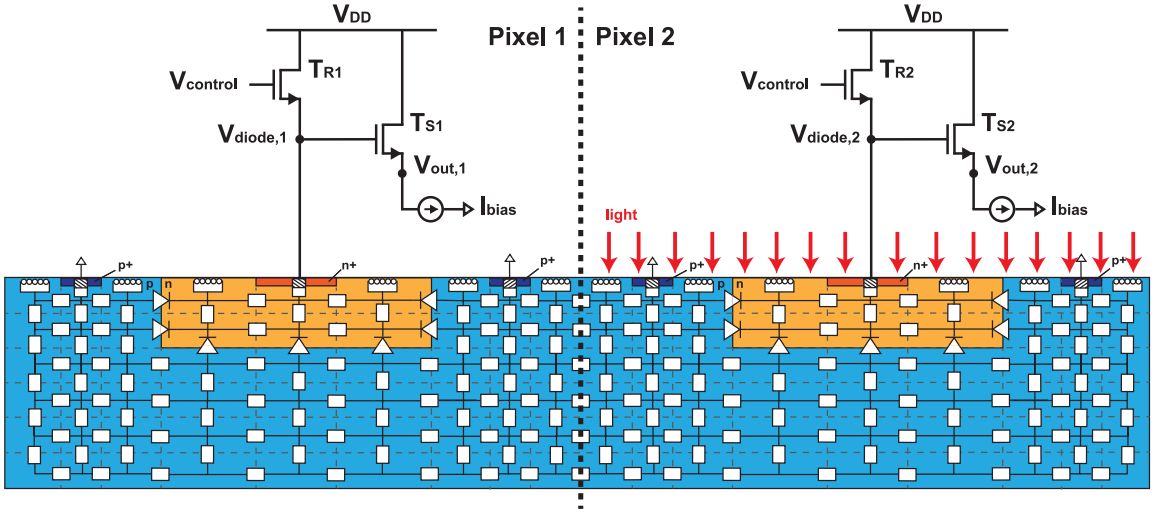

FIGURE 11. Equivalent circuit with Generalized Devices for two adjacent pixels.

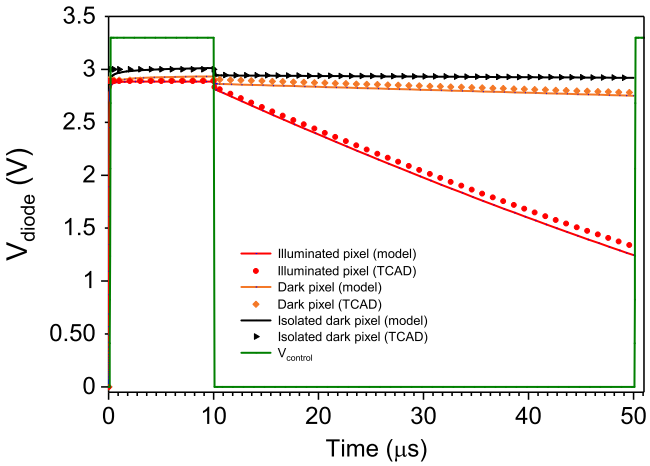

FIGURE 12. Crosstalk study for front-side illumination: time dependence of the voltage at the cathode of the pn junctions for different illumination conditions. Results obtained with the Generalized Devices model are plotted with solid lines while TCAD simulations results are plotted with symbols.

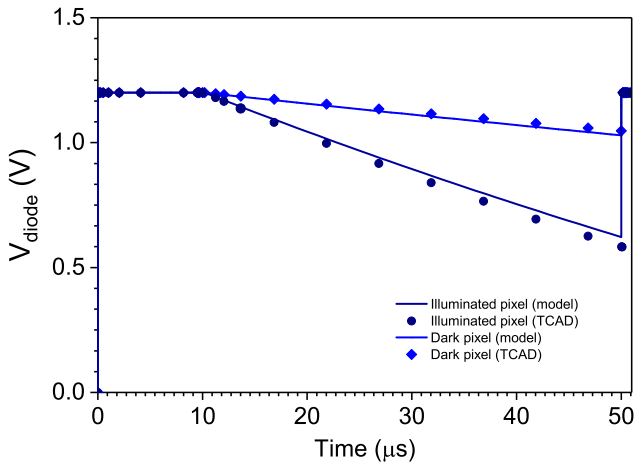

FIGURE 13. Crosstalk study for back-side illumination (smaller pixels) with no in-pixel transistors, only switches: time dependence of the voltage at the cathode of the pn junctions for different illumination conditions. Results obtained with the Generalized Devices model are plotted with solid lines while TCAD simulations results are plotted with symbols.

of 1.5 μm and a distance between two adjacent pn junctions of 1 μm.

B.1. PIXEL ARCHITECTURE ONLY WITH SWITCHES

The 2-pixels structure is simulated first by substituting all the transistors in Fig. 11 with simple passive switches in order to avoid considering transistors compact models and focus on the substrate model only. Indeed, in this case the photodiode is much smaller than in Section V-A and the transistor capacitances cannot be neglected with respect to the capacitance of the photodiode. As we will see, MOSFET capacitances can be responsible for non-idealities in the voltage characteristics. For a proper validation of the model, this must be identified separately.

Fig. 13 reports the simulations for the model and TCAD with ideal switches. The pixel on the right side (see Fig. 11) is illuminated with a red light (wavelength of 600 nm) using an intensity of 1 mW/cm^2 while the left one is not illuminated. The supply voltage V_{DD} is set to 1.2 V and the integration time to 40 μs. To improve the accuracy of the simulation, we slightly modified the model of the diode so as to take into account corners of the pn junction. As depicted in Fig. 4 and Fig. 11, the pn junction is modeled using several Generalized Diodes in parallel. In Sections III and V-A the model used an equivalent length given by the sum of the bottom and lateral sides of the rectangle, thus ignoring 2D effects. Results were still accurate as the contributions to the depletion region of corners was negligible. As the size of the pn junction shrinks, its shape looks more as a square than an elongated rectangle. We then suppressed the overlap between the depletions regions at the corners

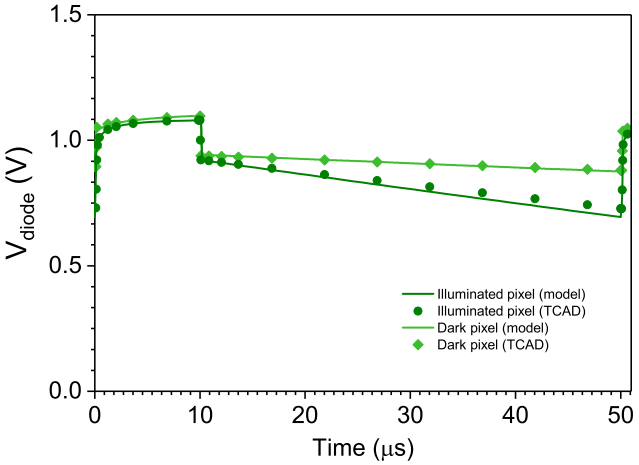

FIGURE 14. Crosstalk study for back-side illumination (smaller pixels) with in-pixel transistors: time dependence of the voltage at the cathode of the pn junctions for different illumination conditions. Results obtained with the Generalized Devices model are plotted with solid lines while TCAD simulations results are plotted with symbols.

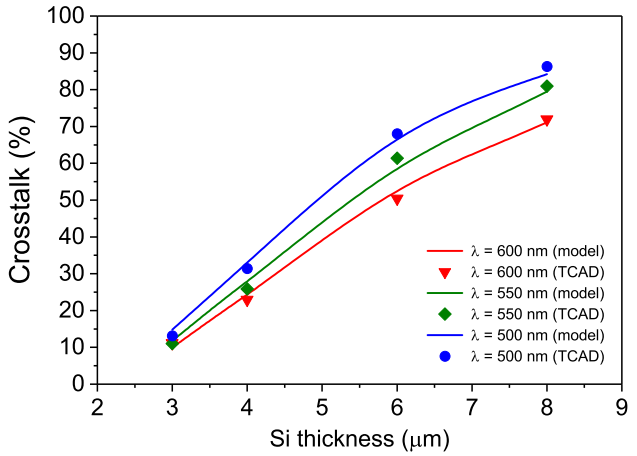

FIGURE 15. Impact of silicon layer thickness in back-side illuminated pixels and wavelength on crosstalk (solid lines for model results and symbols for TCAD simulations).

which are still calculated under the full depletion approximation in one dimension. Deriving a depletion region in 2D for corners is not straightforward. In addition, this will make the model quite complex, while this simplified view gives acceptable results. Indeed, the model can accurately predict the voltage characteristics of each diode as shown in Fig. 13. The crosstalk obtained with the model is 27.4% compared to 24.8% for TCAD.

B.2. PIXEL ARCHITECTURE WITH TRANSISTORS

Since the intrinsic pixel operation, without transistors, has been validated, we can now assess the complete pixel architecture including all the transistors as shown in Fig. 11.

Fig. 14 reports the time evolution of the voltage on the cathode of the two photodiodes (one in the illuminated pixel and one in the non-illuminated pixel) simulated with the model and with TCAD. An external capacitance of 0.1 fF has been added between the gate and the source of the transistors in the model in order to precisely match the capacitances in the compact model of the transistor used in the TCAD tool. In fact, any minor difference in compact models (especially for capacitances) can lead to significant mismatch for such small pixel dimensions since transistors capacitances are no longer negligible with respect to the capacitance of the photodiode. For instance, as can be noted in Fig. 14, the presence of transistors instead of switches is responsible for a *jump* in the transient characteristics, a feature that was not present in Fig. 13 (pixel with ideal switches). This jump is attributed to the charge injection from the MOSFETs when switching.

The model can simulate the full architecture of the pixel including now the transistors as in regular APS, both for front and back side illumination and with state-of-the-art dimensions. Not only the output voltage, but also crosstalk figures of merit can be predicted within the same SPICE environment. For instance, the crosstalk predicted with the model is 24.3%, very close to the value simulated with TCAD, i.e., 23%.

B.3. IMPACT OF SILICON THICKNESS AND WAVELENGTH ON CROSSTALK

As stated before, the thickness of the silicon layer is a key feature for the optimization of the sensitivity to light and crosstalk in back-illuminated APS.

Fig. 15 reports the crosstalk as a function of the silicon thickness for different wavelength (corresponding to blue, green and red light). Importantly, the crosstalk simulated with the model (solid lines in Fig. 15) is in good agreement with TCAD results (symbols) for a wide range of silicon thicknesses and wavelengths. It is possible to note how large the crosstalk becomes for high thicknesses, reaching already 50% for about 5 μm. Based on these SPICE simulations, the acceptable values of silicon thickness are found to be in the range of 3–4 μm, as thinner thicknesses would provide a too low signal on the illuminated pixel. This illustrates how *physics-based* simulations can be carried out in SPICE, together with circuit simulations.

VI. CONCLUSION

A SPICE-compatible model based on Generalized Devices was used to simulate a CMOS 3T-APS with traditional circuit simulation tools. The main advantage of this approach is the co-simulation of the circuit with the sensing device, i.e., the photodiode, including photogeneration of excess carriers, propagation, recombination and surface recombination effects. This peculiarity allows studying the impact of geometrical and technological parameters of the photodiode on the final analog output voltage of the APS, before digital conversion. Moreover, the computation time required for this approach is about three orders of magnitude lower with

respect to numerical simulation with TCAD tools. The voltage at the cathode of the photodiode and at the output of the APS, i.e., after the source follower stage, were simulated for different light intensities. The dependence of the APS dynamic range with respect to major semiconductor physical parameters was evidenced within SPICE simulations, and a good agreement was found in regard to full numerical TCAD simulations. Next, the electrical crosstalk in two adjacent APS was also predicted by the model for front-side and back-side illumination without any fitting parameters, including the impact of the silicon thickness layer on the crosstalk for back-side illuminated APS. This study confirms that using Generalized Devices, the semiconductor, the layout, and the circuit can be coherently co-simulated in SPICE.

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